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Power, Readout and Service Hybrids for the CMS Phase-2 Upgrade

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Abstract

The CMS tracker Phase-2 upgrade silicon modules integrate DC-DC powering stages and an optical transceiver to power and control the front-end hybrids. The strip-strip (2S) module contains a Service Hybrid (2S-SEH) with two-stage DC-DC power conversion, an lpGBT with optical interface (VTRx+), high voltage biasing and temperature sensor ports. The pixel-strip (PS) module utilizes a separate two stage DC-DC converter circuit (PS-POH) and a Readout Hybrid (PS-ROH) containing the communication interface. The design and performance of these three hybrids and their integration in their respective modules are presented.

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Power, Readout and Service Hybrids for the CMS Phase-2 Upgrade

Angelos Zografos[a,1,2], **Georges Blanchot**[a], **Irene M. Dominguez**[a], **Adam E. Hollos**[a], **Mark I. Kovacs**[a] **and Nikola Rasevic**[b]

[a] *CERN*
CH-1211 Geneva 23, Switzerland
[b] *University of Novi Sad,*
Trg Dositeja Obradovića 6, 21101 Novi Sad, Serbia
E-mail: angelos.zografos@cern.ch

ABSTRACT: The CMS tracker Phase-2 upgrade silicon modules integrate DC-DC powering stages and an optical transceiver to power and control the front-end hybrids. The strip-strip (2S) module contains a Service Hybrid (2S-SEH) with two-stage DC-DC power conversion, an lpGBT with optical interface (VTRx+), high voltage biasing and temperature sensor ports. The pixel-strip (PS) module utilizes a separate two stage DC-DC converter circuit (PS-POH) and a Readout Hybrid (PS-ROH) containing the communication interface. The design and performance of these three hybrids and their integration in their respective modules are presented.

KEYWORDS: Data acquisition circuits; Front-end electronics for detector readout; Radiation-hard electronics; Detector design and construction technologies and materials.

[1] Corresponding author.
[2] On behalf of the CMS Tracker Group

Contents

1. Introduction

A major upgrade of the CMS detector is required to cope with the planned luminosity of the High Luminosity LHC (HL-LHC) [1]. The development of the new front-end silicon modules for the CMS Outer Tracker aims to deliver higher granularity, lower mass and the capability for higher data rates. The rejection of low momentum tracks for the L1 track trigger is executed in the front-end electronics by correlating the signals locally from a pair of silicon sensors [1].

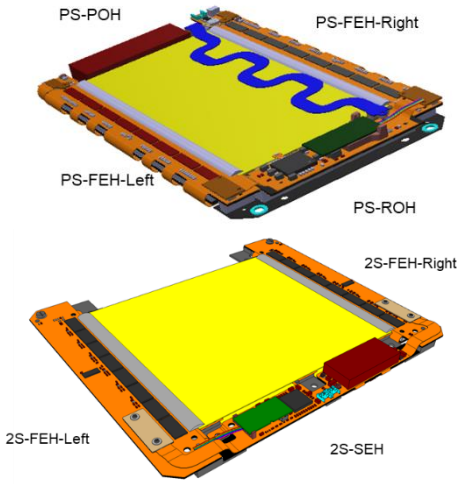

Figure 1. Latest 3D models of the PS module (top) and 2S module (bottom). The hybrids are labelled.

The upgraded Outer Tracker design is made of two main module types each with different sensor separations ranging from 1.6 mm to 4 mm: the Strip-Strip (2S) modules, which feature strip sensors, and the Pixel-Strip (PS) modules, which combine a strip and a macro-pixel sensor (**Figure 1**). These modules are operated at −35 ºC. Both modules contain two front-end hybrid circuits (FEH). The power distribution and optical data transmission and control services are handled by the 2S Service Hybrid (SEH) in the case of the 2S module and by the PS Power Hybrid (POH) and the PS Readout Hybrid (ROH) for the PS module.

The hybrid circuits that constitute the two types of modules of the Outer Tracker are a challenge both in terms of design and in terms of manufacturing. Challenges range from the constrained dimensions (board area and height) to the requirements for efficient power delivery and thermal performance. Low conducted and radiated emissions need to be achieved and the material budget must be limited. The designs have to fulfill all the requirements while avoiding inflating the cost up to prohibitive levels. This is a challenge, since the required quantities (5592 PS modules and 7608 2S modules) are too small to be able to use many custom solutions and at the same time too big to allow for excessive use of manual operations at the manufacturing level.

2. PS Power Hybrid

The PS-POH (**Figure 2**) is responsible for delivering the power to the ASICs of the PS module. Three different voltages (1.25 V, 1.05 V and 2.55 V) are required for the operation of the 16 MPAs (Macro Pixel ASIC), 16 SSAs (Short Strip ASIC), 2 CICs (Concentrator Integrated Circuit), one lpGBT (Low Power Giga Bit Transceiver) and a VTRx+ (Versatile Link Transceiver) of the module for a total power of around 5.5 W nominal. It achieves this using radiation tolerant DC-DC converter ASICs in two stages (**Figure 3**): the bPOL12 (buck converter, QFN32 package) and the bPOL2V5 (buck converter, bump bonded bare die). The MPAs and SSAs minimize the power consumption by utilizing different power domains for analog, I/O and digital supplies: 1.25 V for the two former and 1.05 V for the latter. To avoid having protection diodes from input to VDD conducting during system startup, power sequencing was implemented. Finally, the circuit is designed so that a single version is manufactured, featuring flexible tails that can adapt for all three PS module types.

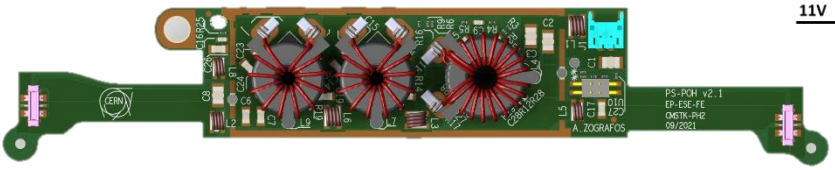

Figure 2. PS-POH v2.1, production version 3D model without shield.

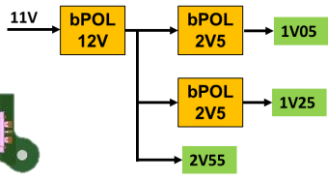

Figure 3. Two-stage DC-DC conversion.

2.1 Custom components

Two different inductors and an electromagnetic interference (EMI) shield are custom built for this circuit.

The DC-DC converters used in this circuit require big value inductors: one with an inductance of 220 nH for the bPOL12 switching at 2.5 MHz – a little bit higher than the region of maximum efficiency of the chip – and two with an inductance of 100 nH for the bPOL2V5 switching at 4 MHz. 3D printed samples were used to verify the coils' designs' geometry and electrical characteristics. A few hundred pieces were later built with soldering temperature withstanding Liquid Crystal Polymer (LCP) and used to build prototypes for the circuit. The coils are air-core, as required for the high magnetic field intensity environment of the CMS Outer Tracker. The particular design allows for a better defined placement of the coils and the possibility for full SMT assembly, thanks to the provided guiding pin and well-defined contacts (**Figure 4**).

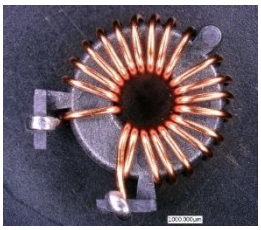

Figure 4. 220nH inductor.

The shield is made of aluminum, plated with nickel and tin to enable its soldering. Two different manufacturing techniques were exercised: folded and soldered, and micro-milled (**Figure 5**). For the former, a thin etched aluminum foil is folded into a box shape and the edges are soldered. In the case of the latter, the shield is milled with high precision from a block of aluminum. The micro-milled solution cannot be as thin as the folded and soldered version, but it can be manufactured to a much higher precision. The limitations of space and the bulkiness of the air-core inductors put the geometric tolerance requirements well into the "fH" category of the ISO2768 standard to allow the shield to fit into the available space and to be soldered reliably on

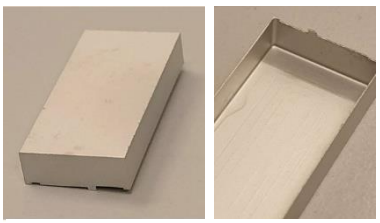

Figure 5. Micro-milled shield.

the circuit without touching nearby components. Because of this, the design moved towards the 150 µm micro-milled solution despite it being heavier than a 100-120 µm thick shield that would offer sufficient shielding for frequencies greater than 2 MHz emitted by the DC-DC converters.

2.2 PCB and layout considerations

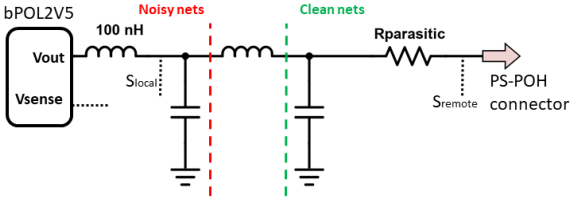

Figure 6. bPOL2V5 output sensing options. Definition of clean and noisy nets.

Two main considerations contributed to the choice of the printed circuit board (PCB). First, to achieve good thermal performance in the sense of reducing as much as possible the thermal resistance between the main heat producers on the board (ASICs and air-core inductors) and the bottom of the circuit, which is where, at the module level, the cooling of the hybrid will take place. Second, to reduce the power losses on the circuit itself without adding unnecessary mass by increasing excessively the copper thicknesses. The voltage drops on the 1.25 V and 1.05 V rails were also an important parameter to control since the powering of the PS module was found to be critical in power integrity simulations. This issue has been resolved, though, by changing the powering scheme of the PS module to include an extra powering tail directly connecting the PS-POH to the PS-ROH and by using remote sensing on the PS-POH's second stage DC-DC converters and effectively removing any non-ground-induced voltage drops between the second stage DC-DC converters and the connectors of the hybrid (**Figure 6**). Originally, the power to the PS-ROH was provided solely by the PS-FEH-Right.

Soldermask	Soldermask
Copper	Copper
Polyimide	Polyimide
Copper	Copper
Polyimide	Polyimide
Copper	Copper
Polyimide	Polyimide
Copper	Copper
Soldermask	FR4 w. thermal vias
CF stiffener	Copper
Compensator	Soldermask
Hard adhesive	Soft adhesive
CF Baseplate	CF Baseplate

Figure 7. Stack-ups considered for the PS-POH (main area).

Different stack-ups were considered, with two of those worth mentioning here (**Figure 7**). A carbon fiber (CF) stiffened flex, as used in the other hybrids of the PS module, and a relatively standard FR4-stiffened rigid-flex. The latter is not only simpler and cheaper to produce, but also can achieve a much smaller thermal resistance. This is the case because of the lack of the compensator layer (which is a thermal insulator) necessary for the CF stiffened version, and of the possibility of the addition of blind thermal vias between the last two layers. The only disadvantage of this stack-up is the CTE mismatch (~16 ppm/K) with the CF baseplate (200 µm thick support upon which the hybrids and the sensors are glued) of the PS module, which requires the use of flexible glue for the adhesion of the hybrid to this CF baseplate. Finally, the copper thicknesses were chosen by running different power integrity simulations and trying to reach a compromise between power losses on the PCB itself and the total weight added (**Figure 8**).

Main circuit copper	GND drop Left	Power Loss on PCB	Copper mass
9/9/9/9/9 µm	19mV	419mW	baseline
20/15/15/20/9 µm	11mV	214mW	+2kg
30/20/20/30/9 µm	8mV	151mW	+4kg

Figure 8. Copper thicknesses, GND voltage drop, power loss & total mass of all POHs needed for the detector. Voltage drops on the other nets do not appear because of remote sensing. The copper thicknesses defined with the manufacturer were very close to the 214 mW solution.

To keep radiated and conducted EMI low, because of the proximity of the circuit to the silicon sensor, all noisy nets – defined as the ones between power input/output of the DC-DC converters and pi filters (**Figure 6**) – are enclosed completely by ground nets below and the grounded shield from the top. Capacitors

in pi filters wherever possible come in parallel, opposite facing pairs. Finally, all single ended lines are routed using only staggered vias to increase reliability.

3. PS Readout Hybrid

The PS-ROH (**Figure 9**) fitted with a VTRx+ is responsible for data exchange (opto-electrical conversion) and control of the PS module [2]. It hosts one lpGBT, a connector for the VTRx+ and a thermistor on a small flexible tail to be glued onto the strip sensor. It has two fine-pitch connectors on flexible tails to connect to the PS-FEHs on the left and right sides and one small connector to connect to a powering tail that brings in directly the 1.25 V from the PS-POH.

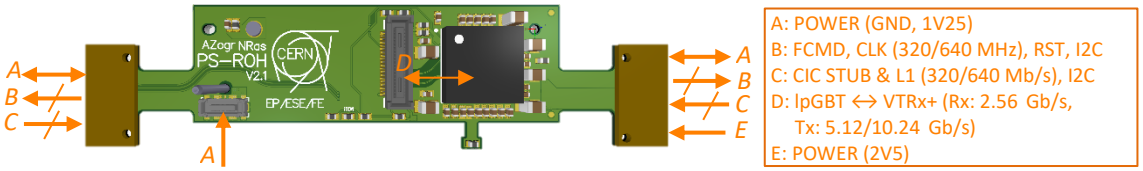

Figure 9. PS-ROH top view and functional diagram. Uplink speeds are selectable with a jumper.

The PCB is a four-layer flex with 12 µm thin copper and polyimide layers, stiffened with a CF stiffener and compensated on the opposite side to keep the circuit flat after lamination [3]. In order to have one version of the circuit for the three different spacings of the PS module, three different aluminum nitride (AlN) spacers were designed to be glued under the hybrid, one for each of the PS module versions (**Figure 10**). The fragility of the AlN spacers was identified, especially in the thinner versions. In order to address this without adding unnecessary mass, the spacer walls become progressively thicker as their height gets smaller (**Figure 11**).

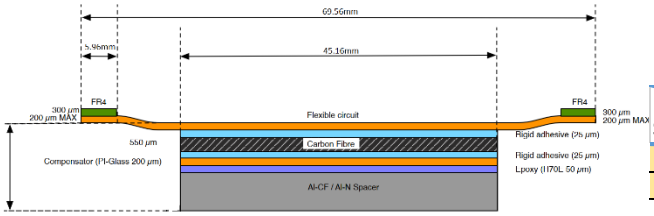

Figure 10. PS-ROH side view.

Spacer \ Module type	1.6mm	2.6mm	4mm
Height	825µm	1825µm	3225µm
Wall thickness	700µm	600µm	500µm

Figure 11. Spacer Top view and wall thicknesses.

The VTRx+, when connected to the PS-ROH, is placed very close to the sensor of the module. It was identified that light leakage from the front and sides of the VTRx+ illuminates the sensor. The analog front-end is not sensitive to the multi GHz operation of the optical links but the increase in leakage current in the sensor was deemed undesirable. A plastic support was designed to be glued on top of the PS-ROH to protect the VTRx+ and shield this light leakage (**Figure 12**). However, the part was expensive to manufacture (1 mm and 2 mm thin walls) and not effective enough in stopping the light leakage.

Figure 12. Vtrx+ support.

The final version of the circuit features thinner and longer tails by reducing the width of the FR4 side stiffeners, to make them more flexible and ease the module assembly procedures and pre-bending. Finally, the AlN spacer and CF stiffener were made less wide to limit their mass.

4. 2S Service Hybrid

The 2S-SEH is serving the combined purposes of the PS-POH and PS-ROH for the case of the 2S module. It includes a two-stage DC-DC conversion (with a single second stage DC-DC

converter, not requiring the 1.05 V output), an lpGBT and a VTRx+ connector. It also hosts a high voltage (HV) filtering circuit, with connectors to host the tails that transmit the high voltage to the sensors of the module and one for a tail hosting the thermistor for sensor temperature sensing. A folded-over area is hosting this functionality (**Figure 13**). The air-core coils and the shield are the same as the ones described for the PS-POH. The circuit is the same for the two 2S module spacings. This is achieved by implementing long flexible tails and an adapted placement of hosting connectors on the 2S-FEHs for the two different spacings.

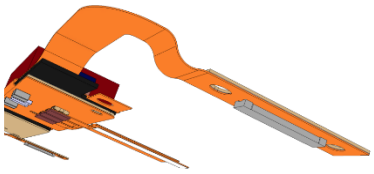

Figure 13. Fold-over area with HV and temperature sensing tails.

As this is a CF stiffened 5-layer flexible circuit, a compensator is needed, as is the case for the PS-ROH. Here, though, the cooling of the circuit is critical since, unlike the PS-ROH, it hosts DC-DC converters. To achieve good thermal contact with the cooling points of the circuit on the 2S module (**Figure 14**), the compensator of the circuit has to be split into two pieces, even though it complicates the assembly of the circuit.

5. Performance and module integration

The designs of the circuits are all ready for the production. They have been iterated in prototyping runs and tested with dedicated test systems developed for each of them. The same test systems will be used to test the hybrids also during production.

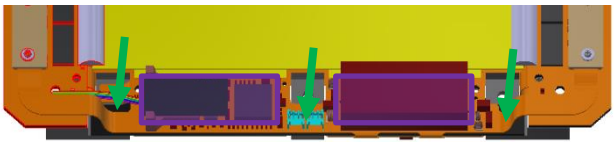

Figure 14. 2S-SEH in a module. Green arrows point to cooling locations. Purple boxes show the location of compensators.

The PS-POH achieved an average power efficiency of 65% for an input voltage of 10 V at nominal load conditions of the PS module. The output ripple on all three outputs was measured and found to be in the range of 500-900 μVrms (integrated over 10 Hz-20 MHz range). No noise increase was picked up by the analog front-ends along the PS-POH side in prototype PS modules, implying that the radiated EMI is low enough. Finally, no issues with mechanical integration in modules were found.

The PS-ROH latest working prototype suffered from some (manageable) mechanical integration issues that are fixed in the latest design. Electrically on the other hand, the hybrid is working as expected, with the operation at 5.12 Gb/s, 320 MHz and 10.24 Gb/s, 640 MHz in all differential pairs found to be reliable even at the lower output current settings, uplink and downlink, in the test system and in modules.

Finally, the 2S-SEH has been tested warm and cold (−35 °C), showing reliable operation both when being tested and when used in prototype 2S modules.

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