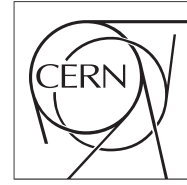




The Compact Muon Solenoid Experiment
Conference Report

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The Apollo ATCA Design for the CMS Track Finder and the Pixel Readout at the HL-LHC

A. Albert, Z. Demiragli, D. Gastler, K. Hahn, E. Hazen, P. Kotamnives, S. Noorudhin, A. Peck, J. Rohlf, C. Strohmman, P. Wittich, R. Zou on behalf of the CMS Collaboration

Abstract

The challenging conditions of the High-Luminosity LHC require tailored hardware designs for the trigger and data acquisition systems. The Apollo platform features a “Service Module” with a powerful system-on-module computer that provides standard ATCA communications and an application-specific “Command Module”s with large FPGAs and high speed optical fiber links. The CMS version of Apollo will be used for the track finder and the pixel readout. It features up to two large FPGAs and more than 100 optical links with speeds up to 25 Gb/s. We study carefully the design and performance of the board by using customized firmware to test power consumption, heat dissipation, and optical link integrity. This paper presents the results of these performance tests, design updates, and future plans.

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ABSTRACT: The challenging conditions of the High-Luminosity LHC require tailored hardware designs for the trigger and data acquisition systems. The Apollo platform features a “Service Module” with a powerful system-on-module computer that provides standard ATCA communications and an application-specific “Command Module”s with large FPGAs and high speed optical fiber links. The CMS version of Apollo will be used for the track finder and the pixel readout. It features up to two large FPGAs and more than 100 optical links with speeds up to 25 Gb/s. We study carefully the design and performance of the board by using customized firmware to test power consumption, heat dissipation, and optical link integrity. This paper presents the results of these performance tests, design updates, and future plans.

KEYWORDS: Data acquisition circuits, Digital electronic circuits, Digital signal processing, Detector control systems, Modular electronics, Trigger concepts and systems

¹speaker

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1 Introduction

High-performance ATCA blades are gaining popularity in high-energy physics experiments in view of the High-Luminosity LHC. The development for high-energy physics applications has proven to be challenging with many problems that need to be addressed (power, cooling, optical fiber management, communication interfaces, etc.). The Apollo platform aims to provide a simple hardware environment and firmware and software toolkit which can be used for the development of ATCA blades [1]. It consists of a common “Service Module” (SM) that handles standard ATCA communications as well as clock and power delivery, and an application-specific “Command Module” (CM) with large FPGAs and many optical links to accommodate demanding algorithms and large data flow.

The Apollo SM is a standard-sized ATCA blade with a 7 U×180 mm cutout to accommodate one full-sized or two half-sized CM boards. It features a Xilinx Zynq System-on-Module with embedded Linux OS for control, monitoring, and local DAQ functions, a CERN Intelligent Platform Management Controller (IPMC) [2] or OpenIPMC [3], and a Wisconsin Ethernet Switch Module [4]. Standard commercial power entry and conditioning modules are used to deliver 12 V_{DC} at up to 30 A to the CM.

2 Overview and CMS Applications

The CMS experiment plans to have major detector upgrades for the High-Luminosity LHC [5], including a new silicon tracker [6]. The Apollo platform will have two applications in the tracker back-end processing system: the Level-1 Track Finding (TF) system and the Inner Tracker Data Trigger and Control system (IT-DTC).

The Level-1 TF reconstructs tracks from the Outer Tracker and calculates track parameters for the Level-1 trigger system. The algorithm requires substantial FPGA resources, which may result

in a large power consumption. It is expected to require one or two Virtex Ultrascale+ FPGAs and 62 optical links at 25 Gb/s. A total of 162 Apollo blades are expected to be used for the TF.

The IT-DTC reads hits from the front-end ASIC chips and converts the data into a compact format. It also converts the trigger signal from the CMS trigger to tokens and transmits them back to the front-end. It is expected to require 72 optical links at 10 Gb/s and 16 optical links at 25 Gb/s. A total of 28 Apollo boards are expected to be used for the IT-DTC.

To satisfy the requirements of the two applications, the CMS design of the Apollo CM can accommodate one or two large Xilinx Ultrascale+ FPGAs with 4-channel bi-directional and 12-channel single-directional Firefly optical engines that sum up to more than 100 optical links with speed up to 25 Gb/s. Two revisions of the design are planned before the final production. The CMS Apollo revision 1 was produced by the end of 2019. The revision 2 design is currently being produced and evaluated. This paper describes the evaluation process, shares what we learned, and presents the final performance of the revision 1 design. It also describes major updates of the revision 2 design and preliminary results on link integrity.

3 Revision 1 Performance Tests

The CMS revision 1 Apollo blade, as shown in Fig. 1, has two large FPGAs (an XCKU15P (KU15P) in an A1760 package and an XCVU7P (VU7P) in a B2104 package) and sites for 4-channel and 12-channel Firefly optical transceivers with up to 124 optical links with speed up to 25 Gb/s. Thorough evaluation tests on all parts have been conducted. This section summarizes the testing procedure and the final results.

3.1 Link Integrity

Up to 19 Firefly optical engines (13 4-channel parts and 6 12-channel parts) can be mounted on the revision 1 blade. We test the entire data path (Multi-Gigabit Transceiver (MGT) inside FPGA $\xrightarrow{\text{electrical}}$ Firefly Transceiver $\xrightarrow{\text{optical}}$ Firefly Receiver $\xrightarrow{\text{electrical}}$ MGT) by using the PRBS-31 pattern built within the Xilinx FPGA. A bit error rate less than 10^{-16} is measured without any errors. Additional eye scans are conducted to check the receiver margins (Figure 2). Because the clock data recovery (CDR) circuit is activated on the Firefly engines, the eye diagrams only give information on the electrical path between the Firefly receiver and the MGT.

3.2 Power and Thermal Performance

To test the Apollo blade under realistic thermal and power constraints, we need to determine the optimal fan level. We use the 450/40 FC Series 14-slot ATCA shelf which has a SCHROFF shelf manager with Pigeon Point ShMM 700. When the fan level goes from 10 to 15, power consumption goes from 500 W to 2000 W and we observe that the FPGA is only a few degrees cooler. With the noise level also taken into consideration, we decided to set the maximum fan level to 10.

Special power inefficient firmware, the Look-Up Table (LUT) oscillator algorithm (developed by the authors of Ref. [7]), is used to make the FPGA draw a large amount of power. The amount of power the FPGA exerts can be adjusted dynamically. Customizations per vendor's recommendations are applied to the LGA80D power supplies to achieve high output power to the FPGAs.

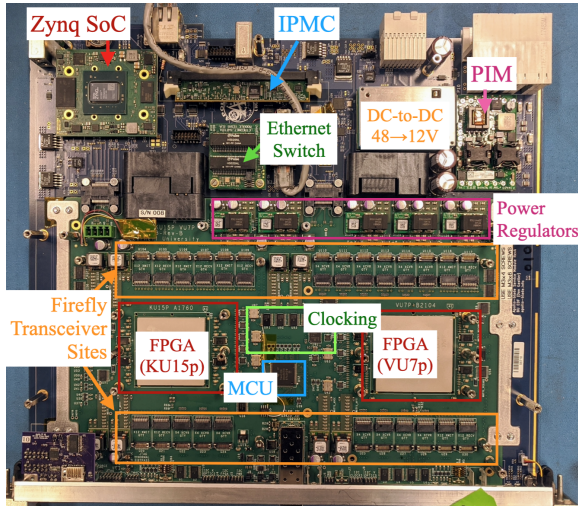


Figure 1. The Apollo revision 1 SM and CM with major components labelled and highlighted in boxes.

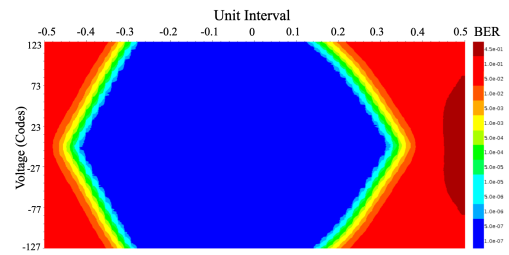


Figure 2. A typical eye pattern with a large opening at a data rate of 25 Gb/s with CDR on the revision 1 CM.

Since the VU7P heatsink is 20% bigger than the KU15P one, we expect the VU7P to have better thermal performance. However, when the FPGAs were first heated up, the VU7P was consistently warmer than the KU15P when drawing the same amount of power. Upon inspection, we found that the VU7P has a non-flat surface (0.1 mm higher in the center), which makes good thermal conduct between the FPGA surface and the heatsink challenging. A few thermal gels and putties are explored to gauge thermal conductivity and ease of application/removal. TG-PP-10 (10 W/(mK)) is found to be the easiest to use and has the best conductivity. The VU7P is 8 °C cooler at 70 W with the TG-PP-10 than with the thermal pad (TG-A6200).

Large temperature gradients across a single FPGA are observed in firmware designs with a concentrated number of LUT oscillators. The VU7P has two Super-Logic Regions (SLRs). Each SLR is a single FPGA die slice and has its own system monitor that can conduct an independent temperature measurement. With a concentrated number of LUT oscillators built on top of one of the two system monitors on the VU7P, a temperature difference of more than 40 °C is observed between the two system monitors. Further investigation suggests that large temperature gradients can also occur within a single SLR. Similar observations have been reported previously [7].

To avoid large temperature gradients, efforts are made to spread out the LUT oscillators evenly across the FPGA. The same number of LUT oscillators in each of the spread-out clusters are always enabled simultaneously during the test. The thermal gradients across the two SLRs of the VU7P are eliminated with the improved firmware design (Fig. 3).

At fan level 10, with the requirement that the FPGAs stay below 80 °C, the revision 1 blade can consume 256 W in total, with VU7P taking 140 W, KU15P taking 86 W and the SM and the rest of the CM components taking 30 W. Figure 3 shows the thermal behavior of both FPGAs. Due to the size of the heatsinks and the FPGA package, the KU15P has worse thermal performance than the VU7P. Consistent thermal performance is observed on three CM boards.

Because of the connection between the heatsinks, the KU15P is thermally impacted by the VU7P. When the temperature on the VU7P increases from 25 °C to 80 °C, the KU15P becomes

10 °C warmer. To get to 80 °C, the KU15P needs to consume 102 W when the VU7P is at 25 °C. It only needs to consume 86 W when the VU7P is at 80 °C. The VU7P, on the other hand, is not thermally impacted by the KU15P.

The results are similar to the power estimation conducted during the design phase of the revision 1 blade. Power loss due to large currents running across the CM plane is measured to be about 12 W at the maximum power.

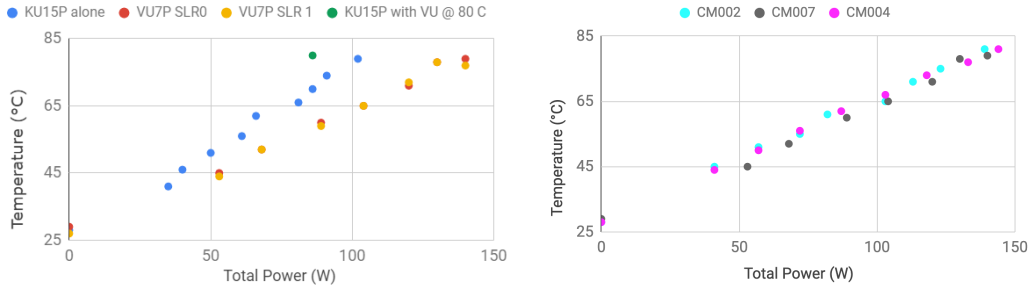


Figure 3. Temperature vs power performance of both FPGAs on one revision 1 CM (left) and the VU7Ps on three revision 1 CMs (right). Red and yellow dots are temperatures measured on the two SLRs of the VU7P. Blue dots represent the performance of the KU15P with the VU7P at 28 °C. The green dot shows the reduced performance of the KU15P when the VU7P is at 80 °C. Magenta, cyan and grey dots on the right demonstrate the consistent thermal performance of three VU7Ps on three boards.

4 Revision 2 and Future Plans

The major changes of the revision 2 CM design (Fig. 4) include updates to clock signal distributions, more powerful FPGAs (two A2577 sites), power and thermal improvements, more adaptations for the optical links, and switching to halogen-free material (EM-890). It has three 70 μm-thick copper planes to reduce power loss in the distribution (revision 1 has two thinner planes). Sites for 14 Firefly optical engines (six 4-channel parts and eight 12-channel parts) are provided with up to 104 optical links with speed up to 25 Gb/s. There are more links between the two FPGAs to provide the algorithms with options. The temperature sense diode outside the system monitors in each Xilinx FPGA is read out because of the temperature gradients observed in the revision 1 thermal tests.

The revision 2 CM is currently under evaluation. Preliminary studies show that a bit error rate smaller than 10^{-16} is achieved on the 4-channel Firefly optical engines at 25 Gb/s with large open eye diagrams (Fig. 5). Since the FPGA heatsinks are 3% larger than the VU7P heatsink in the revision 1 design and the FPGA package is larger, we anticipate each FPGA to be able to handle roughly 125–150 W. For the CMs with a single FPGA, a larger heatsink up to twice the current size can be designed.

Revision 2 of the SM is in production. Major design updates include an upgrade to Ultra-scale+ Zynq SoC, a switch to halogen-free material (TerraGreen), and changes to the clock signal distribution.

5 Summary

The Apollo ATCA blade will be used for the IT-DTC and the TF in the CMS experiment at the HL-LHC. Two revisions of the designs are planned before the final production. The revision 1

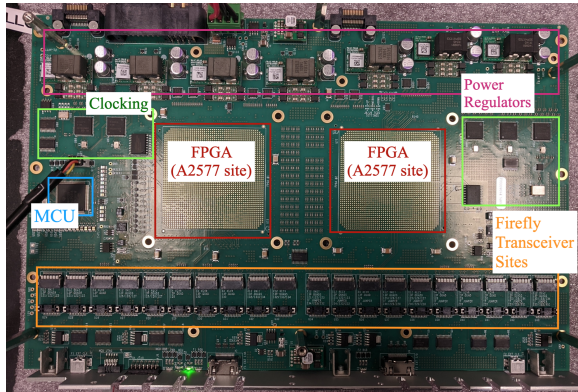


Figure 4. The Apollo revision 2 CM without any FPGAs. Major components are labelled and highlighted in boxes.

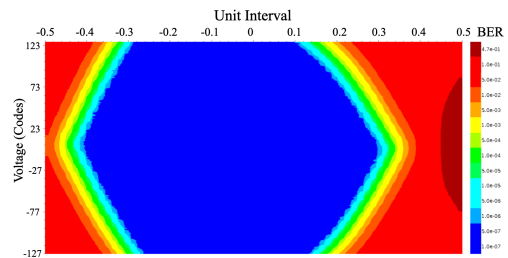


Figure 5. A typical eye pattern with a large opening at a data rate of 25 Gb/s with CDR on the revision 2 CM.

design of the Apollo blade has demonstrated great link integrity and thermal performance. The evaluation tests for the revision 2 design are ongoing. Preliminary link integrity results are shown.

Acknowledgments

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