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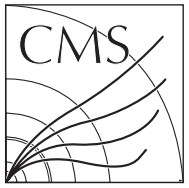

The Compact Muon Solenoid Experiment

Conference Report

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Development of a high bandwidth readout chain for the CMS Phase-2 pixel upgrade

Caleb James Smith for the CMS Tracker Collaboration

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Development of a high bandwidth readout chain for the CMS Phase-2 pixel upgrade

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Keywords: Front-end electronics for detector readout, optical detector readout concepts, radiation-hard electronics

Contents

1 Introduction

The High-Luminosity LHC (HL-LHC) [2] will provide CMS experiment [1] with a peak instantaneous luminosity of $7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$. Compared to the LHC, the HL-LHC will have up to 200 proton-proton collisions (pileup) per event and will result in a higher radiation fluence. To prepare for this data taking environment, the CMS Tracker will be fully replaced in the Phase-2 upgrade [3, 4].

The new inner tracker will have about two billion silicon pixels installed. The detector will be built using hybrid pixel modules that process sensor data using a custom readout chip initially developed by the RD53 collaboration [5]. Each readout chip on the detector needs a control link to receive trigger, clock, commands, and settings from off-detector electronics as well as data links to send pixel data to off-detector electronics. The high bandwidth control and data links are split into two stages: electrical links and optical links. System tests of electrical and optical links are presented.

2 Data Readout Chain

An overview of the data readout chain for the inner tracker is shown in Figure 1. High bandwidth electrical and optical links are used to establish control and data links between pixel modules on the CMS detector and Data Trigger Control (DTC) boards in the counting room. Low-mass electronic links (e-links) up to 1.6 meters long provide 160 Mbps control links (downlinks) and 1.28 Gbps data links (uplinks) between pixel modules and portcards. Optical fibers connect portcards, which are mounted on the support structure inside the detector, to DTC boards in the counting room to establish 2.5 Gbps control links (downlinks) and 10 Gbps data links (uplinks). The portcards each carry three Low-Power Gigabit Transceivers (lpGBT) [7] and three Versatile Link PLUS Transceiver (VTRx+) modules [6]. The lpGBTs convert optical signals to electrical signals (and vice versa), and the VTRx+ modules establish optical links with the DTC boards.

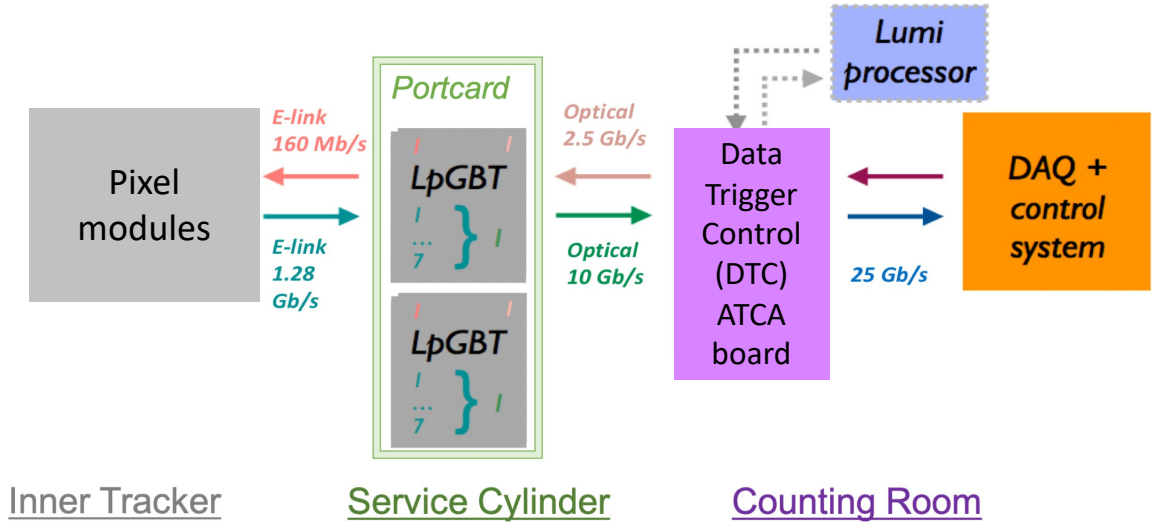

Figure 1. System readout architecture for the inner tracker [4]. Pixel modules communicate with portcards through e-links. Portcards communicate with Data Trigger Control (DTC) boards through optical links.

3 Electrical Links

The electrical links (e-links) are created using low mass, small diameter twisted pair cables. One end of a twisted pair electrical link is shown in Figure 2. E-link bundles are made to connect to modules and provide each module with one control link twisted pair and multiple data link twisted pairs. Each twisted pair is produced using two 36 American Wire Gauge (AWG) copper core (127 microns in diameter) wires surrounded by polyimide insulation (45 microns thick) that are twisted together with 4 twists per inch. The pairs are soldered to small, 20 micron thick PCBs that can plug into Molex connectors with 300 micron pitch [12–14]. To improve durability and handling, the soldered wires are secured with a non-conductive epoxy, and then the bundle is lashed together using polyimide braiding.

Figure 2. One end of a twisted pair electrical link (e-link).

The prototype low-mass electrical links are developed and characterized with a series of measurements. The signal quality is assessed using eye diagrams, which overlay transitions between binary states from repeated measurements of the signal over a time interval. The eye diagram amplitude and jitter are used to quantify the quality of the differential signal and identify any distortion. Bit error rate scans are used to characterize signal integrity across e-links. Cross talk

effects from channels within an e-link bundle (internal) and from multiple bundles (external) are studied.

Furthermore, in one system test of the e-links, an RD53 chip on a Single Chip Card (SCC) is read out over e-links using an FC7 mezzanine card [11], as shown in Figure 3. E-links of two gauges (34 and 36 AWG) and different lengths (from 0.35 to 2.0 meters) are used in the readout chain. Bit error rates are determined using a pseudorandom binary sequence (PRBS) that is sent from the RD53 chip to the FC7 mezzanine card. The amplitude of the PRBS signal is varied using the "TAP0" pre-emphasis digital-to-analog converter (DAC) setting, which ranges from 0 to 1000 and controls the amplitude of the signal output by the current mode logic (CML) driver on the RD53 chip. For this test, the amplitude is increased until the bit error rate of 10^{-11} is reached. Longer e-links require a larger signal amplitude to maintain a given bit error rate. Good performance is seen for e-links up to 2.0 meters.

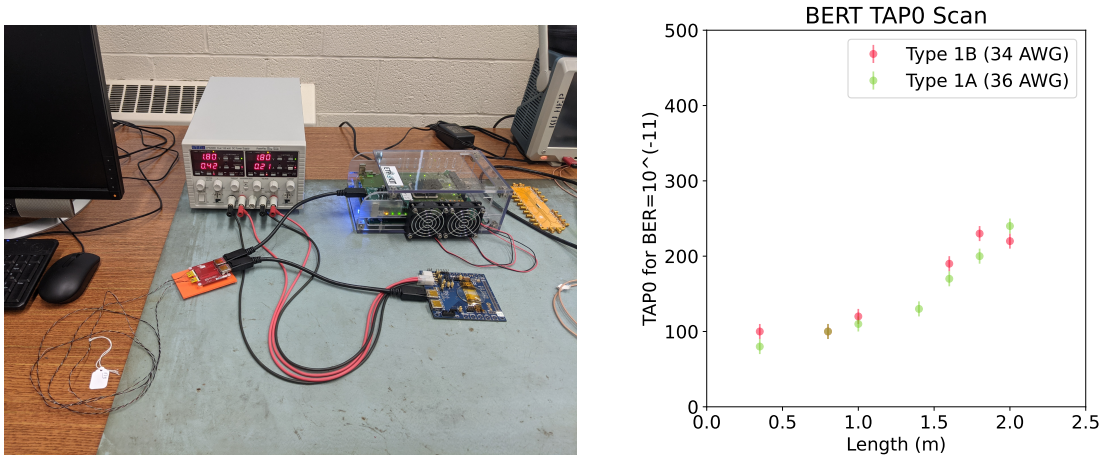

Figure 3. Measurement of signal amplitude (set by TAP0) for electrical links as a function of e-link length for 34 and 36 AWG e-links. In the hardware setup (left), an FC7 mezzanine card is connected to an SCC through two commercial display port cables, an adapter board, and an e-link for control and readout of an RD53 chip. The measurements (right) show the TAP0 setting to achieve a bit error rate of 10^{-11} for e-links of different lengths and gauges.

An external crosstalk measurement was performed, and the results are shown in Figure 4. To mitigate the effect of external crosstalk from a large aggressor amplitude, the victim amplitude set by TAP0 only requires a small increase. Thus, external crosstalk from the single aggressor e-link has a small effect on readout over the victim e-link.

Radiation testing was performed to determine if e-links can maintain performance after receiving up to 1500 Mrad, which surpasses the total dose expected during their use in CMS. Two different epoxies, Araldite 2011 (Ref. [9]) and UR6060 (Ref. [10]), were used for e-links that underwent radiation testing. For doses up to 1300 Mrad, the Araldite 2011 epoxy showed significant darkening, while the UR6060 epoxy remained clear and transparent. The signal integrity on e-links remained good after radiation doses, and UR6060 is chosen as the epoxy used for e-link production. The polyimide braiding used for lashing becomes brittle after 1900 Mrad, but this should not effect the electrical readout.

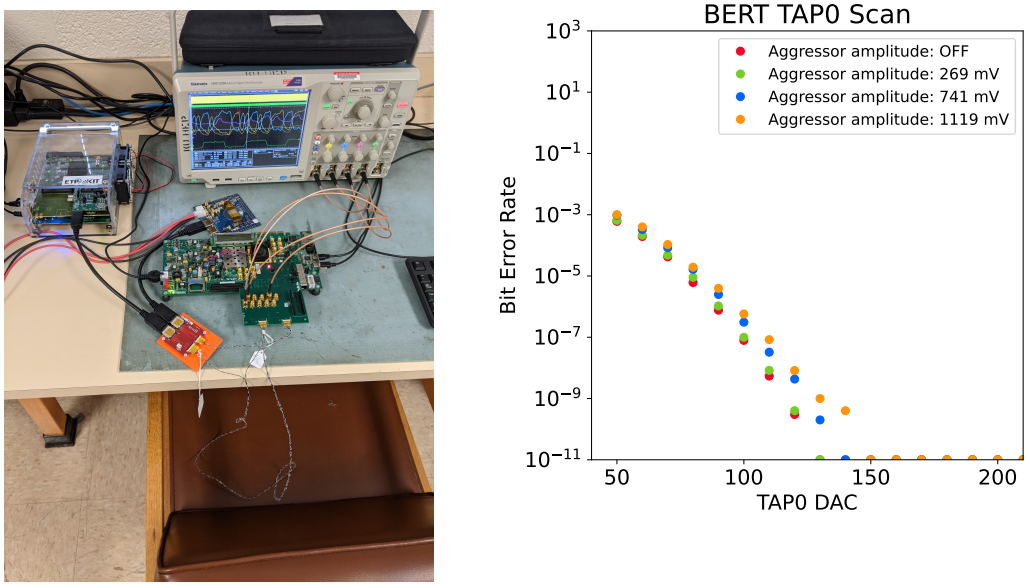

Figure 4. Measurement of the effect of external crosstalk on data transmission. Two e-links (1.4 meters, 36 AWG) are twisted together (left), with a victim e-link connected between an FC7 mezzanine card and SCC to read from an RD53 chip, and an aggressor e-link connected to a KC705. The KC705 sends PRBS signals on four e-link channels on the aggressor at different amplitudes.

4 Portcards with Optical Links

The portcards play an important role in the readout chain in converting electrical signals from on-detector readout chips to optical signals for off-detector DTC boards. The portcard design and a photo of a prototype portcard are shown in Figure 5. Dedicated setups with the portcards reading out SCCs with short coaxial cables have been used to test the prototype portcard and validate the optical part of the readout chain.

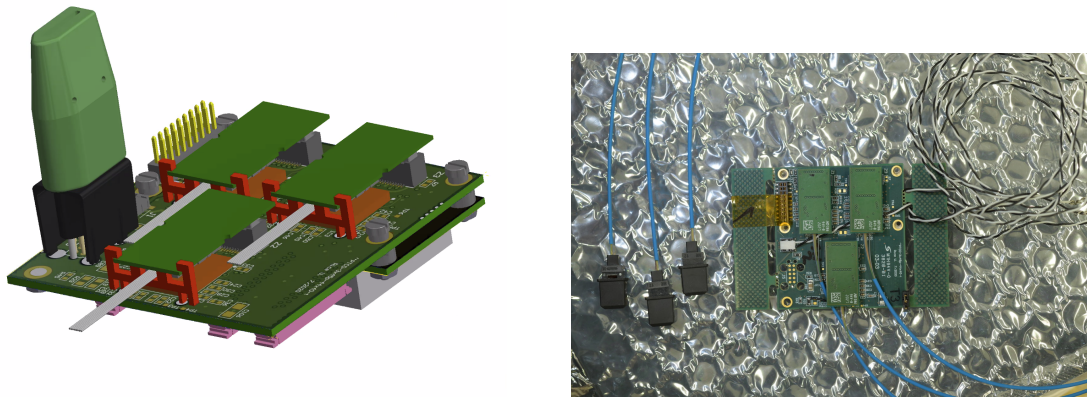

Figure 5. Portcard design (left) and prototype (right). The portcard has three lpGBT and three VTRx+modules, which are used to convert high bandwidth electric signals to optical signals.

The optical links have been characterized by various measurements. In one measurement, the high-speed input to the lpGBT is compared to a 5-bit adjustable constant voltage by a comparator

sampled with a phase interpolated clock. Transitions of the comparator are counted; within the eye the output should toggle, but above or below the eye, no transitions are expected. The data from this measurement are shown in Figure 6. The high toggle count region is large, corresponding to a large eye diagram and a strong optical signal.

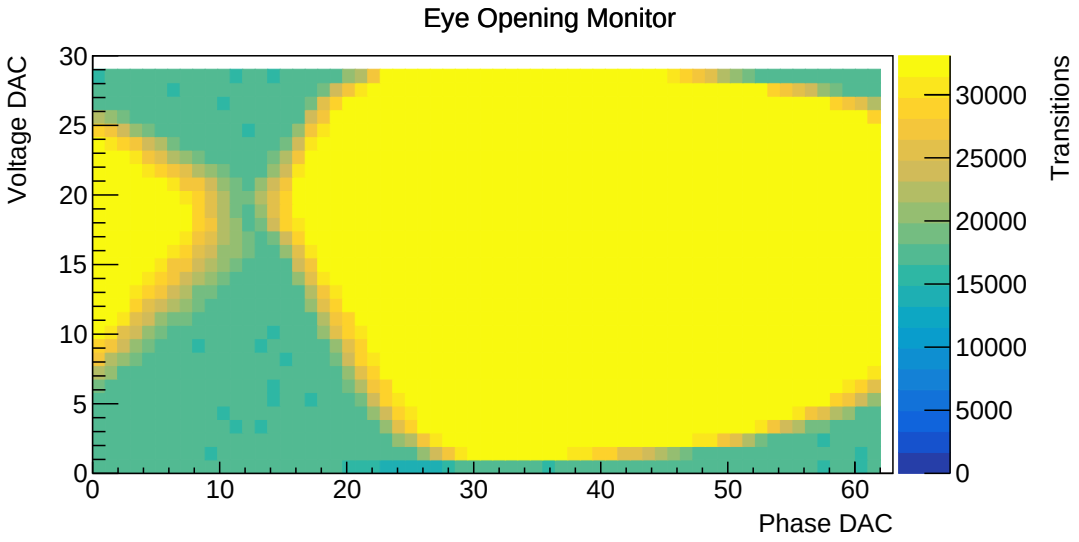

Figure 6. Eye opening monitor from an lpGBT for the 2.56 Gbps optical down link with equalization parameters at default settings. The vertical axis is a 5-bit encoded digital-to-analog converter (DAC) value that corresponds to the constant voltage that the high-speed signal is compared with. The horizontal axis is a 6-bit encoded DAC value that governs the sampling phase used for this comparison. The color scale shows the number of transitions, which is the toggle count. Regions with high toggle count correspond to the eye opening, while regions with low toggle count are outside the eye opening.

The electrical link receivers on the lpGBT are being studied. In one measurement, the signal source is a PRBS7 generator in the RD53 readout chip. This signal is sent over a commercial display port cable, an adapter board, and a Molex FPC cable (Ref. [15]) to be received by an lpGBT. The signal is compared to an internal error checker on the lpGBT. The bit-error rate is measured as a function of clock sampling phase and equalization setting, and the results are provided in Figure 7. The region with a bit error rate of $9.3 * 10^{-10}$ corresponds to zero errors for the total number of bits checked. The phases with zero errors are those where the eye diagram is open. The equalizer on the lpGBT reduces jitter and the bit error rate by processing the high-speed signal to minimize Inter-Symbol-Interferance [8]. Changing the equalization setting has only a small effect on the timing. Low error rates on the lpGBT electrical link receivers are achieved by tuning the sampling phase.

5 Conclusion

The data readout chain is an important part of the CMS Phase-2 pixel upgrade. Various system tests have been performed to characterize the electrical and optical links forming the readout chain. Electrical links can provide stable connectivity at the required lengths, and crosstalk has a small

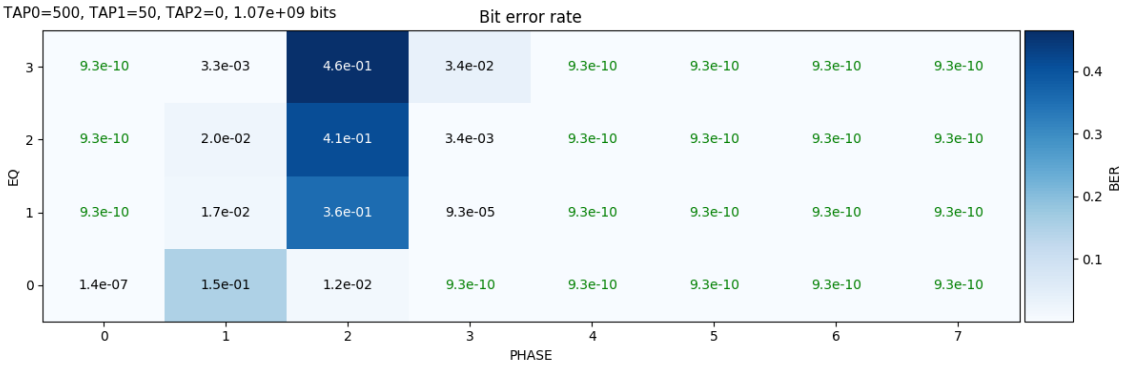

Figure 7. Scan of bit-error rate vs. clock sampling phase and equalization setting for electrical port receivers on the lpGBT driven by the RD53 pixel readout chip. The number of bits checked at each setting is $1.07 * 10^9$. Points in green have zero observed errors and report the reciprocal of the number of bits checked.

effect on signal quality. Conversion from electrical to optical links is working well, and the optical links have good performance. These results form an important input to the final design, production, and testing of components for the pixel detector readout chain.

Acknowledgments

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