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HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter

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Abstract

For the CMS High Granularity Calorimeter (CE), the final version of the 72-channel front-end ASIC (HGCROC3) was submitted in December 2020. HGCROC3 includes low-noise/high-gain preamplifiers/shapers and a 10-bit 40 MHz successive approximation ADC (SAR-ADC) that provide the charge measurement over the linear range of the preamplifier. In the saturation range, a discriminator and a time-to-digital converter (TDC) provide the charge information from the time over threshold (ToT; 200 ns dynamic range, 50 ps binning). A fast discriminator and another TDC provide timing information to 25 ps accuracy. The chip embeds all necessary ancillary services: bandgap circuit, PLL, threshold DACs. We present the experimental results on the latest and final version (HGCROC3) received in April 2021.

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HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter

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ABSTRACT: For the CMS High Granularity Calorimeter (CE), the final version of the 72-channel front-end ASIC (HGCROC3) was submitted in December 2020. HGCROC3 includes low-noise/high-gain preamplifiers/shapers and a 10-bit 40 MHz successive approximation ADC (SAR-ADC) that provide the charge measurement over the linear range of the preamplifier. In the saturation range, a discriminator and a time-to-digital converter (TDC) provide the charge information from the time over threshold (ToT; 200 ns dynamic range, 50 ps binning). A fast discriminator and another TDC provide timing information to 25 ps accuracy. The chip embeds all necessary ancillary services: bandgap circuit, PLL, threshold DACs. We present the experimental results on the latest and final version (HGCROC3) received in April 2021.

KEYWORDS: ASIC; CMS; HGCAL; HGCROC.

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Contents

1. CMS CE requirements

The High Granularity Calorimeter (CE) [1], currently being designed by the Compact Muon Solenoid collaboration (CMS), will replace the existing endcap calorimeters [2] for the High Luminosity phase of the LHC (HL-LHC). The full system will be maintained at -30°C with two types of active elements implemented: 640 m² of silicon sensors within the full electromagnetic calorimeter (CE-E) and in the higher intensity region of the hadronic calorimeter (CE-H), and 370 m² of silicon photomultipliers (SiPMs) for the lower intensity region of the hadronic calorimeter.

Silicon sensors will have three different active thicknesses (300, 200 and 120 μm) in order to optimise the charge collection: each sensor has either 192 or 432 individual diodes, which act as sensor cells. The hadronic calorimeter will use scintillator as the active material in regions where the integrated dose is low enough for the scintillator to retain an adequate light yield over the whole life of the HL-LHC.

Thus, two versions of the chip are required to read out these two types of sensors (silicon and SiPM). They have to provide a charge measurement up to 10 pC for the silicon version and 300 pC for the SiPM version, with a noise level below 0.4 fC (2500 electrons). In order to avoid summing charges from particles produced in different HL-LHC bunches, they have to achieve a fast shaping time, and have less than 20 % of the signal in the next bunch crossing. Furthermore, a high precision timing capability is required (around 100 ps resolution at 10 fC and less than 25 ps above 100 fC).

2. HGCROC3

HGCROC3 is the final version of the ASIC designed to read out the silicon modules of the future CMS CE. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on the detector, the front end ASICs are very challenging and innovative. The HGCROC chip measures and digitises the charge deposited in the silicon sensor pads, provides a high precision measurement of the Time-of-Arrival (ToA) and transmits these data to the back end electronics. It also computes, every bunch crossing, digital sums of neighbouring channels which contribute to build trigger primitives. The requirements for the front end electronics are extremely challenging, including dynamic range over 16 bits equivalent (0-10 pC), noise below 2500 electrons, high-precision timing information (25 ps), in order to avoid summing

charges from particles produced in different hard interactions, and low power consumption (below 15 mW/channel). The front end electronics will face a harsh radiation environment: 200 Mrad and 1×10^{16} neq/cm², where 1 neq represents the non-ionizing damage done by one 1-MeV neutron, by the end of HL-LHC operations. The ASIC includes a fully triplicated control logic to prevent Single Event Effect (SEE) and in the data path, a single error correction/double error detection (SECDED) Hamming algorithm is applied in each buffering element. The final HGCROC3 ASIC was submitted (TSMC 130 nm node) in December 2020 and the first lab tests have started in July 2021. This paper will describe the first measurements and compare them to the previous ASIC iteration (HGCROC2).

2.1 Architecture

HGCROC3 embeds 72 regular channels of the full analog chain in order to perform charge and time measurements, 2 calibration channels connected to smaller cells for calibration with minimum-ionising particles (MIPs) and 4 common mode channels for the common noise subtraction (see figure 1).
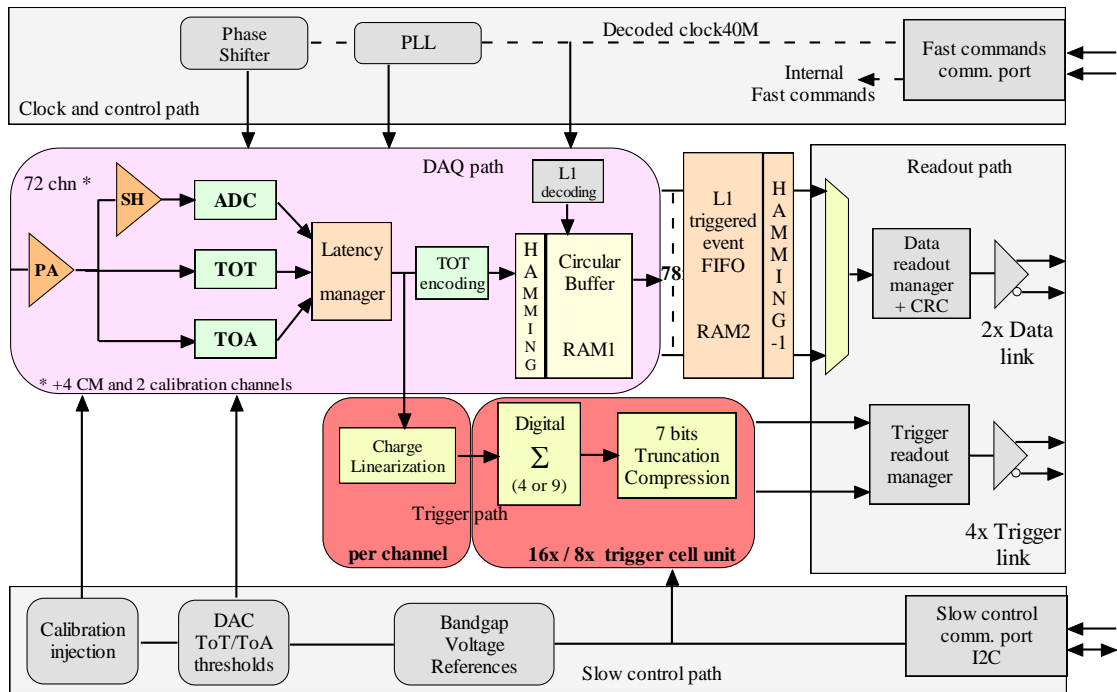

Figure 1. HGCROC3 block diagram with 72 regular channels divided in two paths: data acquisition with memorisation (DAQ) and trigger path.

Each channel is made of a low-noise preamplifier with a tuneable gain to adjust the MIP around 10 ADC counts. In the preamplifier's linear regime, the signal goes to a 10-bit SAR-ADC [3] through the shaper which optimises the signal-to-noise ratio. After the preamplifier saturation, the charge is provided by a discriminator associated to a 12-bit TDC which measures the Time-over-Threshold (ToT) with a 50 ps binning up to 200 ns. Another fast discriminator associated to a 10-bit TDC provides the Time-of-Arrival (ToA) with a 25 ps binning. The chip computes digitised data (ADC, ToT and ToA) every bunch crossing: those data are stored in a 512-depth circular buffer and then readout through two 1.28 Gbps links if a trigger arrives.

As the ASIC contributes to the first level trigger primitives of CMS, it has to provide a compressed view of all events every bunch crossing. This is achieved by summing the charge from adjacent channels (4 or 9) and then by reading them out through four 1.28 Gbps links devoted to trigger data.

An I2C slave interface is used to modify all the static parameters of the chip: the controller and the parameters are triplicated to prevent SEE. The chip is dynamically controlled by the Fast Command block which receives the master clock (320 MHz) and command requests. During operating conditions, they enable the initiation of system-level actions: link synchronisation, calibration or trigger request. After an internal division by 8 of the master clock, the internal PLL generates the others clocks needed to operate the chip: 40 (state machine and ADC), 160 (TDC) and 640 MHz (serialisers).

2.2 Charge measurements

Due to the large dynamic range (up to 10 pC), the charge measurement is divided in two ranges for each channel. The low-end one corresponds to the linear part of the preamplifier with a 10-bit ADC digitisation. In the high-end part, the preamplifier is saturated and the ToT is enabled and converted with a 12-bit TDC (50 ps LSB).

Regarding the ADC, figure 2 highlights its linearity as a function of the injected charge with a 47 pF equivalent detector capacitance. The Integral Non Linearity (INL) plot shows a linearity within 0.5% of the full dynamic range with a 1.6 ADC unit resolution (~0.3 fC): the timing measurement triggering causes the small jump around 15 fC (ToA threshold).

Despite the fact that the ASIC digital activity was doubled due to Triple Modular Redundancy (TMR), the noise results are comparable to the previous submission of the ASIC. The linearity has been slightly improved from 1% to 0.5%.
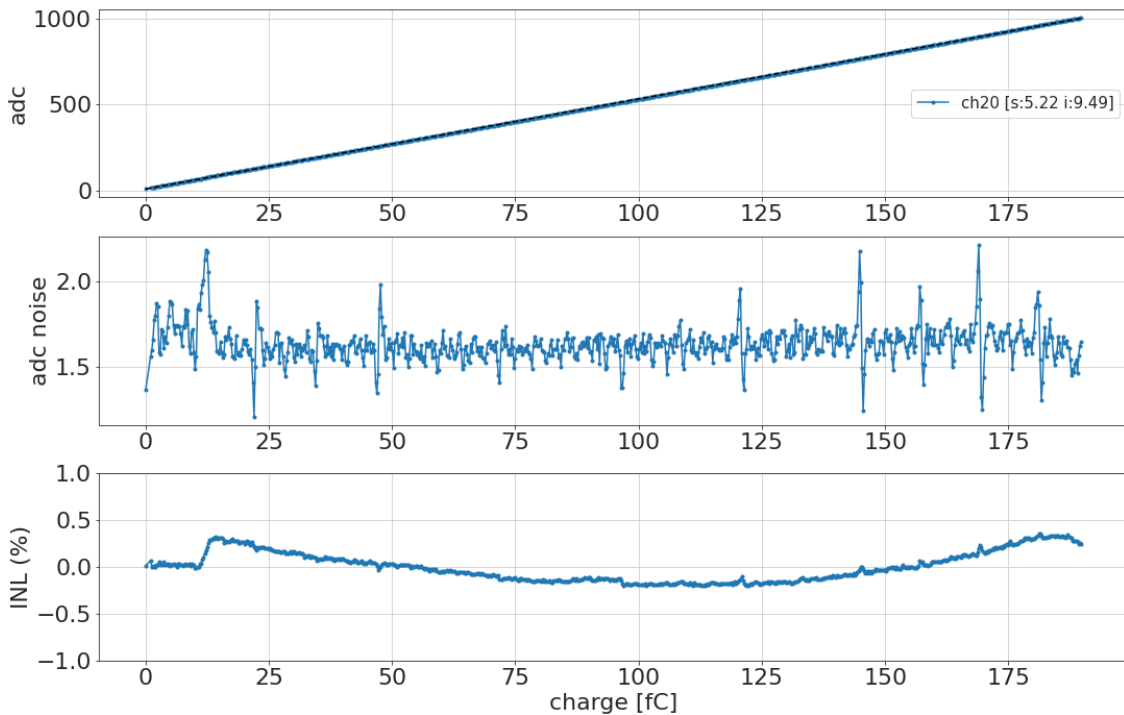

Figure 2. ADC characterisation. Top: charge conversion in ADC units versus injected charge. Middle: noise in ADC units for each charge. Bottom: integral non linearity (INL).

When the preamplifier saturates, its output acts like a Time-over-Threshold (ToT): the signal width gives an estimate of the injected charge. The 12-bit TDC (50 ps binning) is in charge of the digitisation of the pulse width up to 200 ns (which corresponds to 10 pC). Figure 3 exhibits its linearity as a function of the charge: the INL remains within 0.5 % over the full range. Some residual wiggles are visible on the plot of INL vs. injected charge which are due to digital clock coupling on the channel inputs passing through the PCB ground.
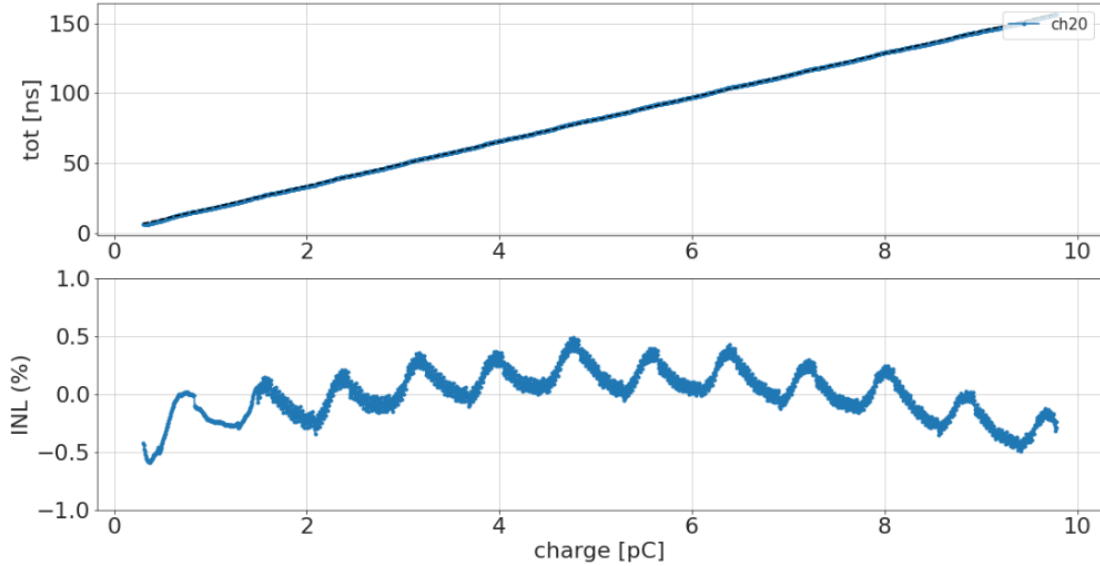

Figure 3. TOT characterisation. Top: ToT pulse width versus injected charge in pC. Bottom: integral non linearity (INL).

2.3 Timing performances

The timing measurement of the ASIC is performed by a 10-bit TDC with a 25 ps LSB. The triggering threshold is set by an internal DAC directly connected to a fast discriminator. The measurements were done with a 47 pF capacitor to mimic the detector capacitance.

On figure 4, the ToA threshold was set to 15 fC and the measured jitter noise floor is around 13 ps (25 ps required): this major improvement was achieved thanks to a new TDC layout and an optimised reconstruction of the digitised value.

The CE timewalk correction will be performed offline. Therefore, a stable and reproducible measurement will be needed. At the minimum threshold (15 fC), the timewalk is below 2.5 ns and the jitter around 120 ps. These results meet the requirements for discrimination of energy deposits among many hard interactions, whether in the same or in neighboring HL-LHC bunch crossings.
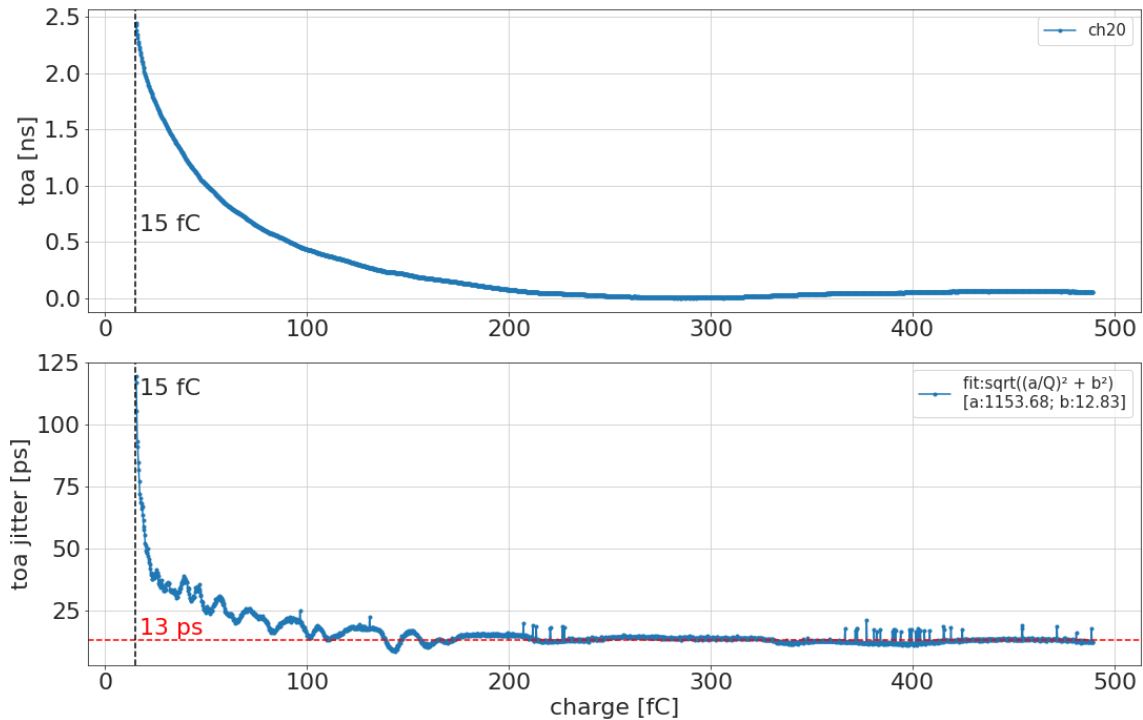
Figure 4. Timing performance. Top: timewalk profile up to 500 fC. Bottom: jitter as a function of the injected charge.

3. Summary

The HGCROC2 chip has been intensively tested over 18 months and all the measurements are now well understood. It is an extremely complex ASIC designed for imaging calorimetry: low noise, high dynamic range, precision timing measurements, high speed links, and a large digital activity in a severe radiation environment.

Its charge performance reaches the specification: 1-2 % linearity, for both the ADC and the ToT with a noise below the requirements (0.4 fC). The timing measurements show a very low 25 ps jitter and the time walk correction is possible by setting the threshold at 20 fC. Some channels output a higher jitter due to problems in the timing reconstruction for a specific foundry corner. This issue has been understood and corrected in HGCROC3.

The final version of the chip (HGCROC3) has been received packaged in July 2021. The main modifications were located in the digital part with a fully radiation tolerant design and the addition of a second stage of memorisation. Only minor changes were implemented in the mixed signal part, except for the ToA TDC, which was corrected. Compared to HGCROC2, it shows the same noise performance (0.3 fC) and an improved linearity (within 0.5%) for the charge measurements. The time measurement jitter has been also improved by a factor of 2 (below 13 ps). The minimum threshold for the time measurement was reduced to 15 fC compared to the previous submission.

The first measurements of the final ASIC are promising: the performance is the same or better even though the digital activity was doubled due to the triplication of the digital part. An SEE campaign is foreseen in the beginning of 2022 to validate the robustness to TID and SEE.

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