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Radiation Damage Studies of Field Plate and p-Stop n-Side Silicon Microstrip Detectors

The RD20 Collaboration

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Abstract

We present results from studies of the properties of dedicated n-side microstrip structures before and after irradiation, with photons to 7 Mrad and fast neutrons to 8×10^{13} n.cm^{-2}. Both p-stop and field plate devices were investigated, each having a range of strip geometries in order to determine optimal configurations for long-term viability and performance.

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1 Introduction

The LHC environment [1,2] raises strong challenges for any detector technology operated close to the interaction region as part of an inner tracking system. We have previously addressed many of the issues concerning single-sided microstrip detectors [3] and, in conjunction with similar work from other groups on both generic silicon detectors [4, 5] and microstrip detectors [6], we have shown that single-sided microstrip detectors will survive a realistic 10 year scenario of LHC operation without significant degradation in performance. One extra requirement has been identified by all groups, namely that the detectors must be kept at a reduced temperature, around 0°C, in order to control the changes in depletion voltage caused by the high levels of radiation damage.

Double-sided microstrip detectors provide the possibility of a second co-ordinate with a minimum of extra material, an important consideration for any LHC tracking system. These are, however, considerably more complex devices both because of the added technical difficulties of double-sided processing and because of the need for extra structures to achieve strip isolation on the ohmic side (the n-side). The maintenance of good isolation under high levels of irradiation will be addressed, together with the quantification of any penalties in higher load capacitance due to the extra structures.

2 N-side isolation techniques

For any oxide-passivated silicon detector, the net positive charge present in the oxide after processing drives the surface into strong accumulation. For n^+ strips on an n^- substrate, figure 1(a), this accumulation layer represents a conductive path which leads to unacceptably low resistance between strips. In order to achieve good strip isolation, it is necessary to interrupt the accumulation layer and create a potential barrier between the strips. There are two main isolation techniques:

a) Field plate isolation [7]

Field plate isolation does not require an extra implantation step on the n-side, but instead uses the MOS field effect combined with integrated AC-coupling, figure 1(b). The readout metallisation is extended to overlap the n^+ strip, which enables the accumulation layer to be interrupted by biasing the metal more negatively than the strip itself and thus inducing an inversion layer of holes at the surface beneath the metal (typically the readout metal would be held close to ground by the readout amplifier, while the n^+ strips would be biased positively in the usual manner).

b) P-stop isolation [8]

Figure 1(c) shows the cross-section through the n-side surface of a microstrip detector, where the accumulation layer is physically interrupted with an extra p^+ region, called a p-stop, placed between each n^+ strip. Once the substrate is fully-depleted, there is no conductive path between the n^+ strips so long as the doping of the p-stop is high enough to counteract the field due to the oxide charge. In addition, the reach-through effect from the opposite p-side of the detector causes the p-stop to float at a potential offset from that of the n^+ strips, thereby increasing the electric field at the surface and contributing to the depletion of the surface region.

3 The N-side test structures

The majority of the results to be presented come from a set of dedicated n-side test structures produced at SINTEF (formerly the Senter for Industriforskning, or SI), Oslo, Norway. These included both field plate and p-stop devices on the same wafer, with a complementary range of geometries to provide direct comparison of the two isolation techniques and to allow optimisation of performance for each one. In addition, the p-stop doping was varied to allow this important additional parameter to be investigated. The corresponding p-side for the n-side test structures was kept simple, with no strips, in order to avoid any possible complications arising from the choice of p-side geometry.

a) Design

Devices with both 50μm and 100μm pitch were produced in order to investigate a range of position resolution and performance options. One detector unit was designed for each isolation technique and for each pitch, with each unit divided into eight sub-units containing four different geometries in AC-coupled, polysilicon-biased form (20 strips for 50μm pitch, 10 strips for 100μm pitch) and four matching geometries in DC-coupled form (7 strips for 50μm pitch, 5 strips for 100μm pitch). A full description of the devices can be found in [9].

Important features of the processing were the use of silicon nitride and two metal layers. An additional 100nm layer of silicon nitride on top of the oxide was used for improving the yield and quality of the coupling capacitors. The double-metal process, necessary for the field plate structures, used 2μm of polyimide to separate the two metal layers. Both nitride and polyimide layers covered the entire surface on the n-side of all the devices.

i) Field plate test structures

Table 1 shows the four geometries investigated for the 50μm pitch field plate devices. The narrow pitch combined with the requirement that the readout metal extends beyond (overlaps) the n^+ leaves little scope for strip width variation and therefore the parameter chosen for investigation was the field plate overlap. There were three geometries with 5μm strip width, with varying amounts of field plate overlap, and one geometry with 10μm strip width which would provide a higher coupling capacitance if this was found to be necessary. An example of the mask layout for one of the 50μm pitch field plate devices is shown in figure 2(a). The 6μm overlap (all dimensions are nominal) was known to be satisfactory for normal production tolerances, with the larger overlaps being considered for improved radiation resistance. Each wafer contained two units, one with 4cm and one with 2cm strip lengths.

Table 2 shows the four geometries chosen for the 100μm pitch field plate devices, where the parameter varied was the strip width. The field plate overlap was fixed at a value slightly more generous than the minimum value in order to allow a greater margin of safety for good isolation after irradiation. This extra width is small in comparison to the pitch and therefore the capacitance should not be significantly affected. Each wafer contained units with 4cm and 2cm strip lengths.

ii) P-stop test structures

Two configurations were chosen for investigation: common p-stops and individual p-stops. Typically, the biasing of p-stop strips has been implemented using accumulation layer biasing, which was expected to be very sensitive to radiation [10]. The use of integrated polysilicon bias resistors avoids this potential problem, and allows new possibilities for the p-stop geometry.

Common p-stop devices, an example of which is shown in figure 2(b), have all the p-stops between the strips connected together beyond the n^+ strip ends, with the biasing connection brought out over the p-stop using either polysilicon or metal. This configuration has the advantage of being compact and simple, with no possible surface conduction channels. However, there are also potential disadvantages of the common p-stop approach due to the fact that there is now a single, electrically-floating, conductor around the entire detector. This could affect both signals and strip capacitance. In addition, any significant resistivity variations across a detector could lead to incompatible reach-through potentials at different points leading to

high currents or full breakdown. Although this is true in any case for the direction parallel to the strips, there is now the added dimension orthogonal to the strips.

Individual p-stop devices, as shown in figure 2(c), are an established design, with physically separate p-stops between the n^+ strips. This results in a surface accumulation layer channel between the end of each strip and the guard ring, the conductivity of which can be used to provide a biasing resistance between the guard ring and the strips. However, for a high radiation environment, polysilicon resistor biasing was considered necessary. The surface channels between the p-stops were therefore designed to be long and narrow, with the intention of ensuring that their resistance should always be substantially larger than that of the polysilicon resistors. Table 3 shows the four geometries selected for the 50μm pitch p-stop devices, where the parameter varied is the gap between the n^+ and the p^+. For a fixed pitch, this can affect the p-stop voltage, the strip capacitance, and possibly breakdown between the n^+ and p^+ caused by the p-stop voltage. Each wafer contained 4cm and 2cm units with common p-stops and a single 2cm unit with individual p-stops.

Table 4 shows the four geometries for the 100μm pitch p-stop devices. As for the 100μm field plate strips, the main parameter varied is the n^+ strip width with the p^+/n^+ gap being kept constant at a nominal 15μm. Again, each wafer contained 4cm and 2cm common p-stop strip units and a single 2cm individual p-stop strip unit.

b) Fabrication

The process is an adaptation of SINTEF's process for double sided AC-coupled silicon microstrip detectors with field plate separation and double metal readout on the n-side [8, 11-14]. It has n-type strips on the back side deposited from a phosphine (PH_3) gas source. The front side strips and the p-stops on the n-side are ion implanted. A uniform layer of approximately 100nm Low Pressure Chemical Vapour Deposited (LPCVD) silicon nitride is used as extra passivation on top of the oxide and is also an integral part of the coupling capacitors. The presence of the nitride should improve stability towards environmental changes, and the diffusivity of alkali ions (fast diffusers in silicon dioxide) in nitride is very low. Boron implanted LPCVD polysilicon was used for biasing on the n-side.

The n-type wafers were delivered by Wacker Chemitronic GmbH and have a resistivity between 3000Ωcm and 5000Ωcm; they are polished on both sides with (111) orientation. The thickness is 280μm. A 600nm field oxide was grown with a combination of TCA, or 111-Trichloroethane, and wet oxidation. The n-type strips on

the back side were defined in this oxide through photolithography and wet etching in buffered hydrofluoric acid while the front side was protected with positive photoresist. The oxide on the front side serves as a mask for the phosphine gas while depositing phosphorous on the back side at 1000°C. A thick oxide was grown over the phosphorous doped layer after removal of the phosphorus glass with hydrofluoric acid. This oxide is used to mask against the boron implantation of the p-stops.

The patterns for the p^+ areas on the front side and the p-stops on the back side were defined by two independent photolithography and etching steps. The p^+ areas on the front side were ion-implanted with boron at 40keV and 5×10^{15} atoms/cm^2. Three boron doses were ion-implanted for the p-stops on the back side. An energy of 30keV and doses of 1×10^{11} cm^{-2}, 9×10^{11} cm^{-2}, and 5×10^{13} cm^{-2} were used for the p-stops. The implant doses and results from process simulation are compared to measurements in Table 5. It was not possible to measure the sheet resistance for the two lowest implant doses. The implant damage on the front and back side was annealed out at 800°C before the final coupling oxide on the p-side was grown at 1000°C with a combination of TCA and wet oxidation. This results in about 200nm of coupling oxide on the n-side and 150nm on the p-side.

100nm of LPCVD silicon nitride was then deposited on the wafer at 790°C. Contact holes to the strips were opened on both front and back sides of the wafer, with the mask on the n-side including openings to the p-stops for measurement of the p-stop voltage via probe pads. The pattern was defined with lithography and the nitride was etched in a Reactive Ion Etching (RIE) system. About 0.5μm of LPCVD polysilicon was deposited for the integrated resistors. A thin passivation oxide, 70nm thick, was grown over the polysilicon before ion implantation of boron. The implantation energy was 60keV and a dose of 3.9×10^{14} cm^{-2} was selected to achieve a sheet resistance of 3.3kΩ/square. Photolithography and etching of the passivation oxide defined the polysilicon pattern in the masking oxide before etching of the polysilicon. All the polysilicon on the front side was removed at the same time. Finally, the passivation oxide was stripped away in hydrofluoric acid and the ion implant annealed at 900°C for 30 minutes in nitrogen. A new passivation oxide was grown over the polysilicon resistors in a final high temperature TCA oxidation at 1000°C without removing the wafers from the furnace.

Contact holes in the polysilicon oxide were opened with photolithography and etching in buffered hydrofluoric acid, the reverse side being protected with

photoresist. About 1μm of aluminium was deposited on both sides of the wafers by sputtering and the metal was patterned before alloying in forming gas (10% H_2 in 90% N_2) at 450°C for 15 minutes. Polyimide was deposited on the n-side, exposed with a mask and developed. The polyimide was cured in a vacuum oven before the second layer of aluminium was deposited on the n-side. A short sputter etch was made before the aluminium sputtering, which improves the contacts between metal 1 and metal 2. A final lithography and etching step defined the second metal pattern.

4 Field plate results

a) Field plate strip isolation

Field plate detectors make use of the MOS effect and are therefore dependent on the flat band voltage remaining low enough such that surface inversion is achieved at a voltage below the required bias voltage. The main effect of ionisation damage on the surface oxide/silicon interface of silicon detectors is to increase the oxide charge and density of surface states, and therefore to increase the magnitude of the flat band voltage. The level of flat band shift is very dependent on the field across the oxide during irradiation and, as in the case of FOXFET devices, it would be expected that for the field plate configuration the flat band voltage would increase under irradiation to be comparable to the voltage across the oxide [15]. This would lead to reduced isolation resistance since the surface could not be forced into inversion, and therefore this could make the field plates inoperable. However, as we have already seen in studies on p-side devices with an additional nitride layer [3], the saturation value of the flat band voltage can be reduced by the presence of the nitride.

Before irradiation the interstrip resistance[1], measured with the full bias voltage also held across the field plates, is very high for all three overlaps and shows no obvious overlap dependence. Figure 3 shows the minimum operational voltage[2] for a 50μm pitch field plate device irradiated with ^{60}Co photons with full operating bias of 100V across both the detector and the n-side coupling capacitors. Before irradiation, the minimum operational voltage is determined by the depletion voltage of the detector (~ 50V) since the flat band voltage is only 10-15V. During irradiation, the flat band voltage increases rapidly at first and so the operational voltage is also seen to increase as the flat band voltage quickly becomes greater than the depletion voltage. The changes are essentially saturated beyond a dose of about 1Mrad, and for all three overlaps it is seen that the detectors remain operational at 100V. However,

there is now a significant overlap dependence with the largest overlap showing the lowest increase in operational voltage, which would indicate that for the smaller overlaps there is a significant contribution from edge effects.

Figure 4 shows that the interstrip resistance, measured at 100V, remains good up to a dose of at least 7Mrad. Previous results have already shown that field plate isolation remains satisfactory after high bulk damage from neutron irradiation [16], and therefore we conclude that good interstrip isolation is maintainable for these devices in high radiation environments.

b) Field plate strip capacitance

Figure 5 shows the unirradiated field plate strip capacitance[3] at 100V, measured at both 100kHz and 1MHz for (a) 50μm pitch, and (b) 100μm pitch field plate strips. The interstrip capacitance[4] has a clear frequency dependence with the values at 1MHz being consistently lower than at 100kHz. The backplane capacitance is the same at both frequencies, and is essentially independent of strip width as would be expected on purely geometrical grounds [17]. Figure 6 shows the changes in interstrip capacitance at 100V caused by irradiation with ^{60}Co photons up to 200krad. The devices were irradiated with a detector bias of 100V and with 40V across the coupling capacitors. Some increases are observed at 100kHz, with the changes already close to saturation by 200krad, but at 1MHz there are no significant changes in interstrip capacitance for either the 50μm or 100μm strips.

c) Microdischarge effects

Recent results obtained within the SDC collaboration have shown that maintaining a voltage across the coupling capacitors of AC-coupled p-side microstrips can lead to microdischarges which generate unacceptable levels of excess noise [18]. This problem is caused by local regions of high electric field being created at the edges of the p^+ strips leading to impact ionisation effects and is made worse by oxide charge build-up. It occurs only for devices where the readout metal extends beyond the p^+, and therefore can be avoided if the metal is kept a safe distance within the p^+. It has also been indicated that this effect can occur on the n-side and, although in this case oxide charge build-up could possibly be beneficial by shifting the threshold voltage of the onset of the effect, it is clear that this would represent a potential problem for field plate devices since they rely on the metal overlap for isolation.

Figure 7(a) shows the leakage current curves for unirradiated 50μm field plate strips where the n-side strips and guard are held at ground potential via the current measuring equipment and the (negative) bias voltage is applied to the p-side. When the field plates are biased, they are also connected to the same bias voltage as for the p-side. For this measurement, made on a probe station, only four field plates out of twenty are actually biased. With the field plates floating, it can be seen that the leakage current curves[5] show no unusual behaviour up to 150V. However, when the field plates are biased the leakage currents begin to rise at around 120V, indicating the onset of microdischarges. The bias value at which the effect begins to occur is not geometry dependent, probably because the largest overlap is due to the bond pads and therefore the same for all devices, but it can be seen that the wider overlaps lead to higher gradients for the leakage current as the bias is increased.

This effect could be expected to be stronger once the junction has moved to the n-side after type inversion. Figure 7(b) shows a similar measurement, but now with all twenty field plates bonded out, made on 50μm field plate strips which were irradiated with neutrons to a dose of 5×10^{13} n.cm^{-2}, well beyond type inversion, at the ISIS neutron spallation source[6], Daresbury Rutherford Appleton Laboratory, UK [19]. The irradiation was made at room temperature, and the measurements were made after several months storage at room temperature, so substantial annealing will have occurred. Even though the leakage currents are much higher due to the neutron damage (note the change of scale), it can be seen that the effects now become visible at a lower voltage.

Figure 7(c) shows the effect of increased oxide charge. The same device used for the measurements in figure 7(b) was irradiated with 0.9 Mrad of ^{60}Co photons, the detector being fully biased during irradiation with 100V across both detector and all field plates. It can be see that, with the exception of the anomalous 10μm strips, the current increases are not visible until ~ 135V indicating that higher oxide charge does indeed delay the onset of the microdischarges.

This effect represents a clear limitation to the use of field plate devices. The investigations presented here are not exhaustive, and it is conceivable that the problems could be controlled by careful process design. It is also possible to use biasing schemes where only the potential difference necessary to ensure good isolation is applied across the field plates. However, on the basis of these results it is not clear whether the threshold for microdischarges for these devices could be maintained above 100V under LHC conditions. It is, however, clear that the design of p-stop devices, which do not require any voltage difference between readout

metal and strip, should be able to avoid this problem simply by keeping the metal within the n^+.

5 P-stop results[7]

a) P-stop strip isolation

For p-stop isolation, the important parameter is whether the p-stop doping is high enough to compensate the effects of the oxide charge, especially after high doses of ionising radiation, and therefore achieve good strip isolation once full depletion has been reached.

i) Before irradiation

Three p-stop implant doses were investigated, 1×10^{11}, 9×10^{11}, and 5×10^{13} cm^{-2}. Figure 8 shows the interstrip isolation measured at a bias of 100V for 100μm pitch common p-stop devices with different p-stop dopings (the depletion voltage of all devices is ~ 50V). It can be seen that the low 1×10^{11} cm^{-2} doping is inadequate, whereas the intermediate 9×10^{11} cm^{-2} provides good isolation and the high 5×10^{13} cm^{-2} provides isolation comparable with good p-side microstrip isolation. It can also be seen, for the intermediate doping, that the 65μm strip, 5μm p-stop devices are systematically worse than the other geometries, indicating that a slightly wider p-stop is advisable at this pitch. This was not true for the 50μm pitch strips where the isolation resistance was consistent across all geometries for a particular p-stop doping. No differences were observed between common p-stop and individual p-stop devices.

ii) After photon irradiation

Figure 9 shows the interstrip isolation measured at 100V as a function of ^{60}Co photon dose for 50μm pitch common p-stop devices with (a) 9×10^{11} cm^{-2} p-stop doping, and (b) 5×10^{13} cm^{-2} p-stop doping. The devices were irradiated under 100V bias. It can be seen that the isolation resistance of the strips with 9×10^{11} cm^{-2} p-stop doping drops rapidly to a value which is no more than marginal for operation, whereas the isolation of the 5×10^{13} cm^{-2} strips remains comfortably high. All changes are approximately saturated by 1Mrad. For the 9×10^{11} cm^{-2} p-stop doping it can be seen that the better performance is obtained from the wider p-stops, but for the 5×10^{13} cm^{-2} p-stop doping it appears that the widest p-stop (ie narrowest n^+/p^+ gap) is significantly worse than the other.

iii) After neutron irradiation

Figure 10 shows the interstrip isolation measured at 100V for 100μm pitch common p-stop devices irradiated with neutrons at ISIS. The devices were irradiated unmounted, unbiased, and at room temperature, with measurements being made approximately two weeks after the end of the irradiation. The interstrip isolation for the devices with 9×10^{11} cm^{-2} p-stop doping, figure 10(a), is seen to fall to unacceptably low levels. It is not entirely clear why this should happen, but one possible explanation is that other materials present during this irradiation may have caused unusually high levels of photon contamination. The decreases in isolation resistance for the devices with 5×10^{13} cm^{-2} doping, figure 10(b), are acceptable, and are consistent with the influence of the increased strip leakage currents on the measurements.

These results show that, with a suitable choice of p-stop doping, the strip isolation of p-stop strips will remain satisfactory for the radiation doses to be expected at the LHC. Dose rate effects may still be important, but it should be possible to choose the p-stop doping to be high enough so that there is a comfortable safety margin for avoiding such problems.

b) P-stop voltage

Due to reach-through between the p-side of the detector and the p-stops on the n-side of the detector, the p-stops begin to take up a voltage different to that of the n^+ strips once the depletion region has reached the n-side, with this voltage increasing approximately linearly with bias from that point. For a given bias voltage, the p-stop voltage is seen to be dependent on the geometry and on the p-stop doping, although surface quality and leakage currents can also be factors. After type-inversion, the substrate is effectively p-type and so the junctions are now at the n-side of the detector. In addition, the p-stop voltage is no longer determined by reach-through and should essentially act as an ohmic contact to the bulk. Figure 11 shows the p-stop voltage measured against bias[8] for the same common p-stop geometry after neutron irradiation at ISIS. After 2×10^{12} n.cm^{-2}, the depletion voltage has reduced from 50V to 20V but the net doping concentration is still n-type and this is confirmed by the p-stop voltage which remains at approximately zero until full depletion is reached. The voltage gradient is similar to that for the unirradiated device, and therefore the p-stop voltage at 100V has increased over the unirradiated value. After a much higher dose of 5×10^{13} n.cm^{-2}, the device is well past type inversion and it can be seen that the p-stop voltage begins rising immediately bias is applied leading to the p-stop voltage at 100V bias being still higher.

Figure 12 shows the p-stop voltage at 100V as a function of neutron fluence for (a) 50μm pitch common p-stop strips, and (b) 100μm pitch common p-stop strips (note the different scales for the two graphs). The geometry dependence can also be clearly seen, with the p-stop voltage being higher for wider p-stops. In particular, it can be seen that the combination of 100μm pitch, narrow strips and wide p-stops lead to p-stop voltages high enough to raise long term issues of reliability against breakdown across the narrow n^+/p^+ gap. In addition, if radiation dose levels are substantially non-uniform across a single device, the possibility of only part of that device being beyond inversion along the length of the p-stop may raise problems.

The influence of ^{60}Co photon damage on p-stop voltage was also investigated. Figure 13 shows the p-stop voltage at 100V bias as a function of dose for 100μm pitch common p-stop devices with (a) 9×10^{11} cm^{-2} p-stop doping, and (b) 5×10^{13} cm^{-2} p-stop doping. The devices were irradiated under 100V bias. The lower p-stop voltage for the lower p-stop doping can be seen, and it is observed that the 9×10^{11} cm^{-2} p-stop voltage decreases by roughly a factor of two. Comparison of figure 13(a) with figure 9(a) suggests a direct correlation between the decrease of p-stop voltage and the decrease in interstrip isolation. The 5×10^{13} p-stop voltage changes are small. In both cases, the changes are approximately saturated by 1Mrad.

c) Geometry dependence of depletion voltage after inversion

For p-side microstrip structures, large gaps between p^+ strips lead to the need for significantly greater bias than the nominal depletion voltage defined by the substrate doping [17]. For n-side microstrips this is not, in general, a problem since the detector depletes from the p-side. However, after type-inversion the detector depletes from the n-side and therefore large gaps on the n-side represent a similar problem to large gaps on the p-side before inversion. Figure 14 shows the depletion capacitance curve, measured between five n-side strips connected together and the matching p-side surface, for 100μm common p-stop strips (a) unirradiated, and (b) after type inversion.

Before irradiation there is no geometrical dependence in the point at which the curves level off. After type inversion, there is a clear geometrical dependence with the wider gaps requiring higher bias to achieve full depletion. Furthermore, signal studies using a 1064nm infra-red laser to simulate the passage of minimum ionising particle indicate that, for the devices after type inversion, the bias required for correct operation of the narrowest strip is around 50% higher than the bias at which the CV curve indicates full depletion. Figure 15 shows the variation of pulse height

with bias for the same devices used in figure 14, read out using a prototype of the RD20 low noise preamplifier/shaper which has nominal peaking time of 45ns [20].

It is also interesting to compare the behaviour of the n-side strips after inversion with similar geometry p-side microstrips. Figure 16 shows the comparison of the depletion voltages, taken as the intersection of the two gradients on the log/log CV curve, normalised to the values for the widest strips. It can be seen that the unirradiated p-side strips and the n-side strips after type inversion behave identically. Although we have not verified this experimentally with field plate devices, this would seem to imply that the presence of the p-stops does not play a major part in this behaviour and therefore that this post-inversion geometry dependence should be equally applicable to field plate structures.

d) P-stop strip capacitance

Having determined that the high 5×10^{13} cm^{-2} p-stop doping is necessary to maintain satisfactory isolation under high levels of irradiation, we restrict our discussion of the strip capacitance to these devices. Results comparing the capacitance of intermediate doping p-stops and high doping p-stops before irradiation have already been published [21,22].

i) Before irradiation

Figure 17 shows the unirradiated strip capacitances at 100V bias for (a) 50μm common p-stop devices, and (b) 100μm common p-stop devices. Results from 4cm devices are shown, but there were no significant differences in the values for the 2cm devices. For both pitches it can be seen that there is significant frequency dependence in the nearest neighbour capacitance[9] and also in the non-adjacent neighbour capacitance[10], with the 100kHz values being generally higher than the 1MHz values. The backplane capacitances have no significant frequency or geometry dependence.

The nearest neighbour capacitance is sensitive to the surface region, and by comparison with the unirradiated values from figure 12, it is observed that lower p-stop voltages correspond to greater differences between the 100kHz and 1MHz values. The importance of the p-stop voltage for the strip capacitance of these devices is demonstrated in figure 18. In figure 18(a), the nearest neighbour capacitance, measured against bias up to 100V, is plotted as a function of p-stop voltage, also measured against bias up to 100V, for the three different 50μm pitch,

5μm strip width, common p-stop devices. It can be seen that the characteristics are very similar for the different devices at both frequencies. The origin of the frequency dependence at 100V is now clear since all three curves at 1MHz are close to their limiting values once the p-stop voltage has passed 6V, whereas the 100kHz values are still decreasing beyond a p-stop voltage of 9V. Figure 18(b) shows that, by first scaling the data to the 1MHz, 100V values in order to remove the geometrical width/pitch dependence, very similar behaviour is seen from the 100μm pitch devices.

Figures 17(b) and 18(b) also show that the nearest neighbour capacitance for the 5μm strip width and 100μm pitch at 100kHz actually decreases below the 1MHz values at 100V. Figure 19 shows the capacitance of corresponding 100μm pitch individual p-stop strips. The 100kHz and 1MHz nearest neighbour values are much closer for all the geometries, probably because of better surface quality on this device, but what is clear is that the nearest neighbour capacitance at 100kHz is never lower than at 1MHz. In addition, the non-adjacent neighbour capacitance values are now essentially independent of frequency, as would be expected on purely geometrical grounds.

The decrease of the 100kHz nearest neighbour values below the 1MHz values for the narrowest 100μm pitch strips is probably due to an additional coupling of the strips to the guard affecting the measured values. This will be addressed in more detail in a later section, but for these devices the effects are small.

The extra non-adjacent neighbour capacitance, which is shown more clearly in figure 20, can be explained by the fact that the strip now has an additional capacitive path to the non-adjacent neighbours via the conductivity of the p-stop. This additional capacitance will be determined by the frequency of interest combined with the conductivity of the p-stop and its capacitive coupling to all the other conductors in the system. Figure 20 shows that this is significant at 100kHz, but only small at 1MHz, with the narrowest p-stop always having the lowest amount of extra capacitance. This was also confirmed by measurements of the non-adjacent capacitance of the common p-stop devices with intermediate doping [21,22], where the values were similar to the individual p-stop values. However, the fact that the widest p-stop does not exhibit the largest additional capacitance indicates that the effect of the p-stop network is not entirely trivial. It should also be noted that this effect is likely to be stronger at lower frequencies, which could have implications for

large scale systems where problems with low frequency common-mode interference can arise.

ii) After photon irradiation

Figure 21 shows the variation of nearest neighbour capacitance at 100V as function of photon dose, measured at 1MHz, for (a) 50μm pitch common p-stop strips, and (b) 100μm common p-stop strips. The devices were irradiated biased at 100V. Significant increases are seen in both cases. For the 50μm pitch, the increases are largest for the devices with the widest gap between n^+ and p^+, where the oxide/silicon interface is exposed. At 100μm pitch, the increases are largest for the widest strips with the narrowest p-stops (the n^+/p^+ gap is kept constant). The capacitance to the non-adjacent neighbours and to the backplane remained constant.

iii) After neutron irradiation

The effect of neutron irradiation alone on strip capacitance was not expected to be large since we have already shown that the capacitance values for these devices are close to being independent of bias once the p-stop voltage has reached about 6V. However, the increased p-stop voltages beyond inversion can be expected to be beneficial for the capacitance as the oxide damage increases. Figure 22 shows the nearest neighbour capacitance, measured at 100V and 1MHz, for unirradiated devices, after neutron-irradiation at ISIS to a dose of 2.5×10^{13} n.cm^{-2} (beyond type inversion), and finally after a further ^{60}Co photon irradiation, biased at 100V during irradiation, up to a dose of 6Mrad. It can be seen that there are small decreases after the initial neutron irradiation, due to the large increases in p-stop voltage. After photon irradiation in addition to the neutron irradiation, the increases are significantly lower than for the devices irradiated only with photons.

It is also interesting to compare our results with those from Hamamatsu devices with similar geometries already published by the SDC collaboration [ref 6, figure 7]. For ease of comparison, figure 23 shows the variation of interstrip capacitance at 1MHz and 100V with photon dose for both unirradiated and neutron-irradiated 50μm pitch SINTEF devices. The pre-irradiation SDC values exhibit a much wider variation with p-stop width, but the widest p-stop device is close in value to the widest p-stop SINTEF device. The bias voltage is not quoted, but it seems likely that the capacitance values for the narrower p-stops had not yet reached their limiting values. The general trend with photon irradiation for both sets of devices is that wider p-stops lead to lower capacitance increases. Also shown in [ref 6, figure 7] are

the capacitances measured after proton irradiation to 3.5Mrad, beyond type-inversion. Comparison with the neutron-irradiated SINTEF devices, also in figure 23, shows generally good agreement for the narrower p-stops but a substantially lower value for the SDC strips with the widest p-stop.

No reference to p-stop voltage is made in [6], but the general inference from both sets of data is that the evolution of the detector capacitance with dose under LHC conditions will be determined by the two competing processes of increasing oxide charge and increasing p-stop voltage. The p-stops should be as wide as possible, although care should be taken to ensure that long-term breakdown problems do not arise due to high p-stop voltages across very small n^+/p^+ gaps.

iv) Comparison with other manufacturers

A set of common and individual p-stop devices, closely matching in design those produced at SINTEF, were also produced for RD20 at Micron Semiconductor Ltd, Lancing, UK [23]. The process included polysilicon resistors on both sides of the wafer, but only single metal layers. The p-stop sheet resistance was approximately 1kΩ/square, twice that of the highest-doping SINTEF p-stop devices. First results of unirradiated strip capacitance are presented here. Figure 24 shows the capacitances of 2cm DC-coupled devices at 100V for (a) 100μm pitch common p-stop devices and (b) 100μm pitch individual p-stop devices. It can be seen that the totals at 100V are approximately 0.5pF/cm higher than the equivalent SINTEF devices, for all geometries, which is entirely due to higher nearest neighbour capacitance. An attempt was made with one of the devices to identify whether humidity could be a contributing factor, but no significant changes were observed after three weeks in a dry atmosphere at room temperature. Also plotted in figure 24 are the totals at 200V bias, where the nearest neighbour capacitance was beginning to level off, and the values are more consistent with the SINTEF devices. The frequency dependence of the nearest neighbour capacitance is stronger for these common p-stop devices than for the SINTEF equivalents, with all geometries appearing to have a lower nearest neighbour capacitance at 100kHz than at 1MHz. For the individual p-stop devices, the nearest neighbour capacitance is almost identical for the two frequencies and so it is clear that the network of the common p-stop is disturbing the measurement in some way.

Figure 25 shows the capacitance of a single strip to the guard ring, with all other strips biased correctly, for both common and individual p-stop devices and, in addition, the corresponding values for one of the SINTEF 2cm common p-stop

100μm pitch devices. The capacitance deficit for the common p-stops at 100kHz can be clearly seen to be due to the substantially increased capacitance to the guard at this frequency. However, it should be noted that, without careful analysis of the p-stop network, it cannot be simply stated at what level the guard capacitance will affect the other measurements. For the SINTEF devices, the capacitance to the guard is significantly lower than for the Micron devices but, in any case, the good agreement between 4cm and 2cm long devices, and also generally between common and individual p-stops, shows that it does not strongly affect the other measured values. It also appears that, for all devices investigated in this work, the 1MHz frequency is high enough to avoid the undesirable effects of the common p-stop network.

v) Sensitivity to processing

Some of the SINTEF wafers required reprocessing due to over-etching of the first metal layer. This involved plasma stripping followed by reworking of the polyimide and both metal layers on the n-side of the wafers. The capacitance behaviour of p-stop devices from these wafers were found to be very similar to those of the Micron strips, with substantially higher nearest neighbour capacitances at 100V in comparison to the original, non-reprocessed wafers. It is interesting to note that the leakage current performance of the Micron devices was significantly better than that of the original SINTEF devices, which would indicate that the mechanisms responsible for surface leakage currents are not necessarily correlated with those which contribute to the capacitance.

vi) Possible alternatives to the common p-stop approach

The compactness of the common p-stop is clearly very attractive, and other design variants can be considered. The next simplest configuration is that of the "p-box" whereby each n^+ strip is entirely surrounded by its own individual p-stop "cage", separated from the neighbouring p-stops by small gaps. New designs incorporating this approach are presently in production.

6 Conclusions

A substantial comparative study has been made of n-side microstrips with field plate and p-stop isolation schemes. We have demonstrated that, with suitable design and processing, satisfactory isolation resistance can be maintained for both

techniques after radiation doses similar to those expected at LHC. There is little difference between strip capacitance values for field plate and p-stop devices before irradiation. After photon irradiation, the capacitance increases for field plate devices are marginal whereas p-stop devices show capacitance increases of ~25% at 100V. However, these increases will be suppressed in the presence of bulk damage by higher p-stop voltages due to the changes in effective resistivity. We have confirmed that the microdischarge phenomenon occurs for field plate devices, and therefore that it will be more difficult than for the p-stops to design and operate field plate detectors in high radiation environments. We have shown that, after type-inversion, n-side strips with narrow width and large pitch require increased bias voltages in a similar fashion to unirradiated p-side strips. For p-stop devices, we have identified some potential drawbacks with the simplest common p-stop structure and have proposed an alternative "p-box" approach for high radiation environments. We have also observed a strong sensitivity to processing which can lead to substantial variations in p-stop capacitance both between manufacturers and between different process runs from the same manufacturer.

7 Further results

This paper represents a summary of a very large amount of data. More details of the studies made within RD20 on these devices can be found in a number of RD20 technical notes [24-27] available on request from Carole Ponting at CERN.

8 Acknowledgements

This work has been funded by CERN and several national agencies: INFN (Italy), NAVF (Norway), KBN, The Polish State Committee for Scientific Research (Poland), SERC (UK). We thank them for their support. Irradiation facilities were provided by the ISIS facility at Daresbury Rutherford Appleton Laboratory and gamma sources at Imperial College and Cracow. Invaluable technical support was provided by the Imperial College electronics workshop. The electron beam masks used for the production of the wafers were produced by the Central Microstructure Facility at DRAL. Luciano Bosisio is thanked for helpful comments on the design of the p-stop devices, and finally we gratefully acknowledge the contributions of the rest of the RD20 collaboration through their feedback during this work.

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Footnotes

[1] The interstrip isolation resistance in all instances was determined from the gradient at zero voltage difference of the current of one strip measured against the voltage applied to both of its nearest neighbour strips.

[2] The minimum operational voltage for the field plate devices is defined here as the bias voltage at which the interstrip isolation increases above 10MΩ, this voltage being applied across both detector and coupling capacitors.

[3] All capacitances for both field plate and p-stop devices were measured using the parallel model.

[4] The interstrip capacitance is defined here as the capacitance between the central strip and all other strips, not just the nearest neighbour strips.

[5] The leakage currents are comparatively high, which we attribute to the presence of the nitride since it has already been observed to lead to higher surface-generated leakage currents on the p-side [3], but are not high enough to represent any problem for our application.

[6] The neutron spectrum at ISIS is typical of that expected at the LHC, peaked around 1MeV with a damage factor approximately 1.4 times greater than that of an equivalent fluence of monoenergetic 1MeV neutrons. All doses quoted have an absolute error of 20% due to limits in the accuracy of neutron cross-section data but a relative error of no more than 5%.

[7] Due to unexpected faults in the majority of the polysilicon resistors where they crossed the p-stops, all p-stop device measurements presented from the SI devices have been obtained from the DC-coupled test structures. Although this is not expected to significantly change the results with respect to AC-coupled devices, since the geometries remain the same, this does mean that the microdischarge effect discussed in the field plate section could not be addressed for the p-stop devices.

[8] In order to minimise loading of the p-stops, all measurements of p-stop voltage were made using a very high input impedance Keithley 617 electrometer. Contact to test points on the p-stops was made via probe needles only.

[9] The nearest neighbour capacitance is defined as the capacitance between the central strip and the strips immediately adjacent to it on either side.

[10] The capacitance to the non-adjacent neighbours, also referred to in the figures as the "other neighbours" is defined as the capacitance to all strips except the nearest neighbours. For the 50μm pitch DC-coupled devices with seven strips this refers to the pair of strips beyond the nearest neighbours on each side of the central strip. For the 100μm pitch DC-coupled devices with five strips there is only one non-adjacent neighbour strip on each side. In both cases, more strips on either side should contribute very little extra geometrical capacitance.

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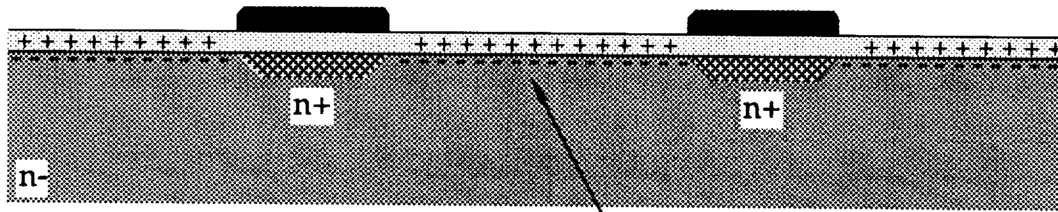
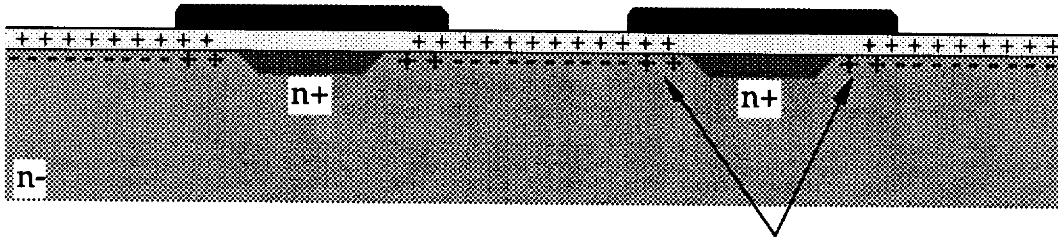
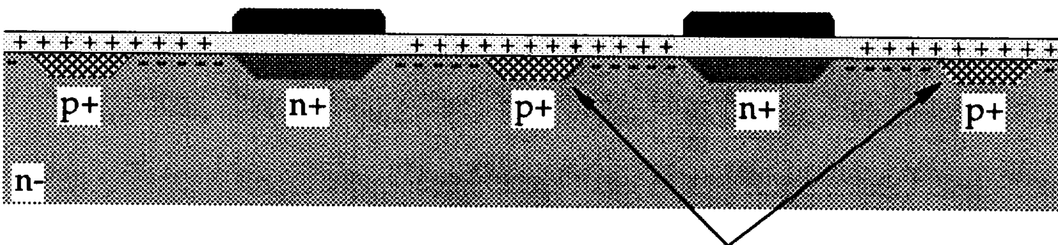


a) No isolation

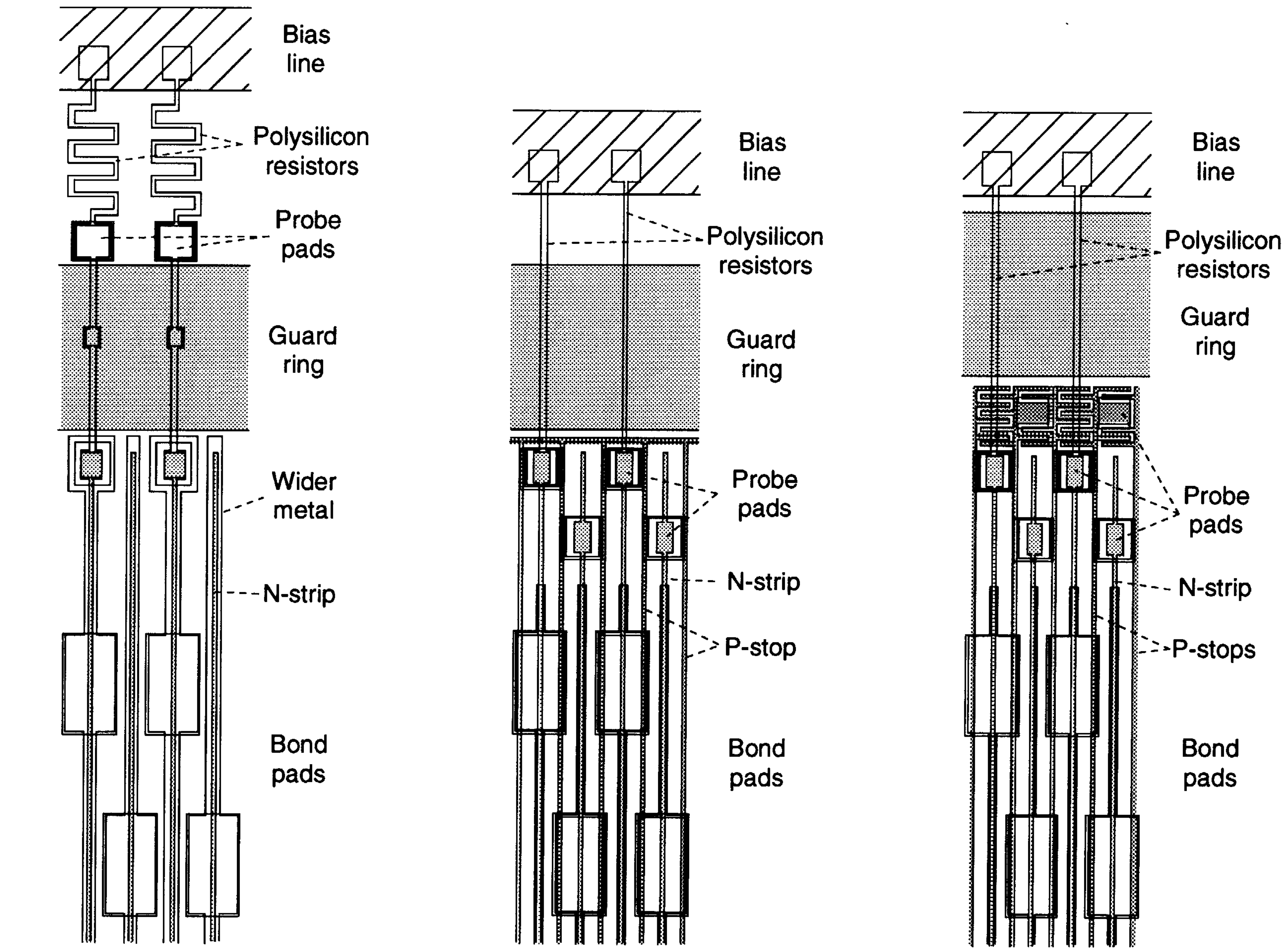


b) Field plate isolation



c) P-stop isolation

Figure 1



a) Field plate isolation b) Common p-stop isolation c) Individual p-stop isolation

Figure 2

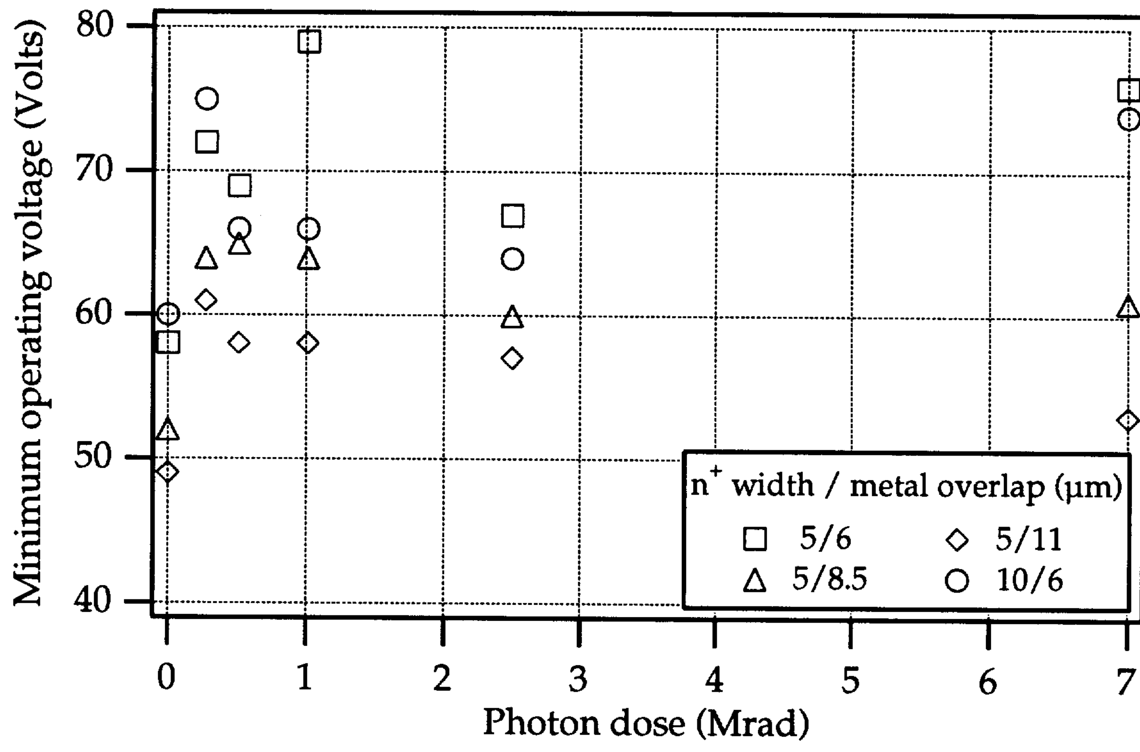


Figure 3 Minimum operating voltage for 50µm pitch field plates vs photon dose

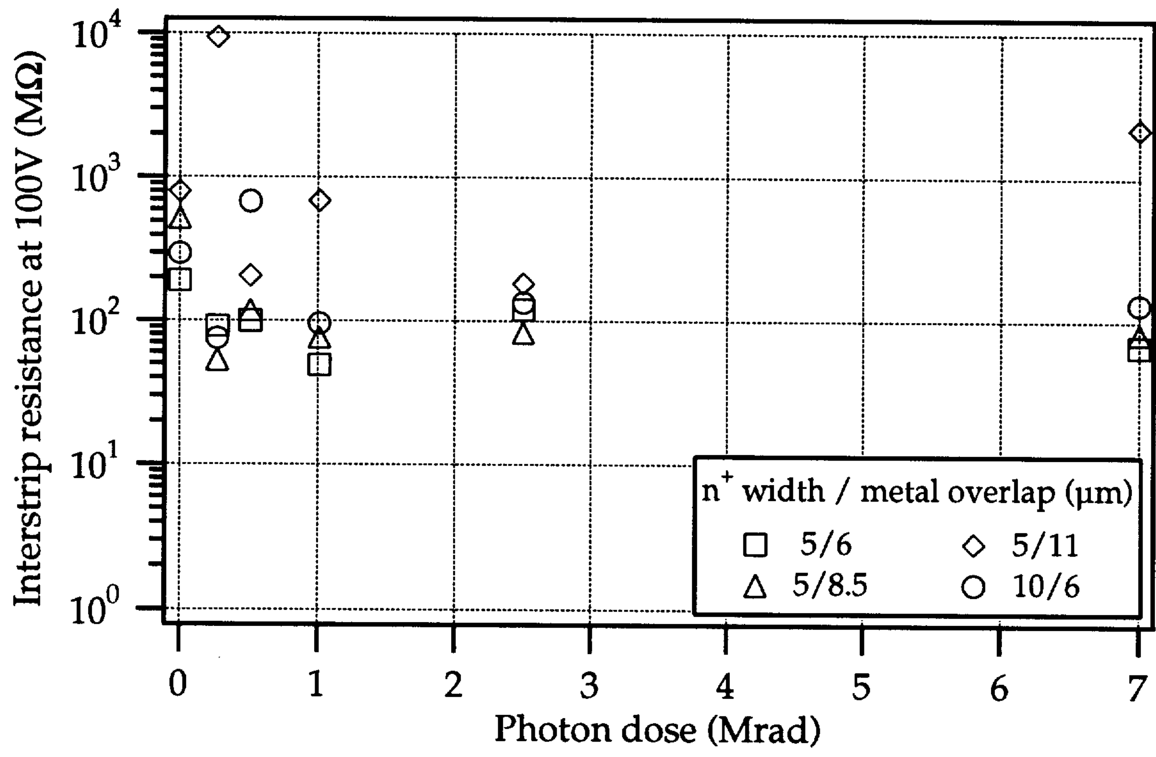


Figure 4 **50µm pitch field plate isolation at 100V vs photon dose**

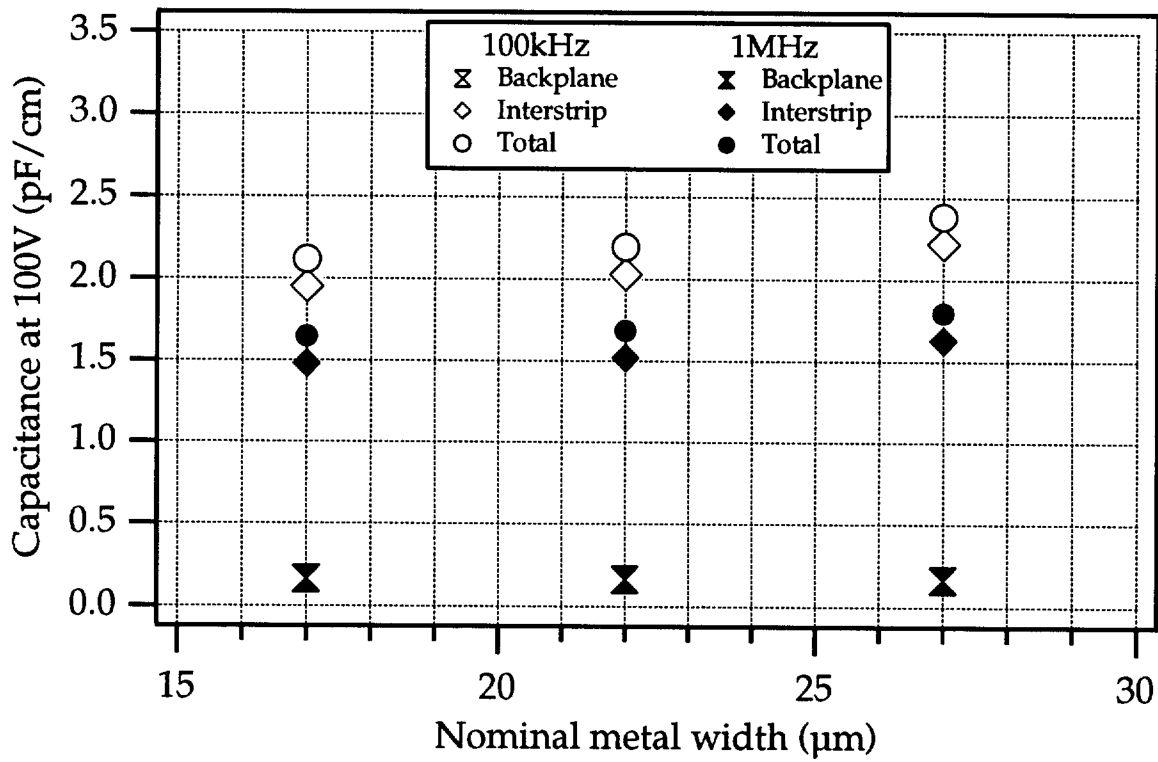


Figure 5(a) **Field plates, 50µm pitch, capacitance at 100V, unirradiated**

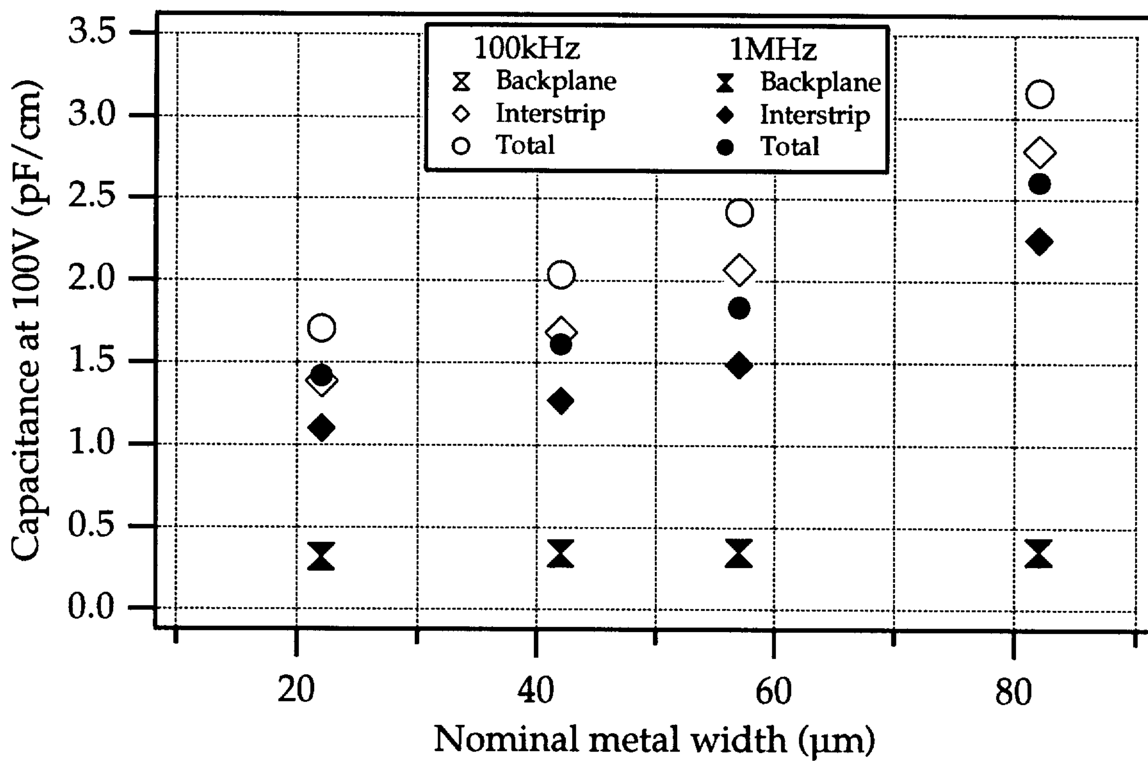


Figure 5(b) **Field plates, 100µm pitch, capacitance at 100V, unirradiated**

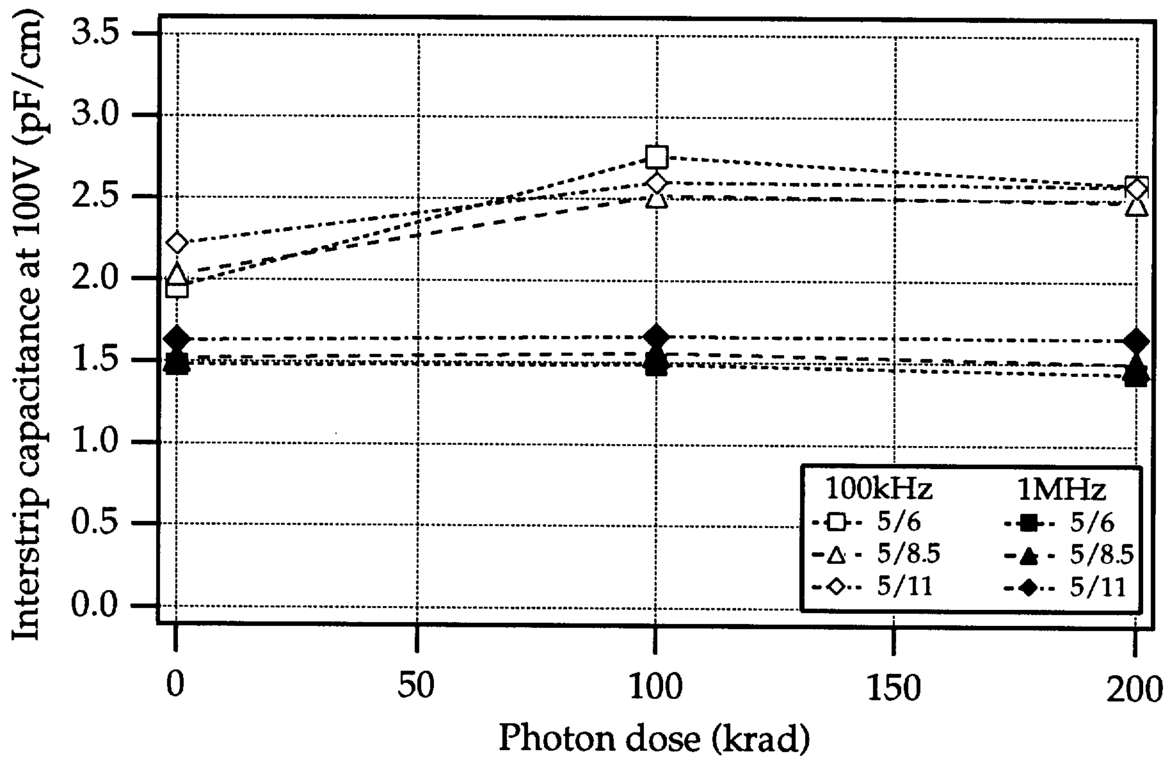


Figure 6(a) **Field plates, 50μm pitch, capacitance at 100V, photon irradiated under bias**

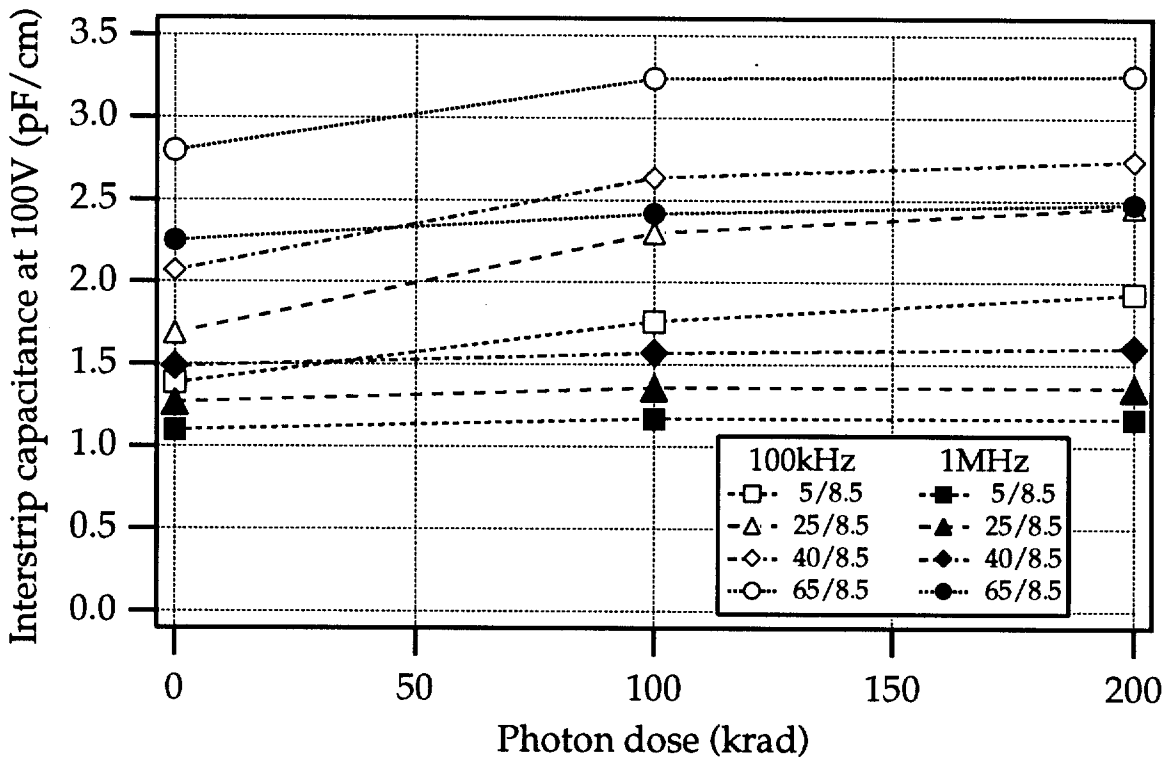


Figure 6(b) **Field plates, 100μm pitch, capacitance at 100V, photon irradiated under bias**

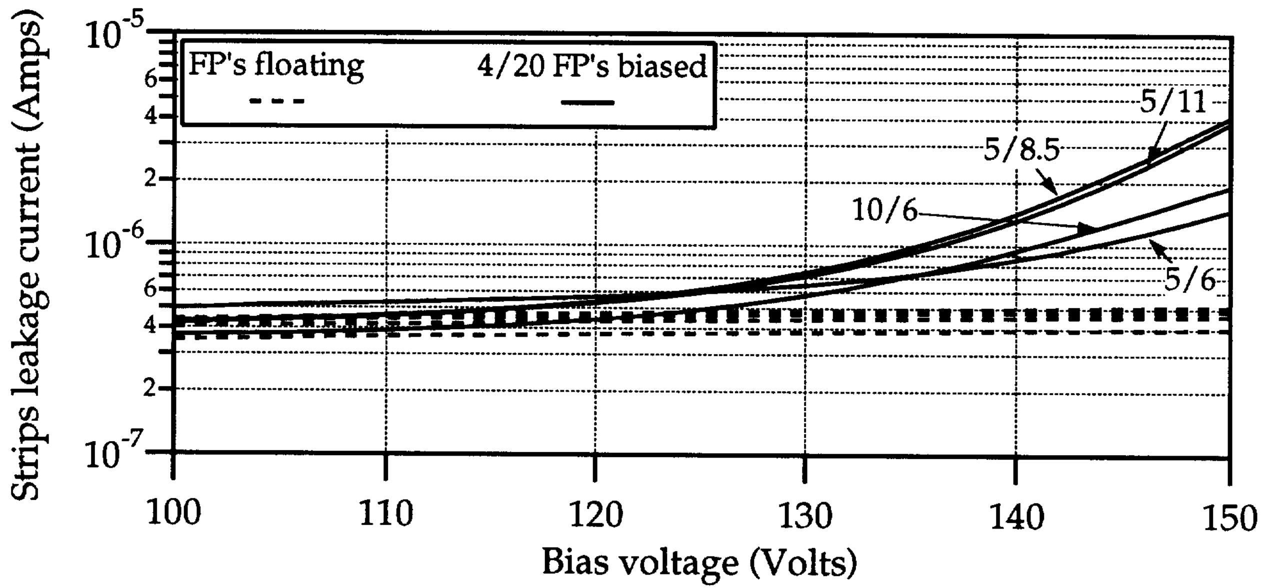


Figure 7(a) **Field plates, 50μm pitch, leakage current, unirradiated, fp's floating/biased**

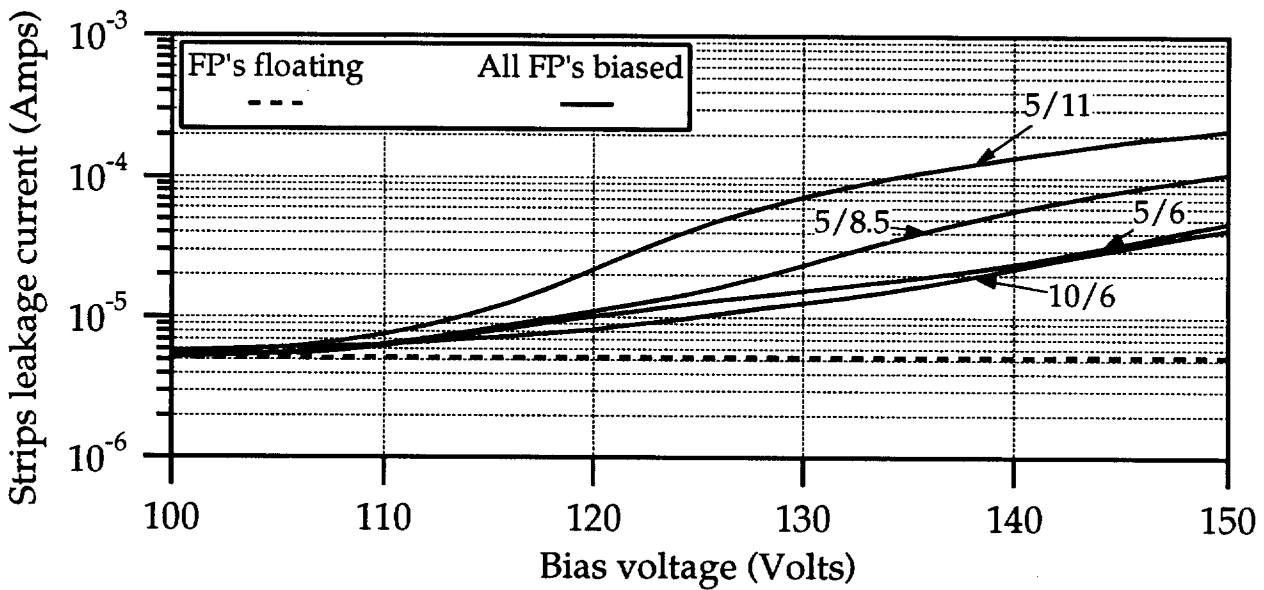


Figure 7(b) **FP50 leakage current, 5e13 neutrons + long anneal, fp's floating/biased**

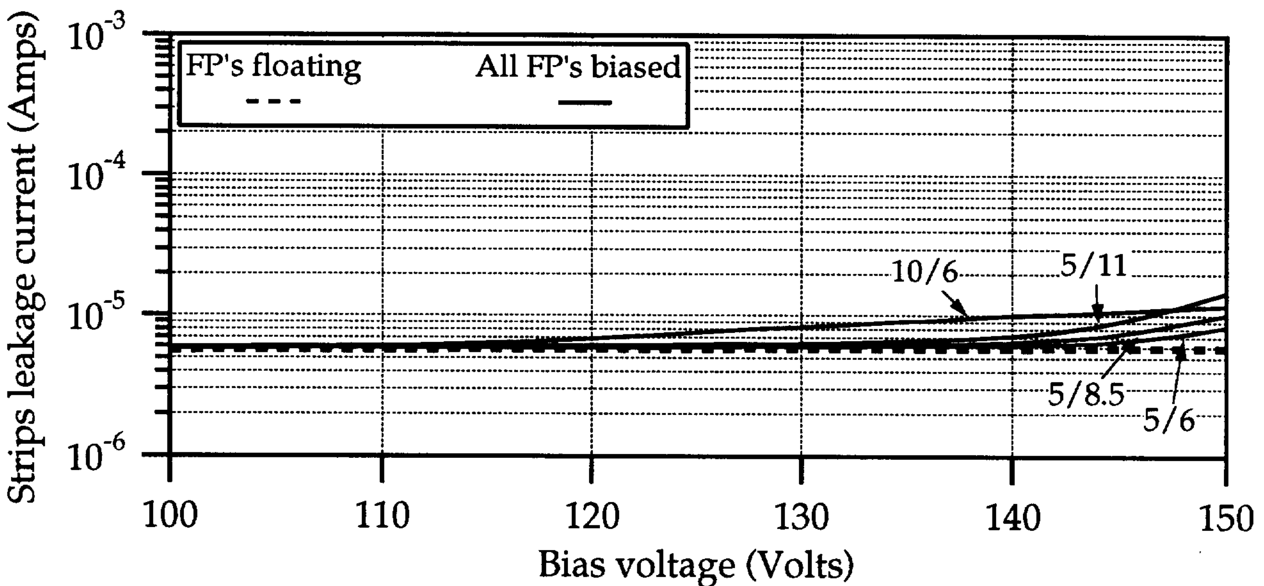


Figure 7(c) **FP50 leakage current, 5e13 n + 0.9Mrad photons, fp's floating/biased**

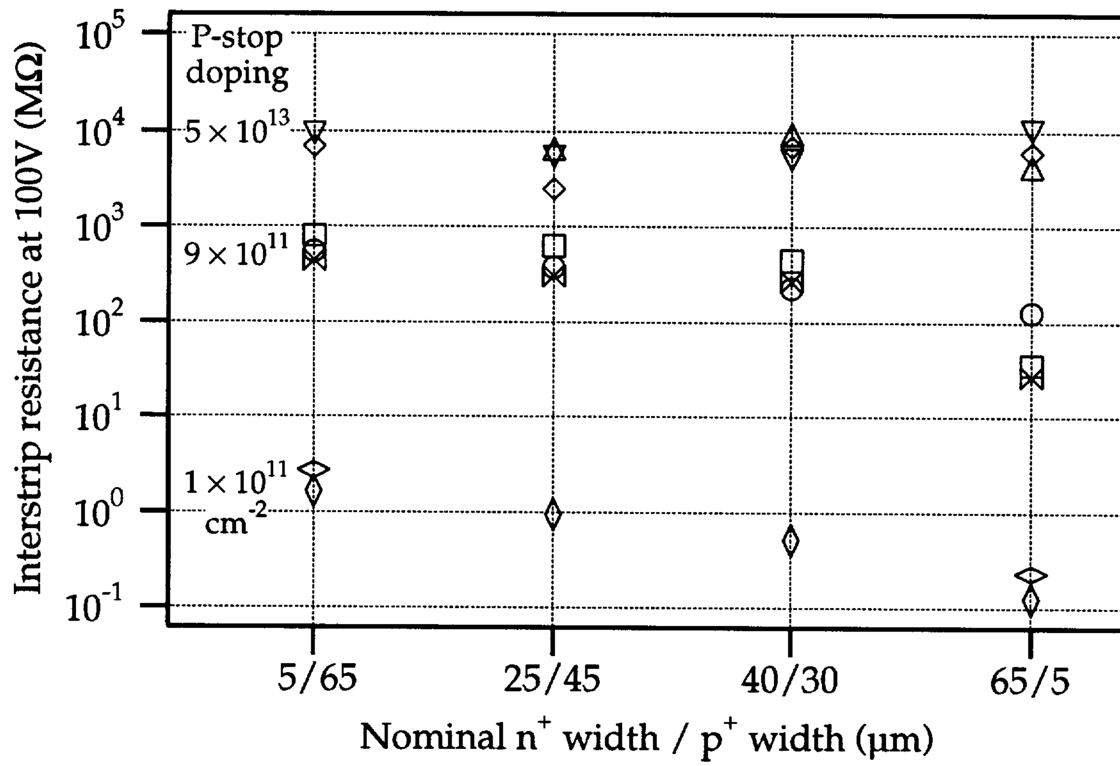


Figure 8 Common p-stops with different p-stop doping densities, 100μm pitch, interstrip isolation at 100V, unirradiated.

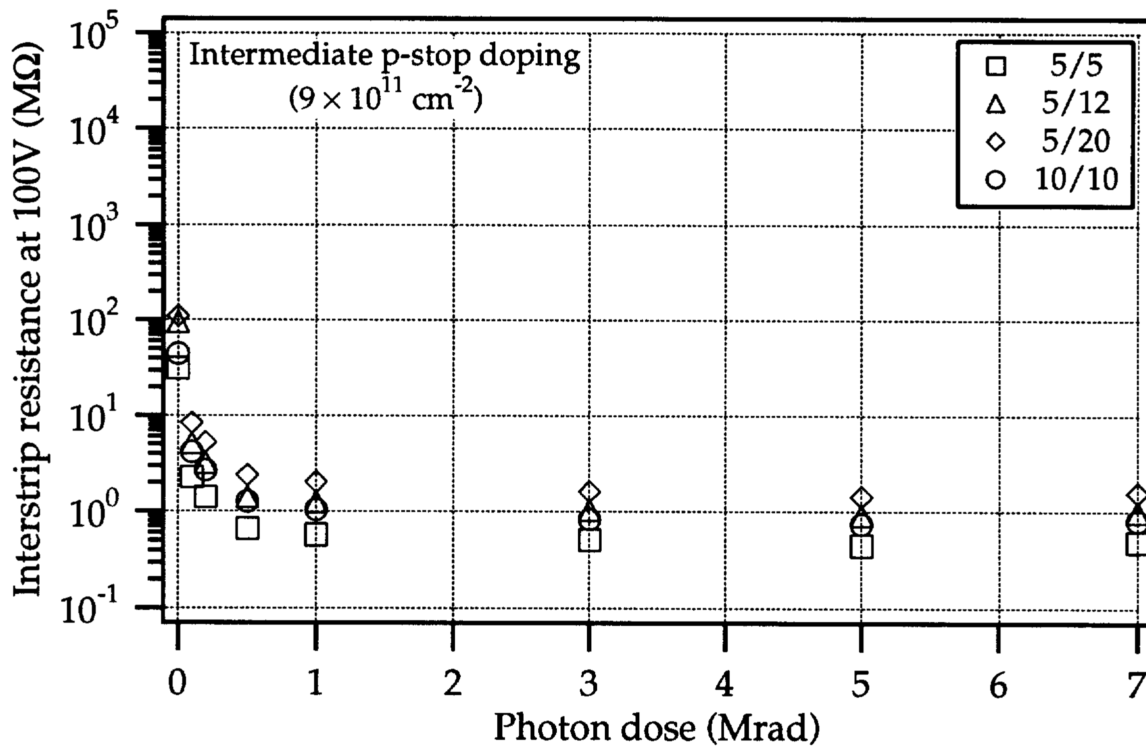


Figure 9(a) Common p-stops, 50μm pitch, intermediate p-stop doping, interstrip isolation at 100V vs photon dose

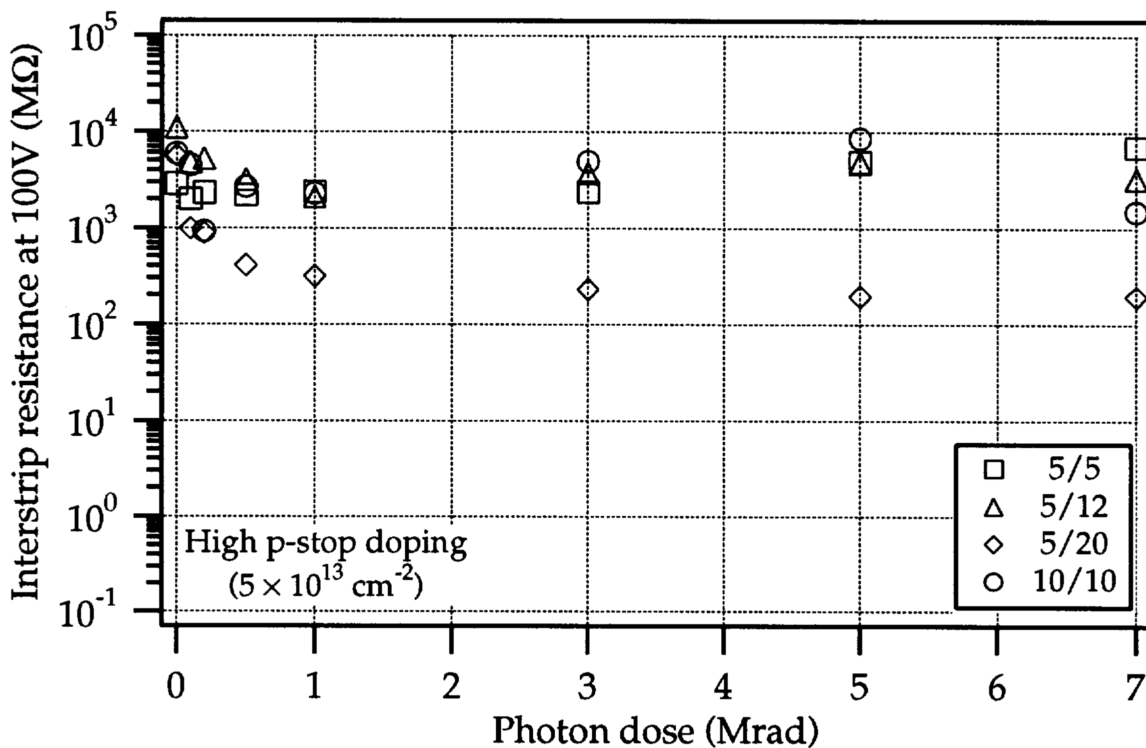


Figure 9(b) Common p-stops, 50μm pitch, high p-stop doping, interstrip isolation at 100V vs photon dose

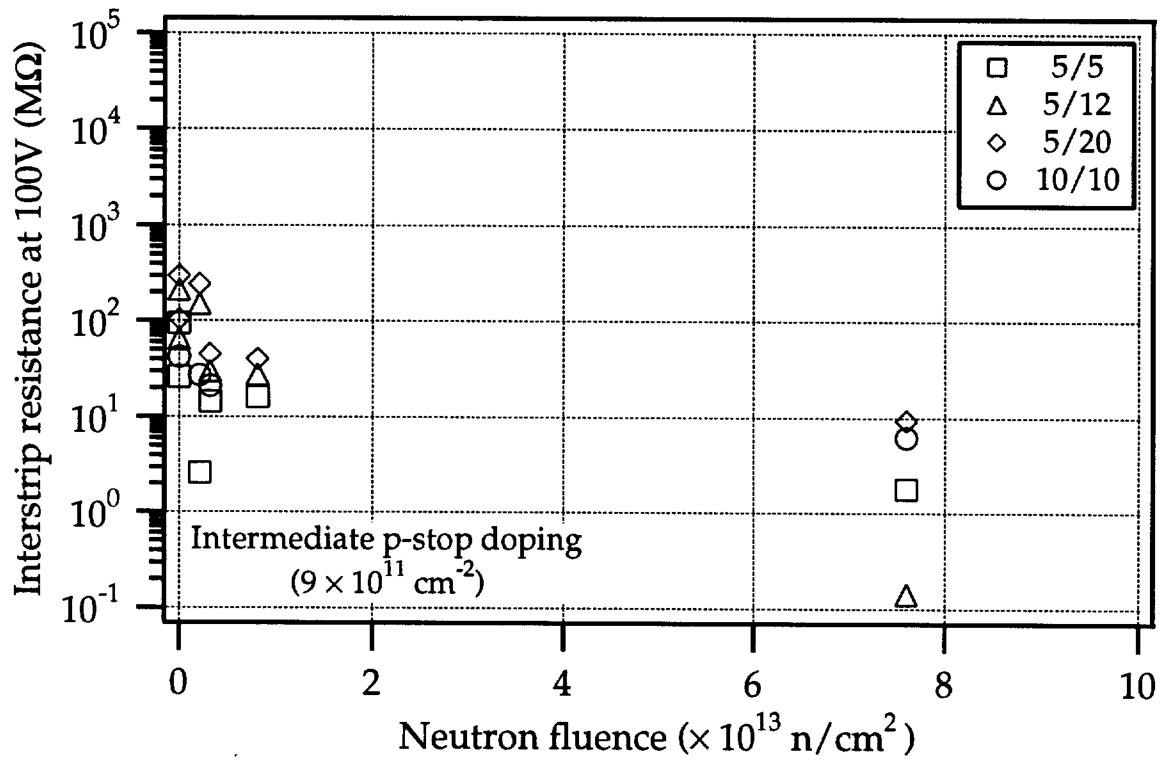


Figure 10(a) Interstrip isoln at 100V vs neutron fluence for 50μm pitch common p-stops, intermediate p-stop doping

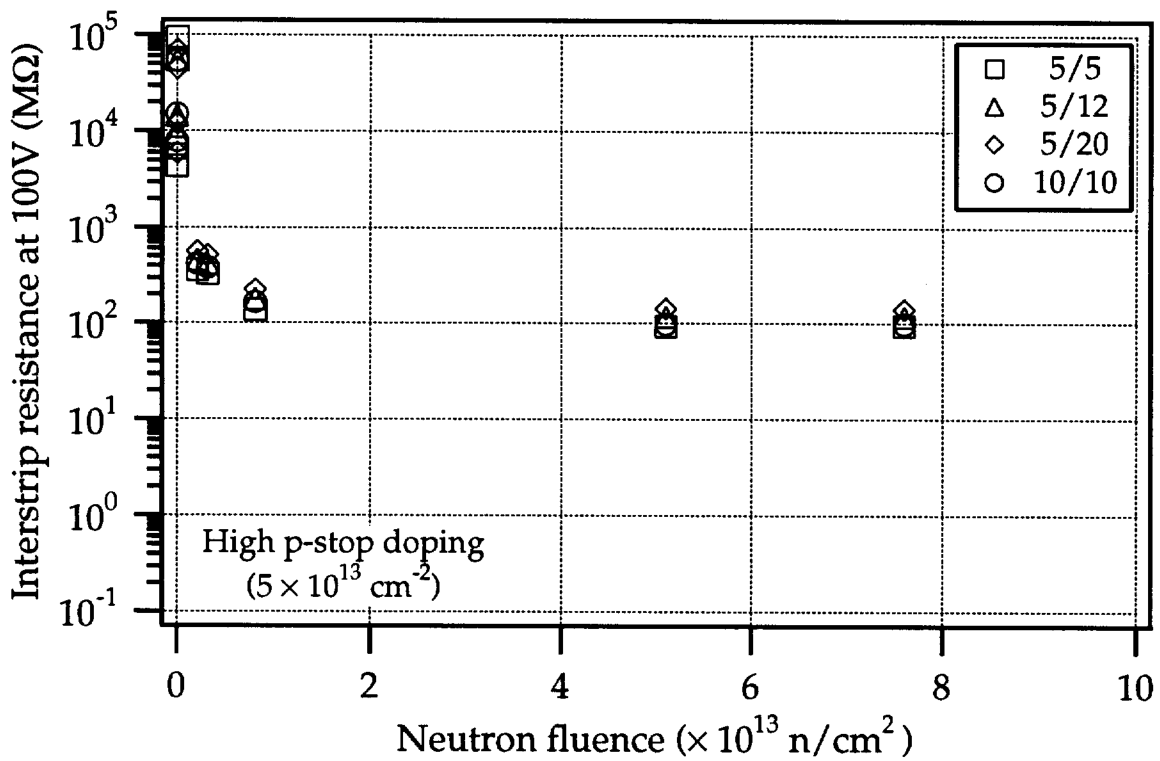


Figure 10(b) Interstrip isoln at 100V vs neutron fluence for 50μm pitch common p-stops, high p-stop doping

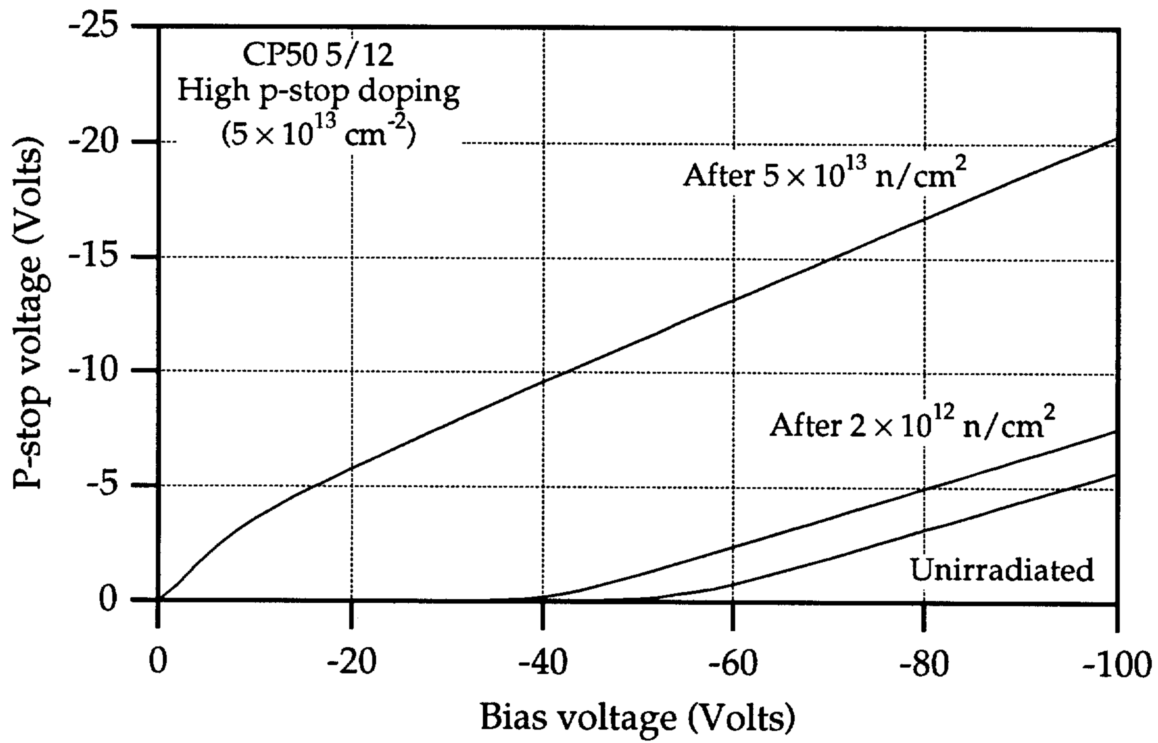


Figure 11 P-stop voltage vs bias for common p-stop device 5/12, 50µm pitch, after different neutron fluences, high p-stop doping

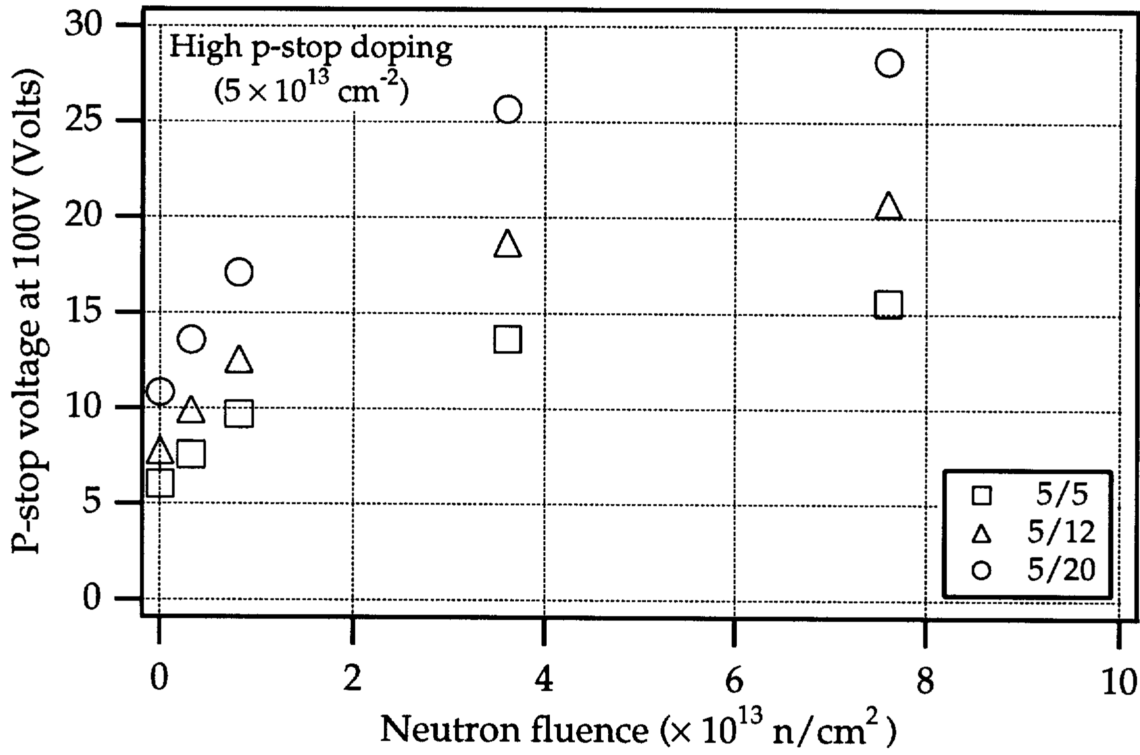


Figure 12(a) P-stop voltage at 100V vs neutron fluence, 50μm common p-stop strips, high p-stop doping

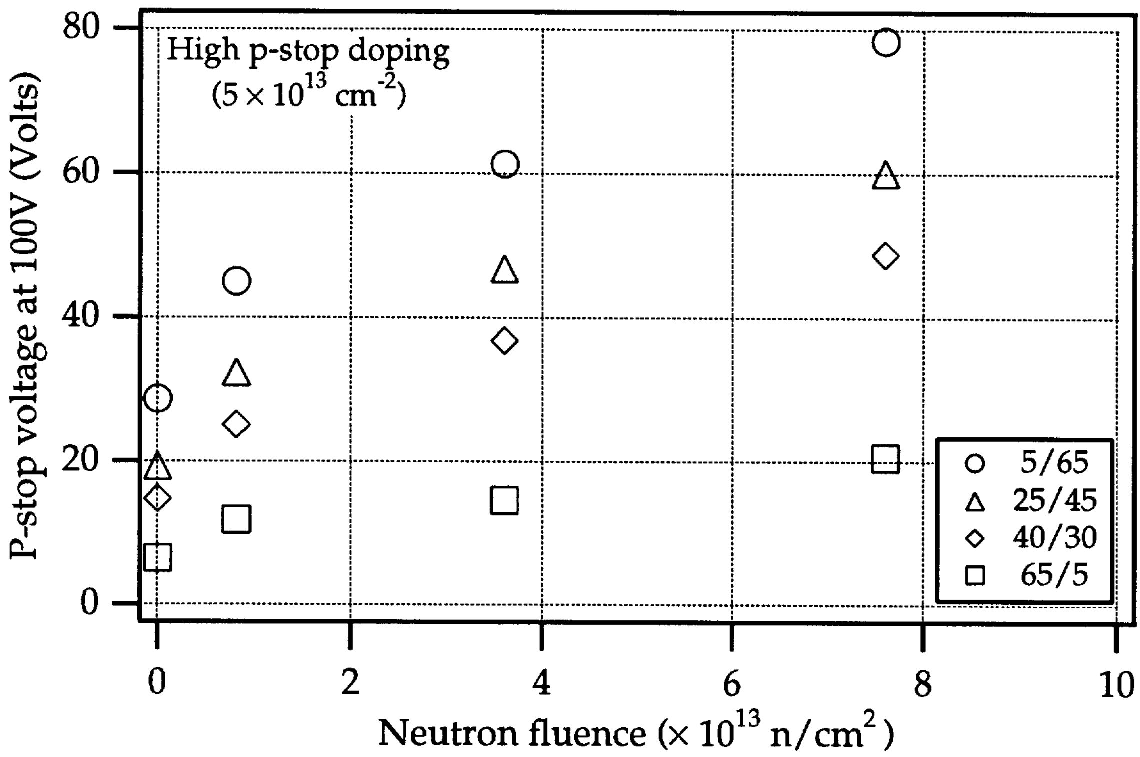


Figure 12(b) P-stop voltage at 100V vs neutron fluence, 100μm common p-stop strips, high p-stop doping

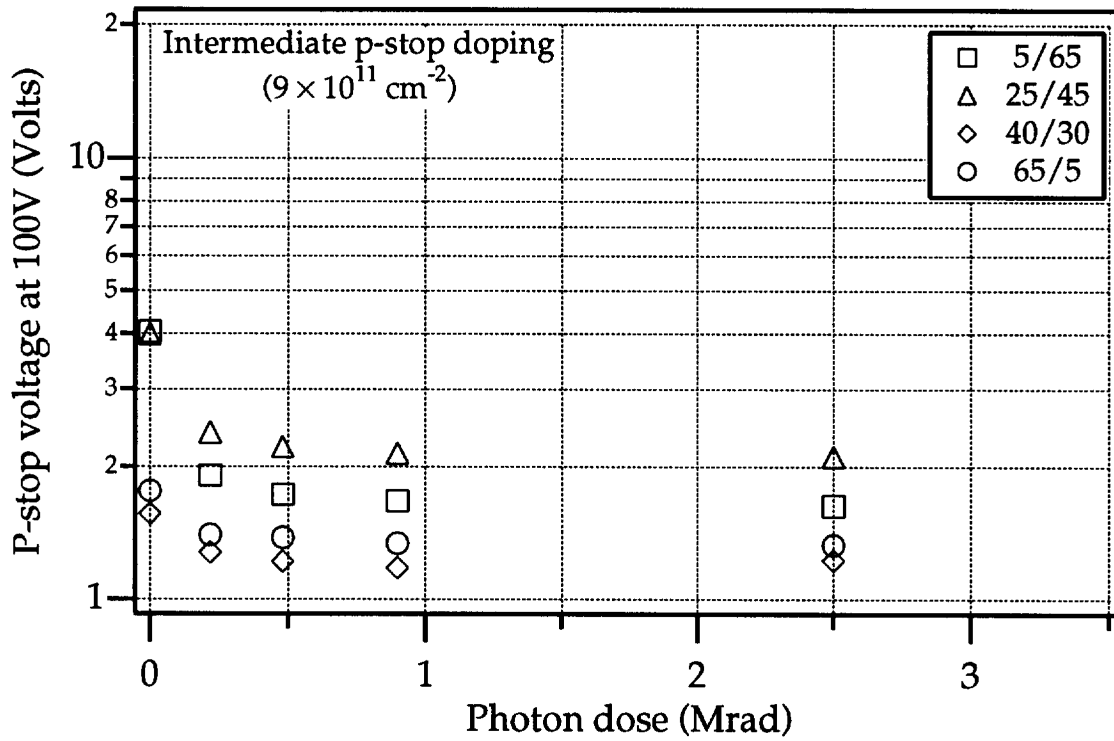


Figure 13(a) P-stop voltage vs gamma dose, 100μm pitch common p-stop strips, intermediate p-stop doping

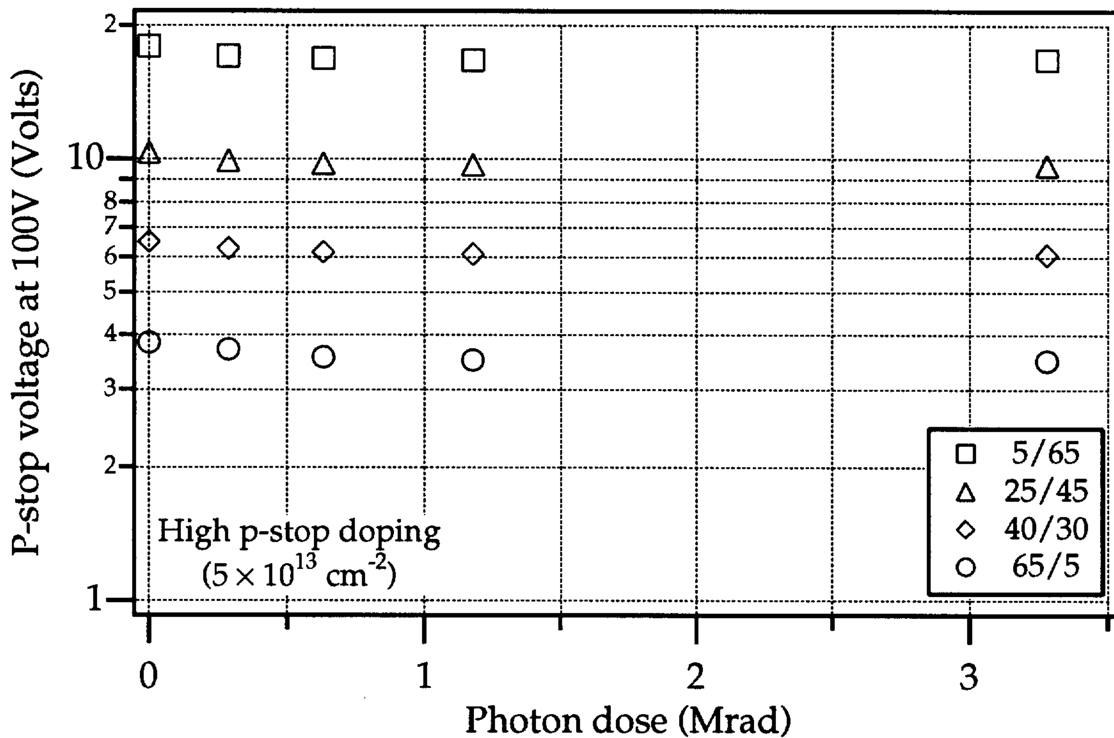


Figure 13(b) P-stop voltage vs gamma dose, 100μm pitch common p-stop strips, high p-stop doping

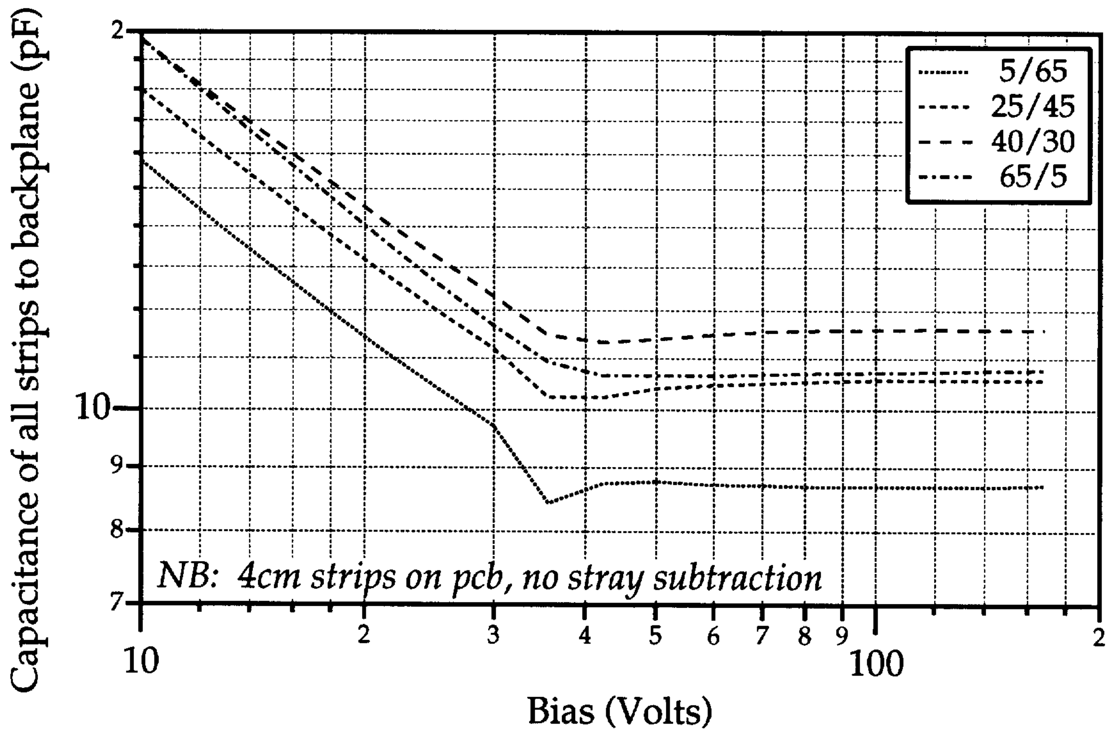


Figure 14(a) CV of 100μm pitch common p-stop strips to backplane, unirradiated

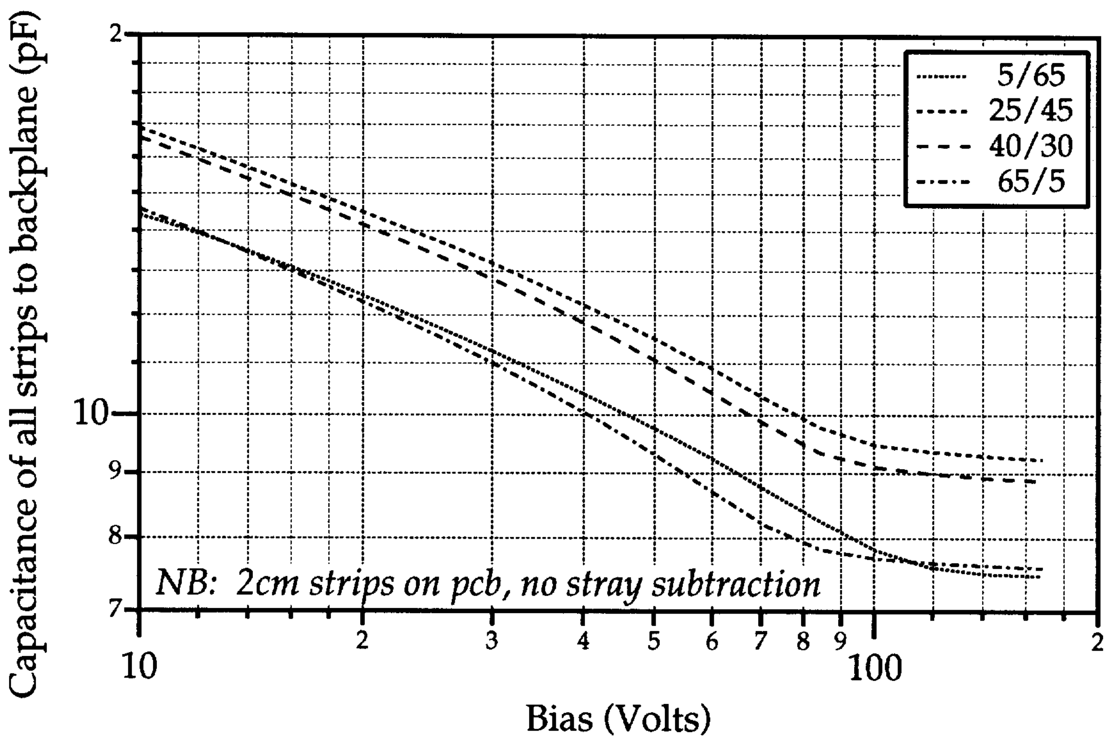


Figure 14(b) CV of 100μm pitch common p-stop strips to backplane, neutron irradiated beyond type inversion

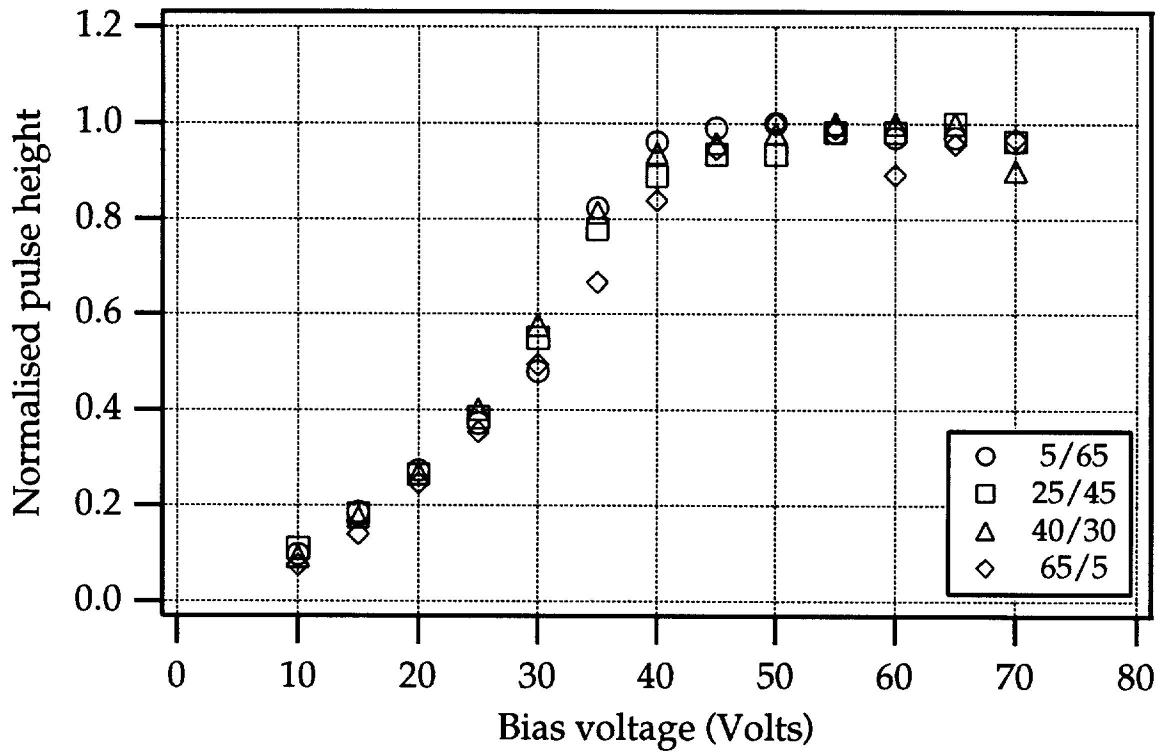


Figure 15(a) N-side strip pulse height vs bias for 100μm pitch common p-stop strips before type inversion

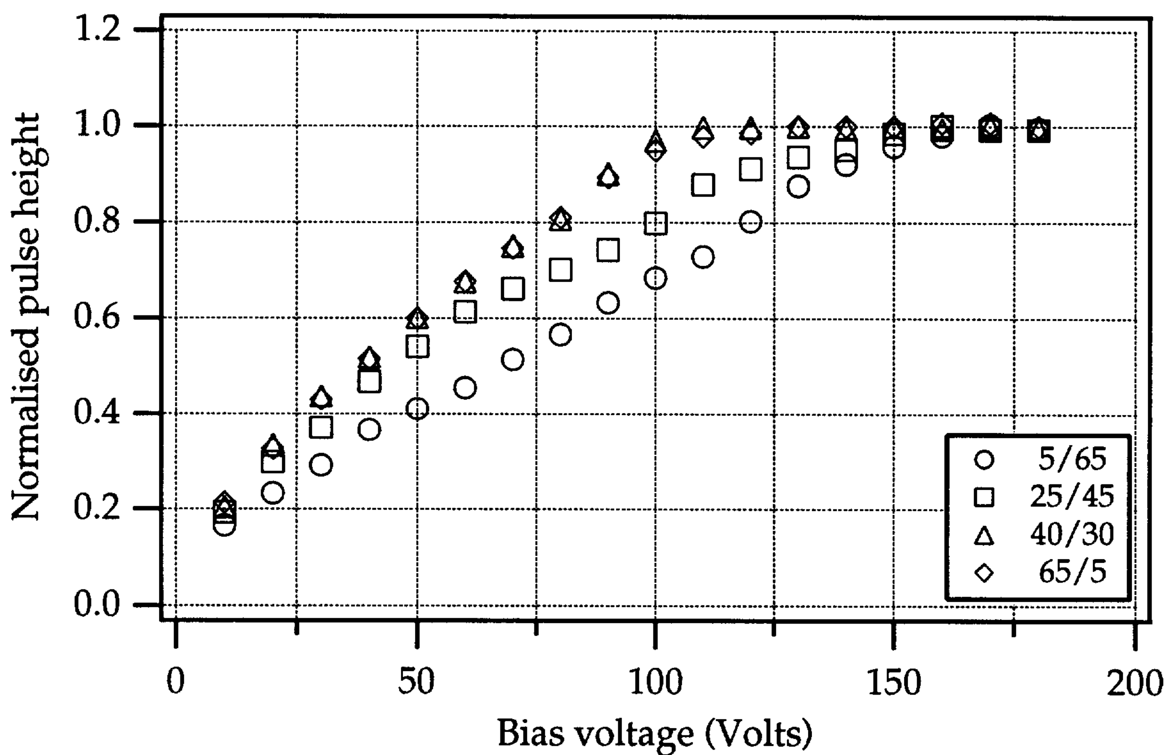


Figure 15(b) N-side strip pulse height vs bias for 100μm pitch common p-stop strips after type inversion

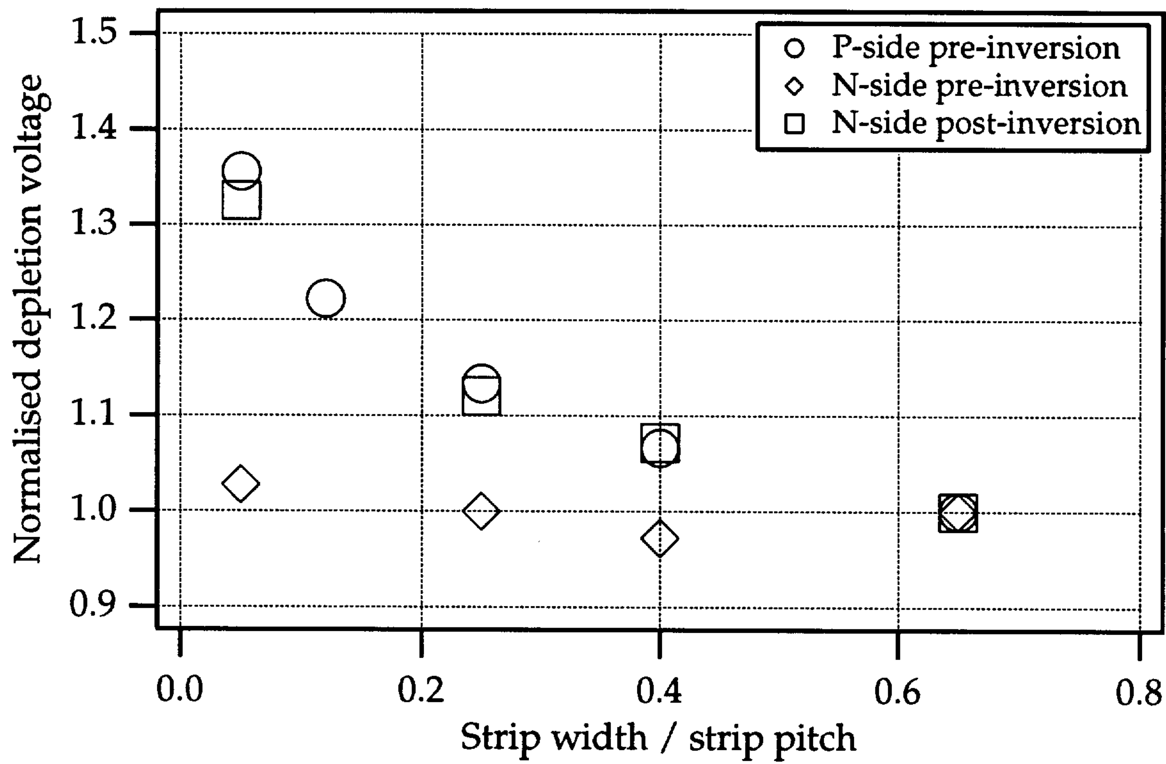


Figure 16 **Depletion voltage determined from CV curve for 100μm pitch common p-stop strips, both before and after type inversion, and similar geometry p-side strips**

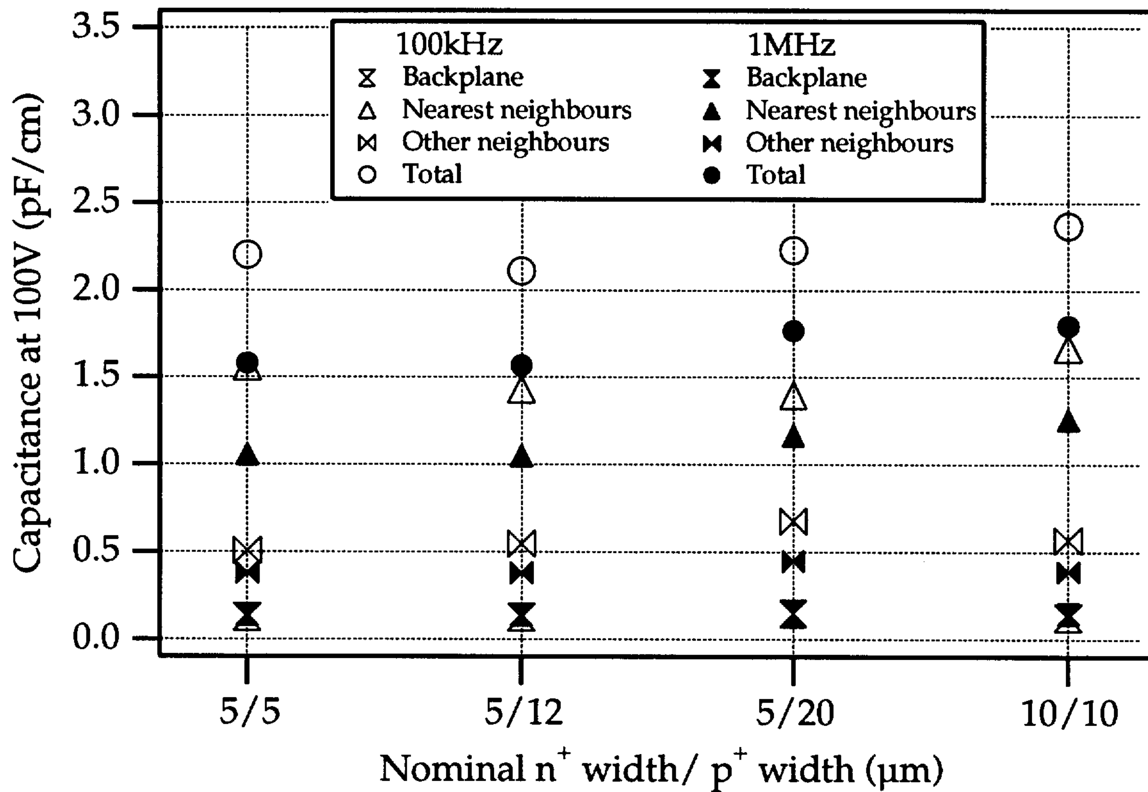
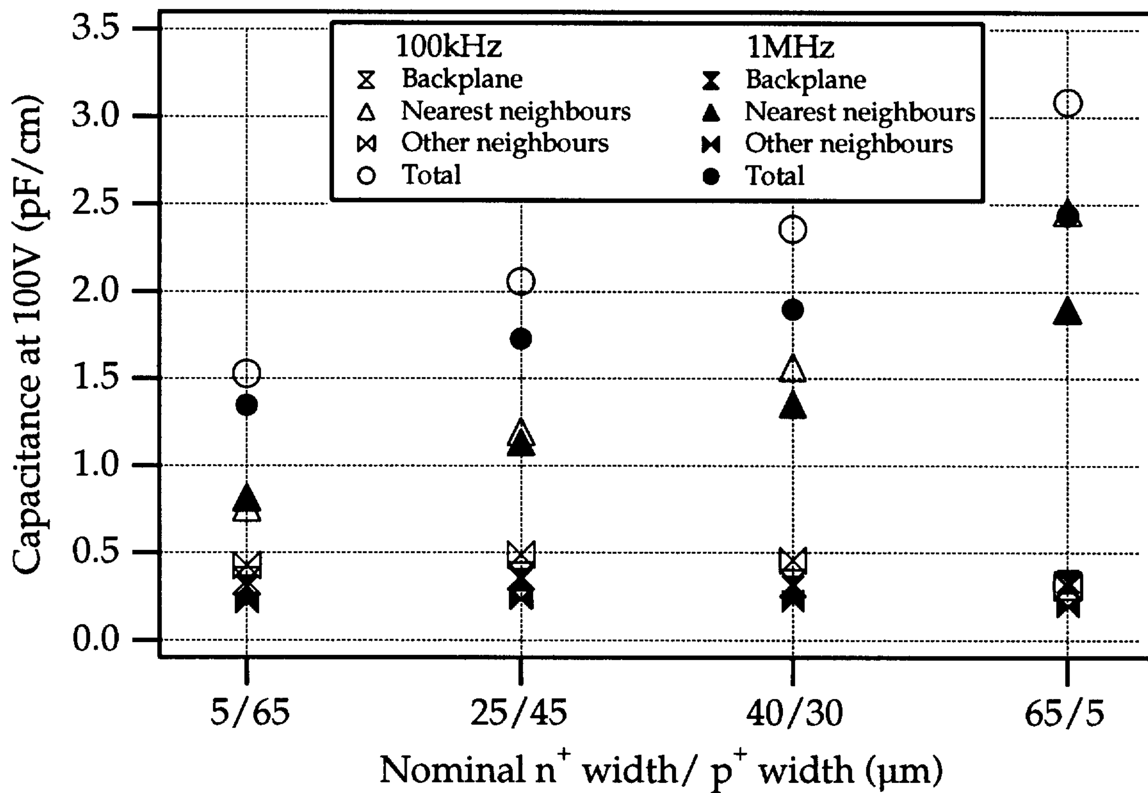


Figure 17(a) Capacitance at 100V of 50μm pitch common p-stop strips, high p-stop doping, unirradiated



17(b) Capacitance at 100V of 100μm pitch common p-stop strips, high p-stop doping, unirradiated

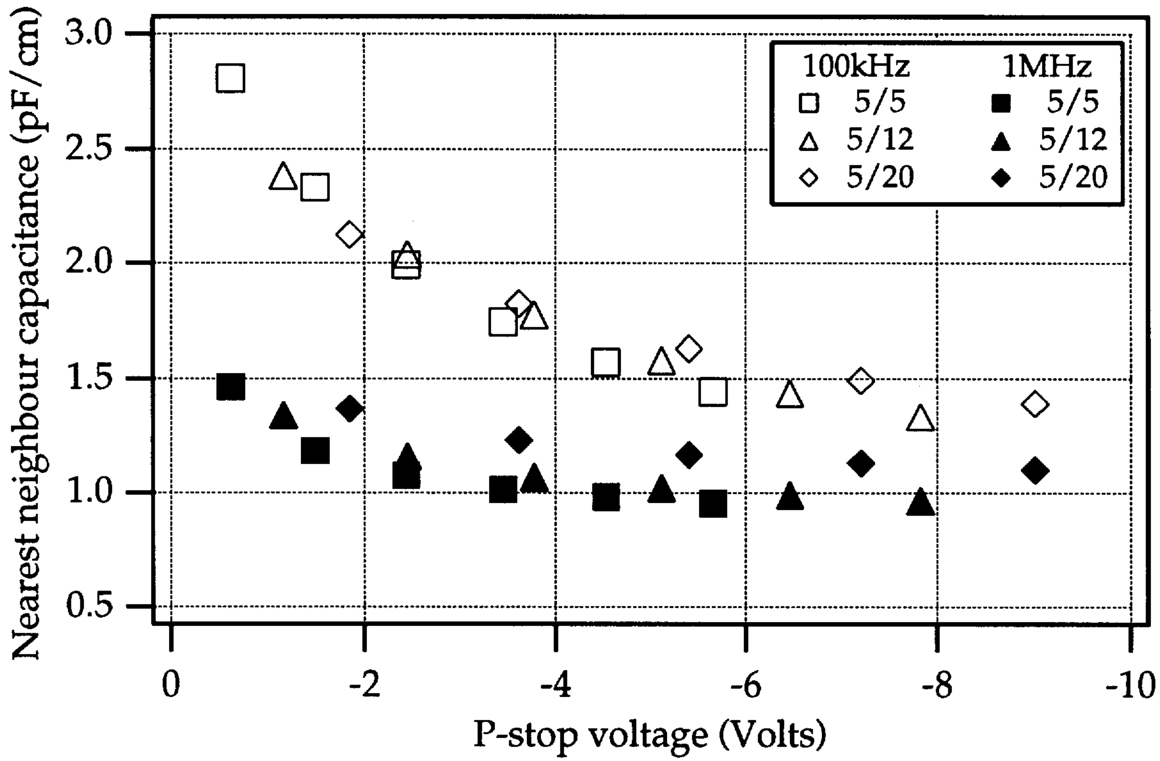


Figure 18(a) Nearest neighbour capacitance vs p-stop voltage, 50μm pitch common p-stops, high p-stop doping

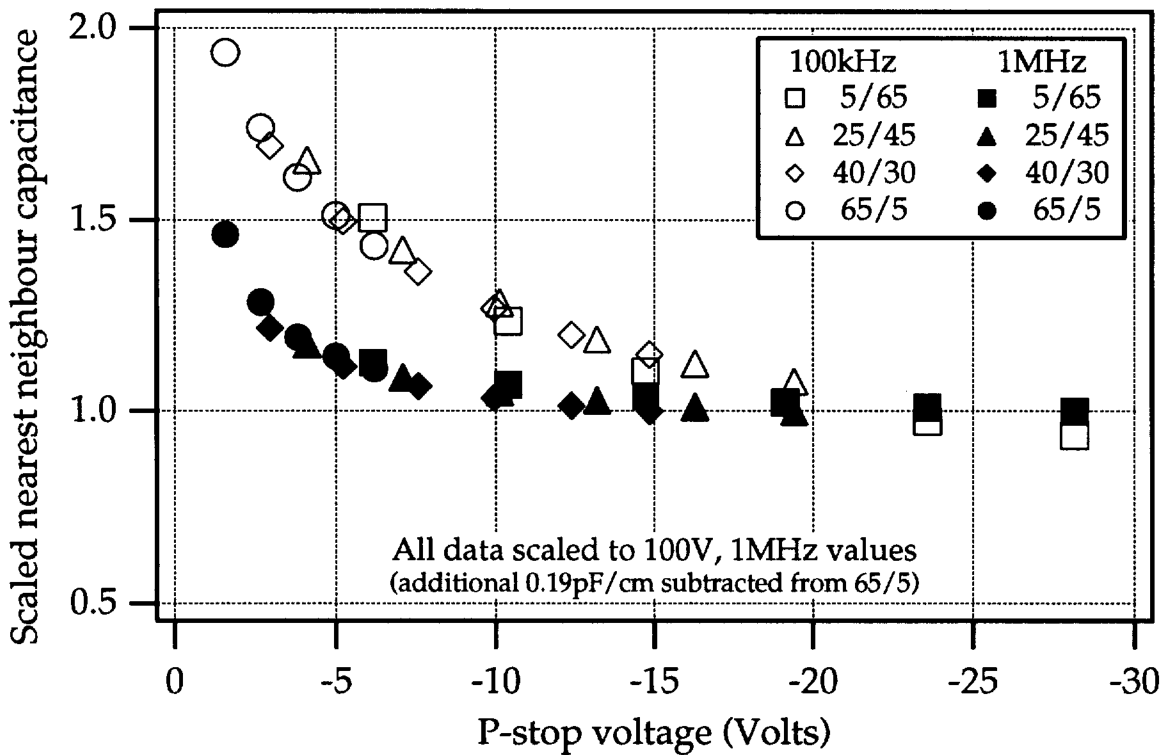


Figure 18(b) Scaled nearest neighbour capacitance vs p-stop voltage, 100μm pitch common p-stops, high p-stop doping

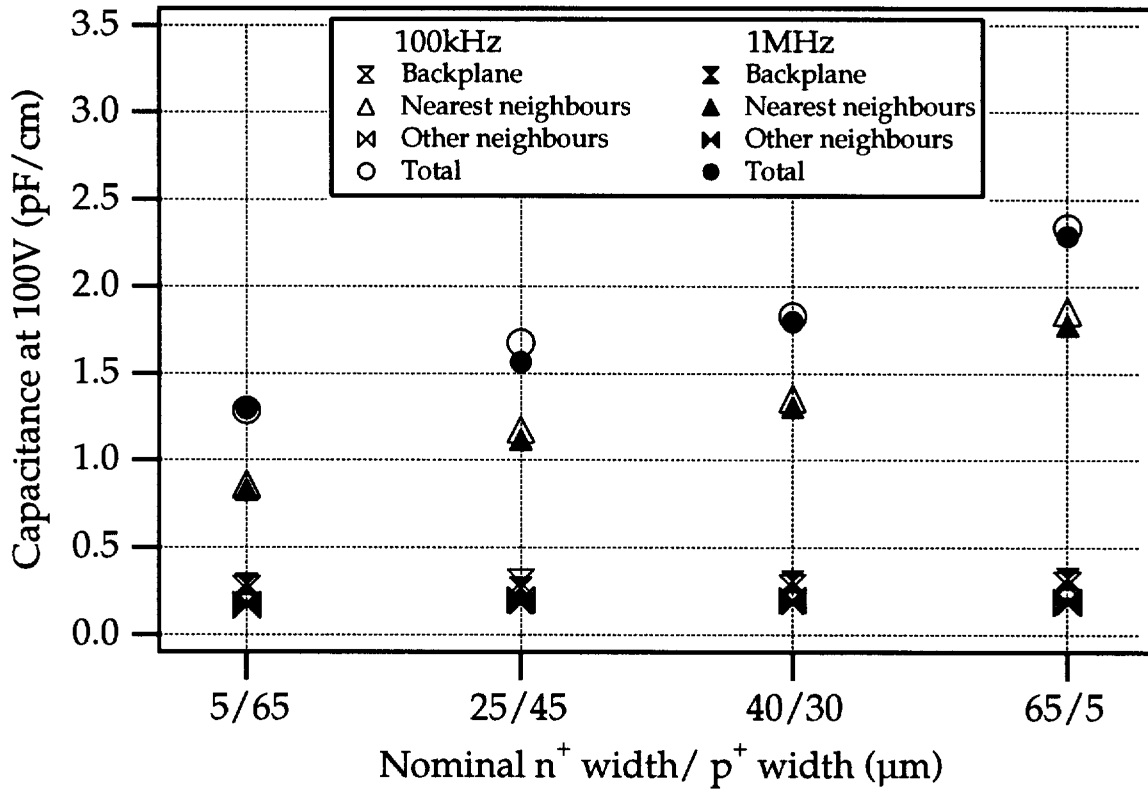


Figure 19 **Capacitance at 100V of 100μm pitch individual p-stop strips, high p-stop doping, unirradiated**

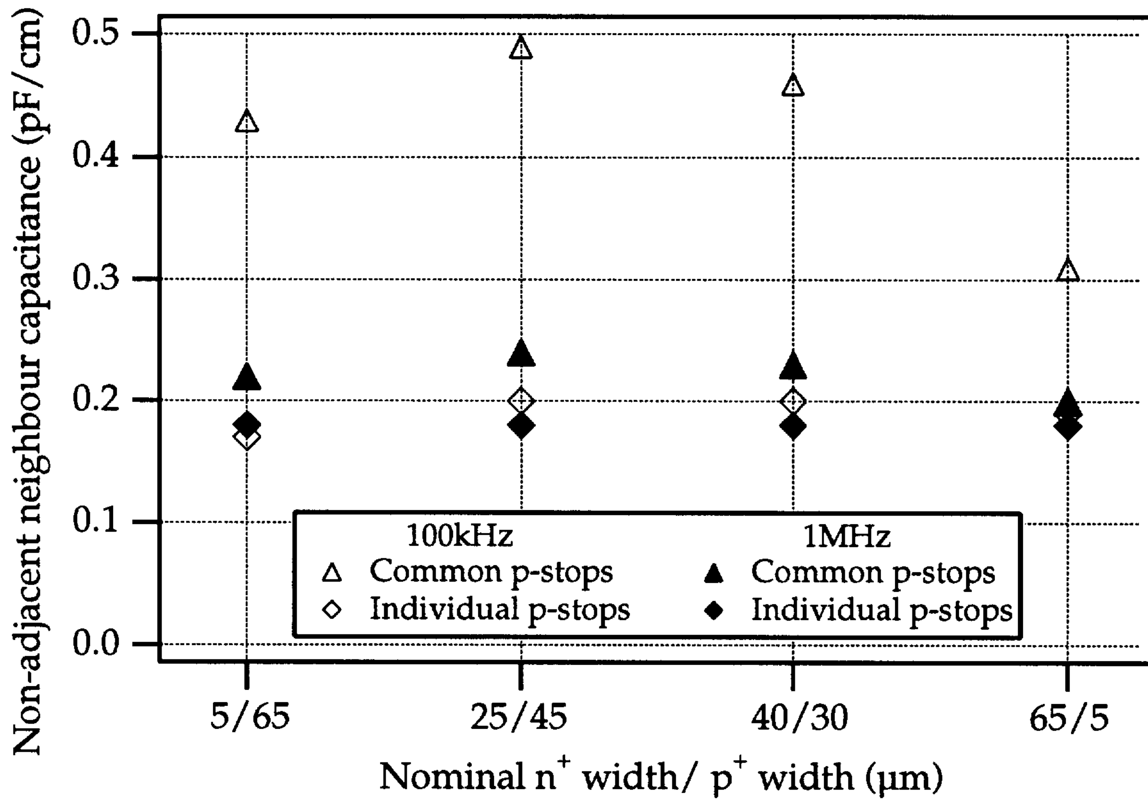


Figure 20 **Non-adjacent neighbours capacitance at 100V for common and individual 100µm pitch p-stops, high p-stop doping, unirradiated.**

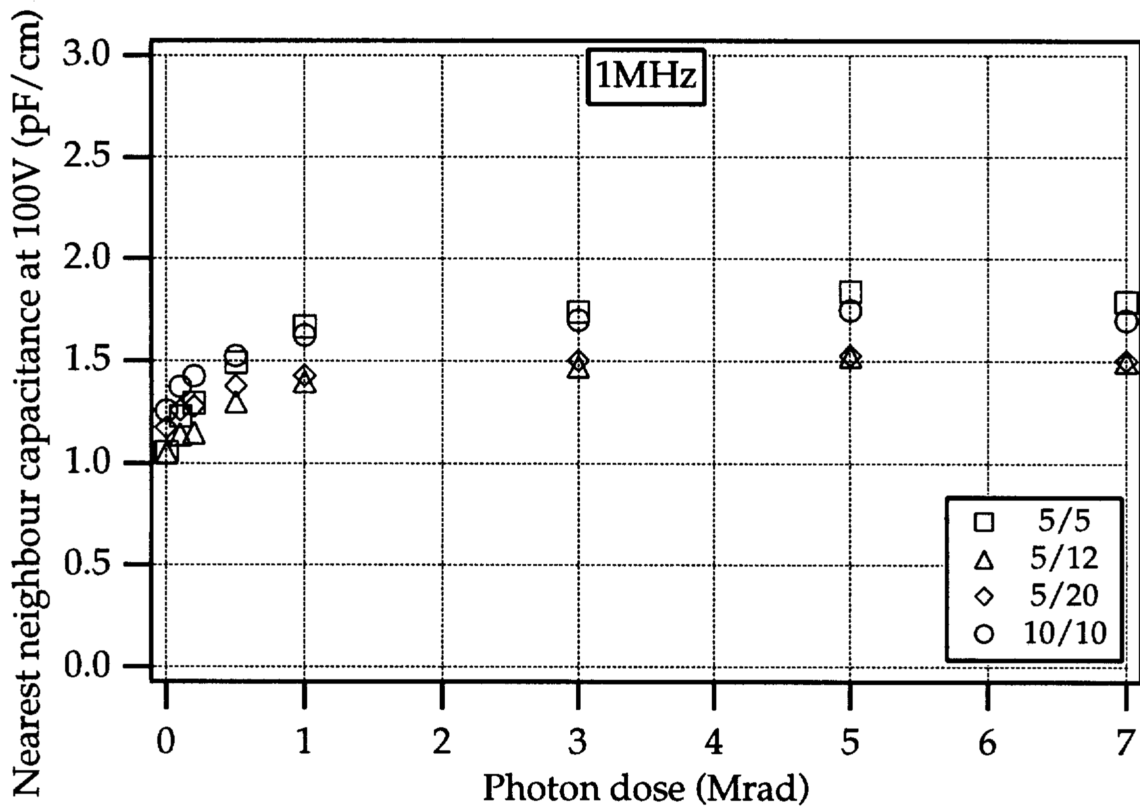


Figure 21(a) Capacitance at 100V, 1MHz vs photon dose, 50μm pitch common p-stops, high p-stop doping

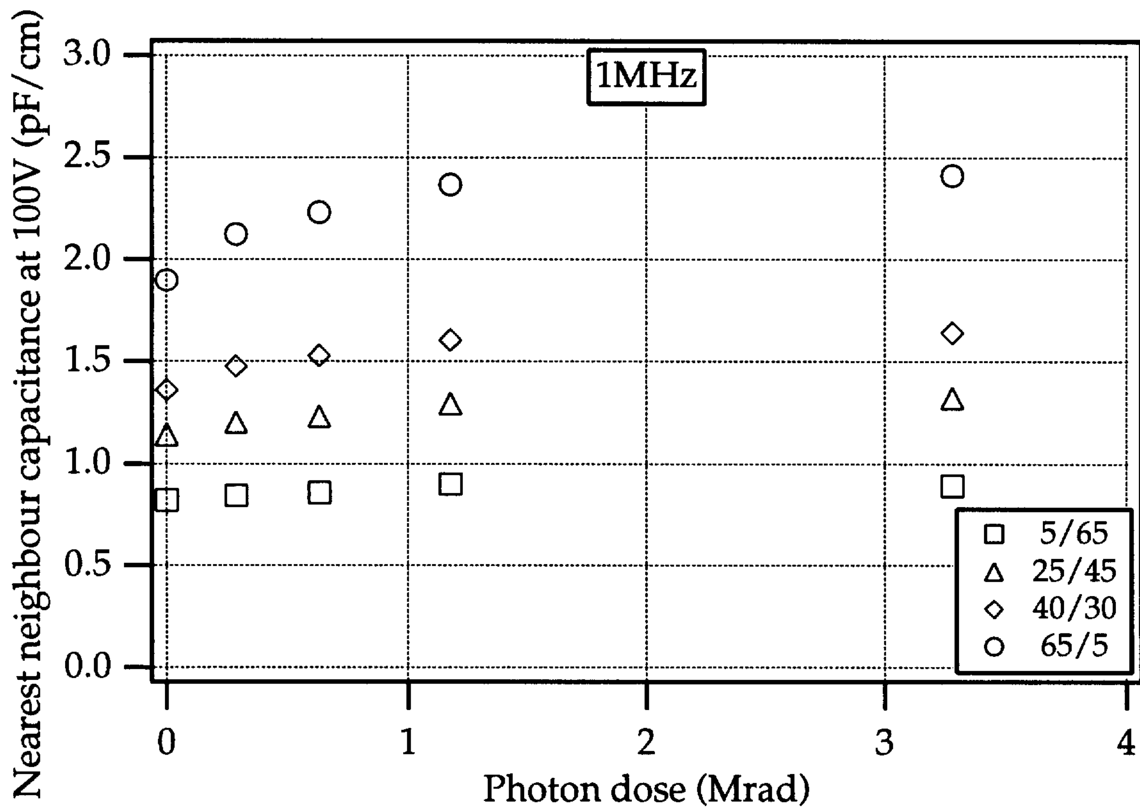


Figure 21(b) Capacitance at 100V, 1MHz vs photon dose, 100μm pitch common p-stops, high p-stop doping

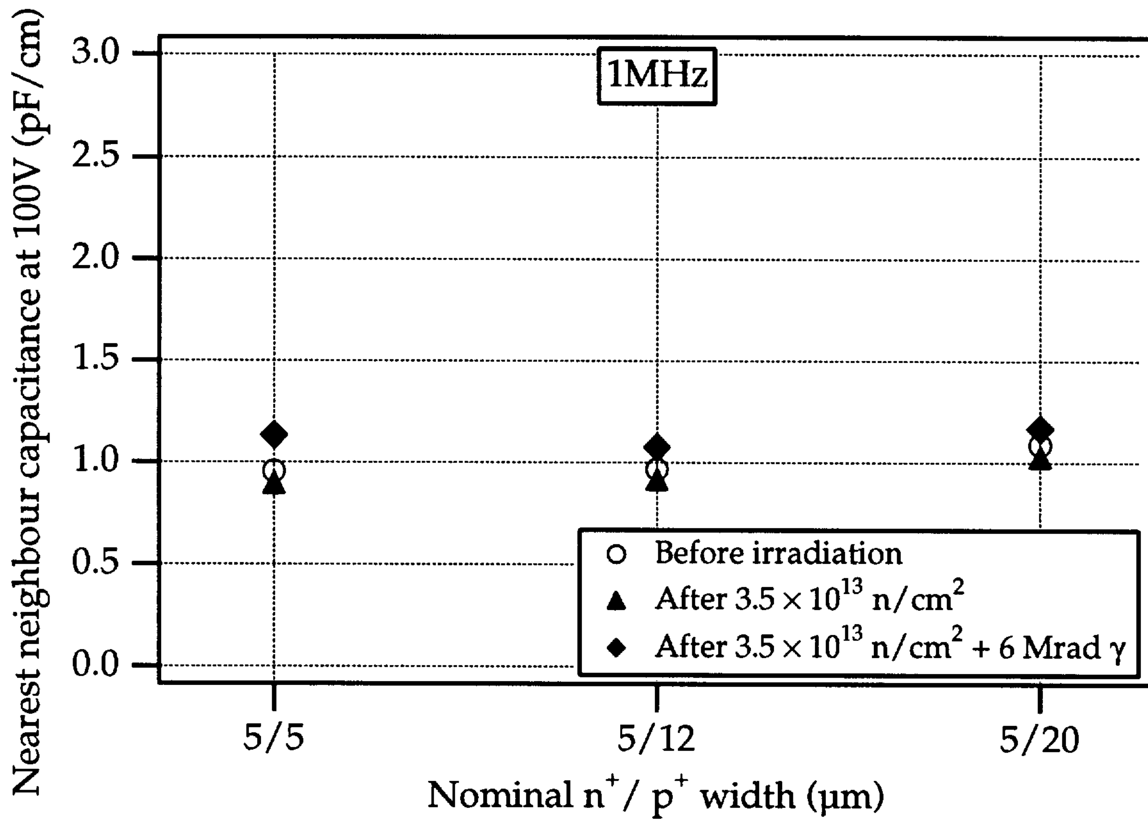


Figure 22(a) Nearest neighbour capacitance at 100V, 1MHz, 50μm pitch common p-stops, high p-stop doping, unirradiated, neutron irradiated, neutron + photon irradiated

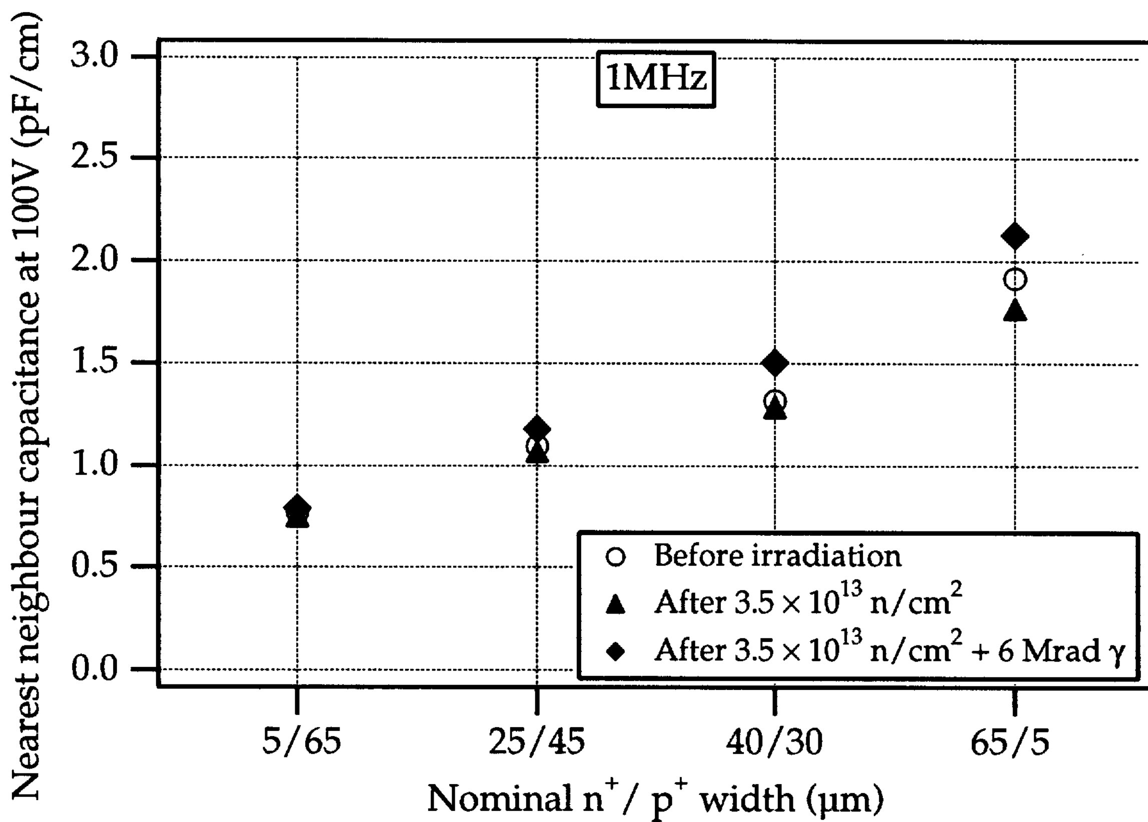


Figure 22(b) Nearest neighbour capacitance at 100V, 1MHz, 100μm pitch common p-stops, high p-stop doping, unirradiated, neutron irradiated, neutron + photon irradiated

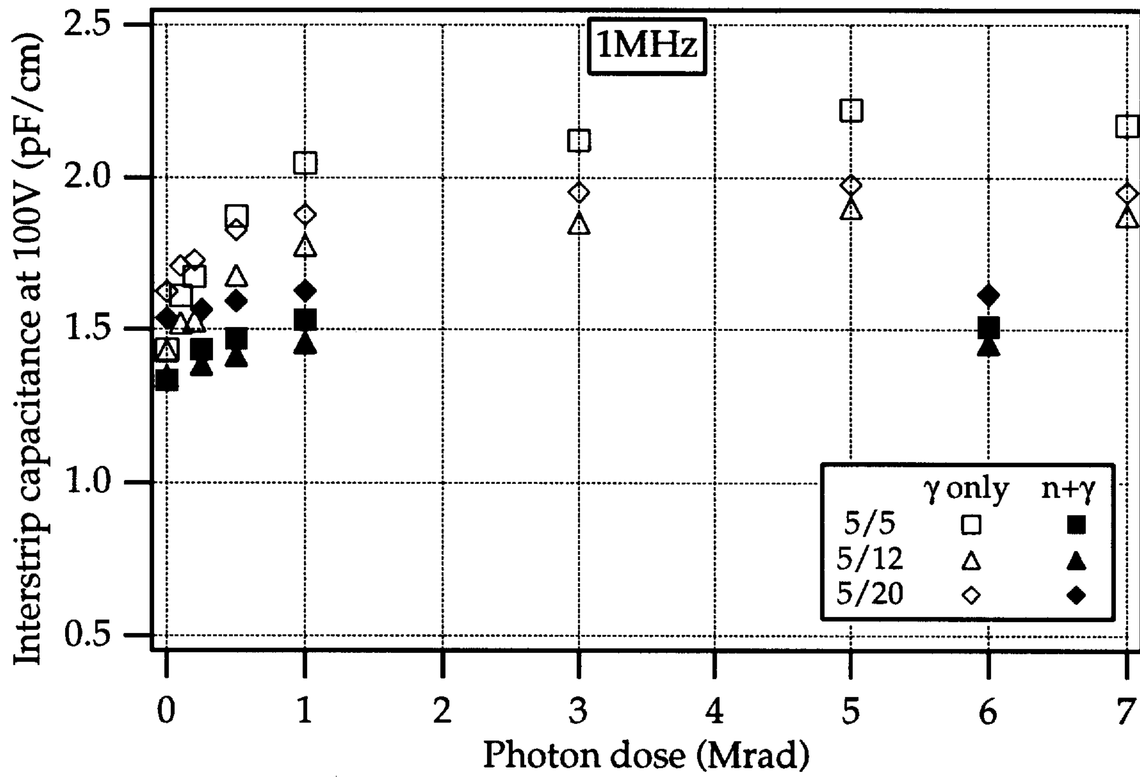


Figure 23 Variation of interstrip capacitance at 1MHz, 100V,with photon dose, for normal and neutron irradiated 50μm common p-stops, high p-stop doping.

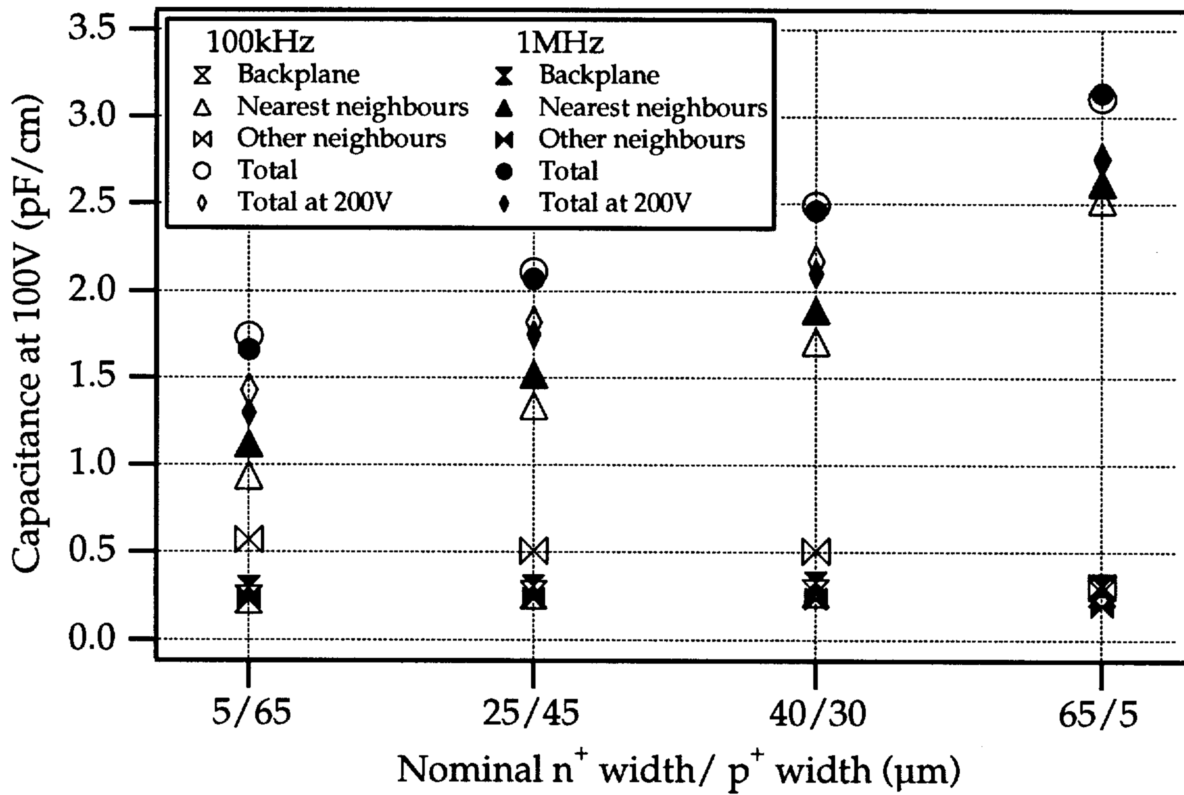


Figure 24(a) Capacitance at 100V for unirradiated 100μm pitch common p-stop Micron devices

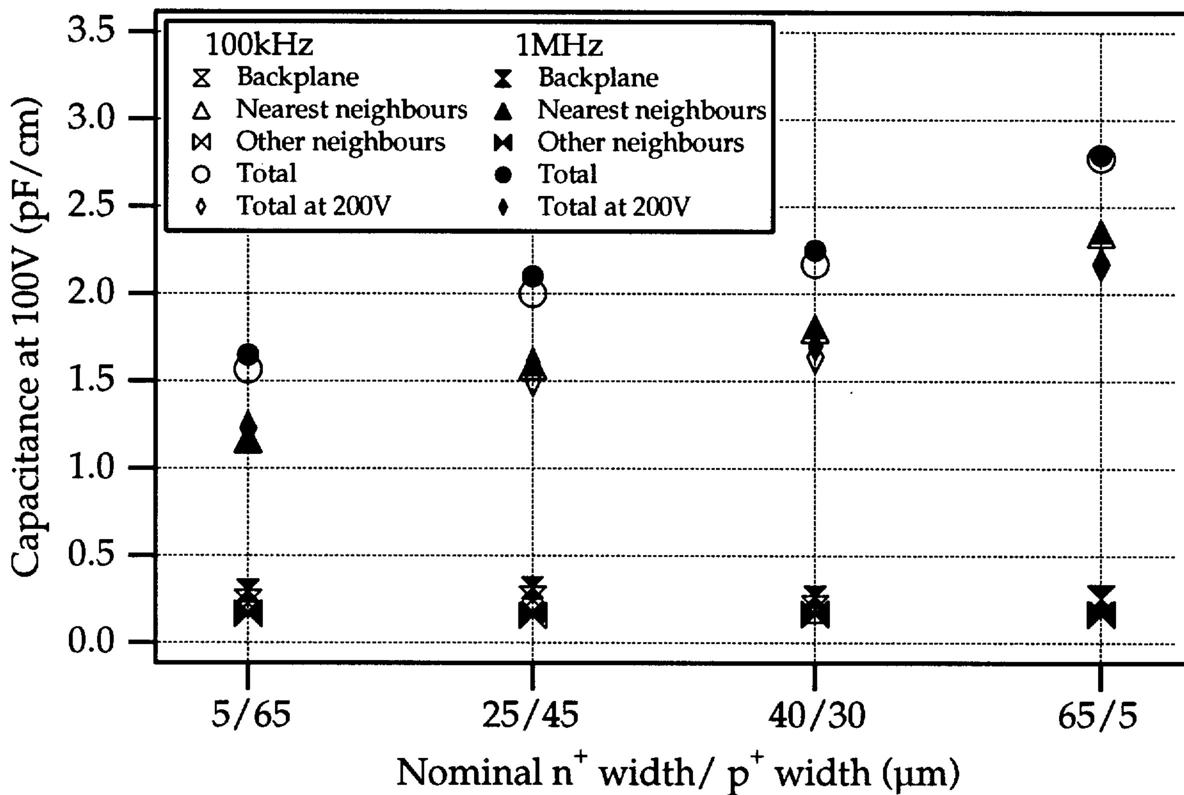


Figure 24(b) Capacitance at 100V for unirradiated 100μm pitch individual p-stop Micron devices

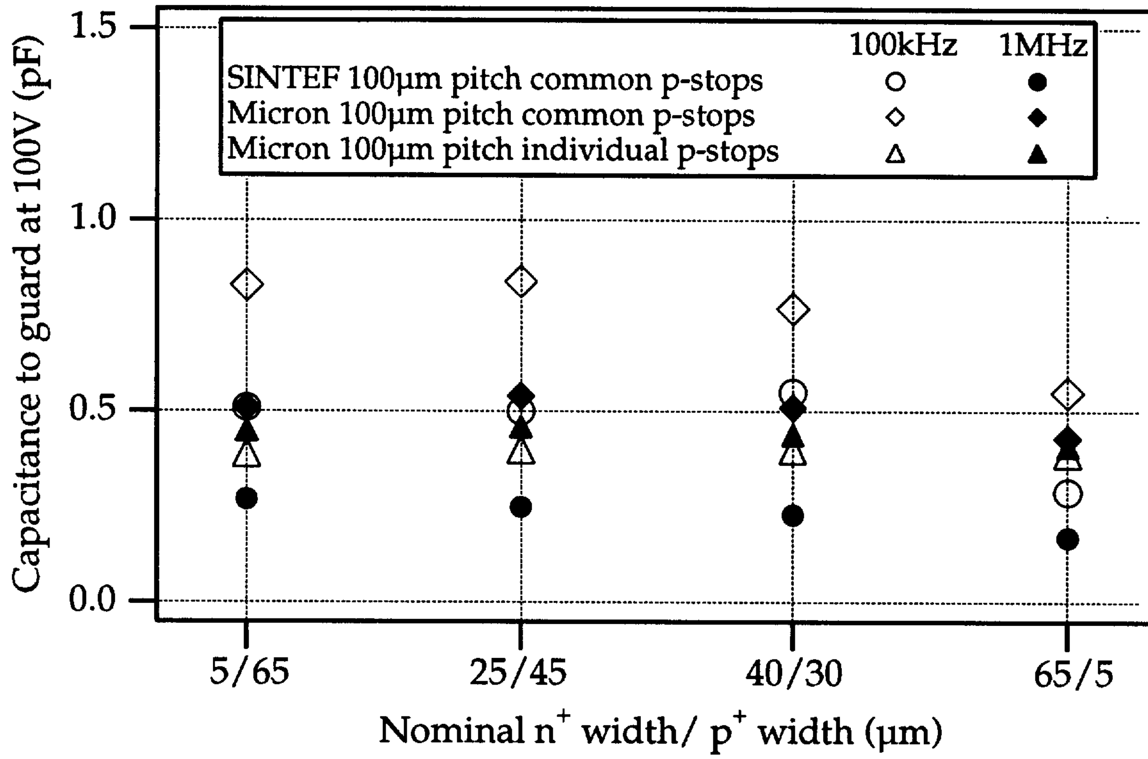


Figure 25 Capacitance to guard at 100V for unirradiated Micron devices and SINTEF devices