Upgrade of the RPC detectors data collection and transmission electronics for the ATLAS experiment at High Luminosity LHC

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ABSTRACT: Resistive Plate Chambers technology is used to trigger muon particles in the ATLAS Muon Spectrometer central region. The foreseen High Luminosity Large Hadron Collider operation imposes replacing their trigger and readout electronics with a Data Collector and Transmitter system, which implements an optical link (Low Power Gigabit Transceiver) to handle data bandwidth up to 10.24 Gb/s. A testing system has to be implemented to assess all Data Collector and Transmitter prototypes for the mass production. While the first Data Collector and Transmitter prototype was under fabrication, a methodology has been developed that renders feasible indispensable implementations towards the complete validation of the functionalities of the Data Collector and Transmitter and of any board that implements the Low Power Gigabit Transceiver optical link.

KEYWORDS: CERN; ATLAS experiment; LHC; Muon Spectrometer; RPC detectors; VHDL; FPGA;

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1. Introduction

The High Luminosity Large Hadron Collider (HL-LHC) will have an instantaneous luminosity 7.5×10^{34} $cm^{-2}s^{-1}$ well above the original LHC design value of 10^{34} $cm^{-2}s^{-1}$, resulting in higher data rates and radiation levels that will pose significant challenges to both the experiments' detectors and the readout and trigger electronic systems.

To preserve the acceptance of critical signatures for physics, the trigger system of the ATLAS experiment [1] has to maintain both low-momentum trigger thresholds and manageable trigger rates. Hence, it will undergo a decisive upgrade (Phase II upgrade) by increasing the trigger rate and latency to 1 MHz and 10 μs, respectively, so that more complex trigger algorithms than in the present system can be feasible [2]. This trigger scheme renders the current readout and trigger electronics obsolete, which accommodate a maximum rate of 100 kHz with a maximum latency of up to 3 μs, therefore the upgrade of the electronics is necessary.

This work refers to the Phase II upgrade of the trigger electronics system in the central region (barrel) of the ATLAS Muon Spectrometer [3], that will play a vital role in exploiting the HL-LHC physics potential. It focuses on the radiation resistant Data Collector and Transmitter (DCT) boards that will replace the on-detector readout and trigger electronics of the Resistive Plate Chambers (RPC) used mainly to trigger muons in the central part of the Muon Spectrometer.

Due to the importance of the DCT system, the complexity of the signals it handles, and the large number of boards required (1570 DCTs), an automated test station has to be developed to evaluate the performance of all its functionalities. Towards this end, a test bench has been developed to assess the Low power Gigabit Transceiver (LpGBT) optical link of the DCT boards.

2. The RPC detector system upgrade

The ATLAS Muon Spectrometer is arranged in three concentric cylinders of muon stations around the beam axis (barrel region) (Figure 1) and three parallel layers of muon stations on both sides of the barrel, perpendicular to the beam axis (end-caps). Both barrel and end-caps consist of an

inner (I), middle (M), and outer (O) region, equipped with different detector technologies. Two detector technologies are employed mainly to trigger muon particles; the barrel's resistive plate chambers (RPC) and the Thin Gap Chambers (TGC) in the end-caps, respectively. An RPC detector consists of two sensitive gas gaps that produce pulses caused by the incident charged particles of typical 0.5 pC. The readout of the signals is performed via capacitive coupling by metal strips on both sides of each chamber, providing two position coordinates measurements. As illustrated in Figure 1, the ATLAS RPC system consists of three RPC layers. Two RPCs are mounted on the middle layer of MDT chambers (BM) and the third one on the outer (BO) MDT

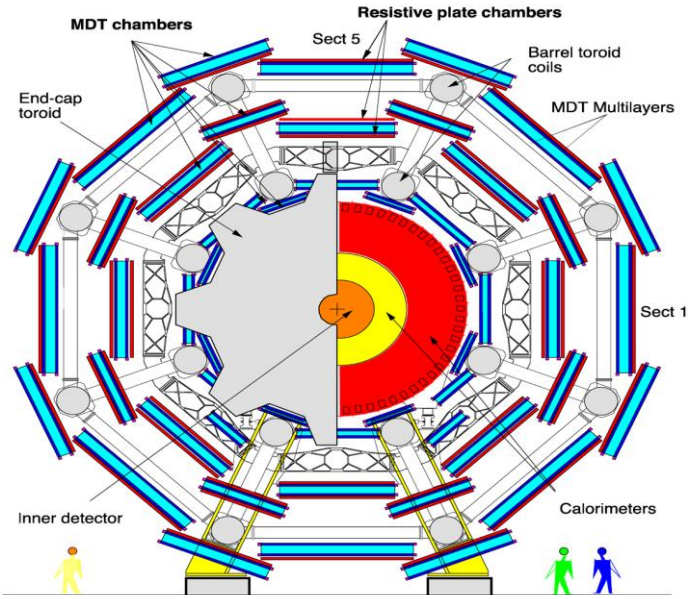

Figure 1. A view of the present ATLAS muon spectrometer barrel layout in the plane transverse to the beam axis [4].

layer. Currently, there are no RPC detectors in the inner barrel layer. For the Phase II Muon upgrade, a new inner layer (BI) of RPC triplet detectors will be installed that provide a more redundant trigger system and will cover the "blind spots" of the toroid magnet supports, increasing the acceptance from 75% to 95%.

The new BI RPC layer will provide higher rate capability (kHz/cm^2), a longer lifespan (more than ten years at HL-LHC conditions), a better spatial resolution (less than 1 cm), and a better time resolution of about 0.5 ns.

3. The RPC electronics upgrade

The current RPCs' electronics consist of Front-End boards (FEs) using the legacy ASD ASIC which amplifies and discriminates the signals from the RPCs' strips and trigger/readout boxes. These trigger boxes implement the lower-level trigger logic and host the buffers that store the data for readout upon a trigger acceptance. A new high-gain and low-noise FE ASIC [3] for the

BI layer, which integrates the amplifier, discriminator, TDC, and serializer is under development. The first pre-prototype of this ASIC is already fabricated and tested.

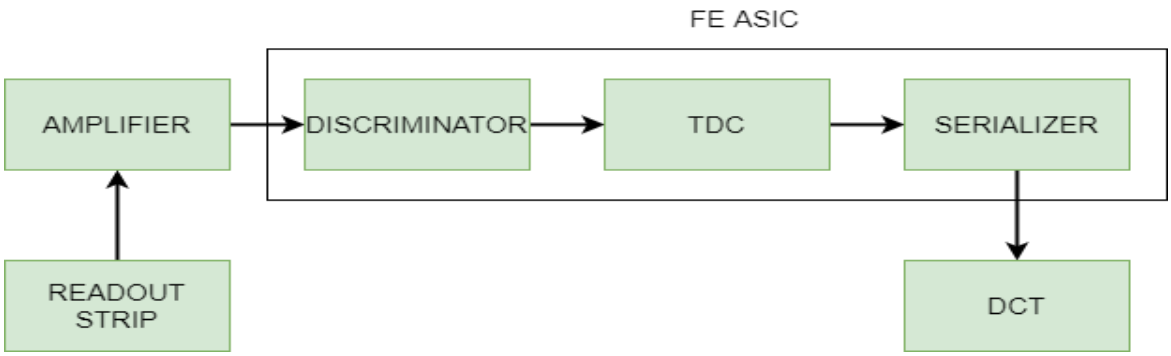

Figure 2. A simplified block diagram of the new FE ASIC [3].

4. The RPC Data Collector and Transmitter (DCT) board

The DCT boards will replace the current RPC trigger/readout boxes. The DCT resides on the detector, samples hit data from up to 36 FE boards, and sends zero-suppressed data to the off-detector barrel Sector Logic (SL) boards that implement the trigger and readout logic (Figure 3). Two different DCT variants will be produced: one for the BM/BO region, where the TDC will be implemented in the FPGA of the DCT with 800 ps time resolution, and the one for the BI region where the TDC will be implemented by the new FE ASIC. In total, 1570 DCT boards will be used.

The two key components for the functionality of the DCT are the LpGBT [5], that handles the bi-directional optical communication with the SL, and a Xilinx ARTIX-7 (XCA200T) FPGA, that handles the RPC hit data. The LpGBT ASIC offers an uplink (DCT to SL) bandwidth of 10.24 Gb/s with a user bandwidth of 8.96 Gb/s using the FEC5 coding.

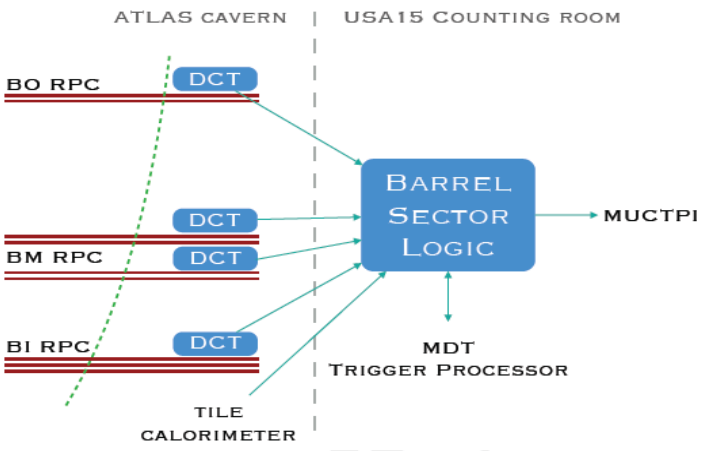

Figure 3. A simplified scheme of the Phase II RPC readout and trigger system.

The uplink user data consists of; 27 E-links at 320 Mb/s for the RPC hit data from up to 288 readout strips; one E-link at 320 Mb/s for monitoring the on-board parameters such as: temperatures, voltages, hit rates and SEU events, one Slow Control (SC) E-link at 80 Mb/s for the monitoring of the LpGBT core and its GPIO port. The downlink (SL to DCT) bandwidth is 2.56 Gb/s with a user bandwidth of 1.28 Gb/s. The downlink user data consists of; one E-link at 320 Mb/s for the TTC signal; one E-link at 320 Mb/s for configuration commands to the FPGA firmware, one SC E-link for the configuration of the LpGBT and the firmware upload to the FPGA through the GPIO port.

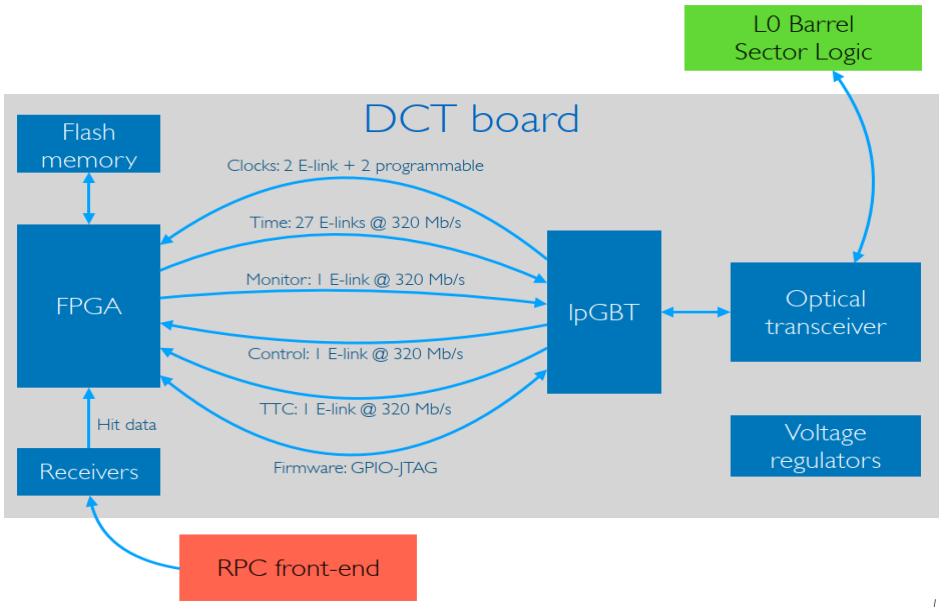

Figure 4. Block diagram of the DCT prototype.

5. The testing of the DCT

For the prototype and the mass production testing of the DCT a test bench is under development. This test bench should be able to emulate both the communication with the FEs and the SL. The key component for the test bench is the LpGBT-FPGA, a firmware which provides the back-end counterpart of LpGBT, designed by the GBT-project at CERN. The LpGBT-FPGA core comes as a couple of modules without MGT instantiation. Development of new firmware was needed to implement the design to a Xilinx VC709 development board. Since the DCT prototype is under fabrication, and loopback tests of the LpGBT-FPGA are not possible due to asymmetry of its downlink and uplink data rates, the tests were performed by using a customized version of the LpGBT-Emulator, a firmware implementation of the LpGBT ASIC.

The test configuration (Figure 5) consists of two VC709 boards, one for the LpGBT-FPGA and one for the LpGBT-Emulator, connected through an optical fiber. Fixed pattern or PRBS7 data were transmitted from the LpGBT-FPGA, received by the LpGBT -Emulator and checked for errors (and vise versa). For a 48 hour continuous run with PRBS data, zero errors were detected with a resulting Bit Error Ratio (BER) of 1.8×10^{-14} for each E-link.

Additionally, the same test was performed with fixed pattern data for 72 hours without any errors, with a resulting BER of 1.2×10^{-14} for each E-link.

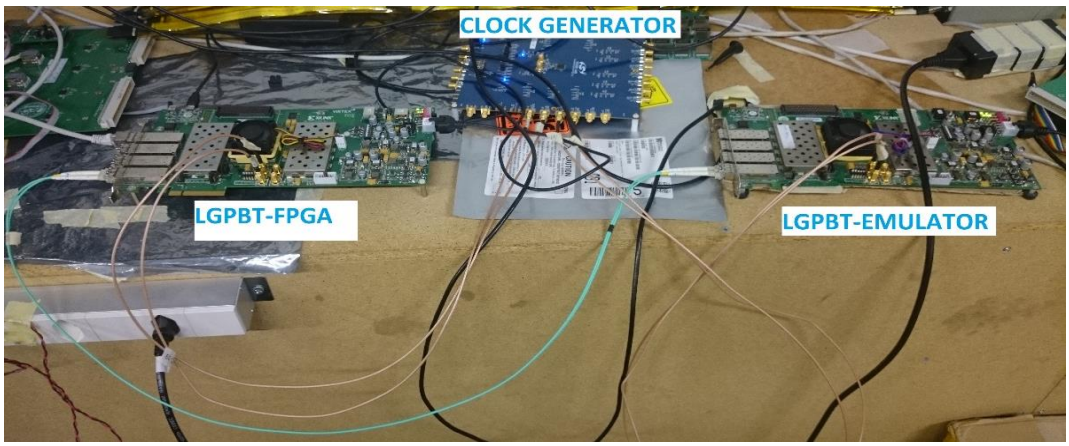

Figure 5. LpGBT-FPGA testing setup.

6. Conclusions

The rate and latency requirements of the Phase-II ATLAS trigger system are incompatible with the current RPC on-detector trigger and readout electronics. Therefore the trigger and readout scheme will be upgraded including the DCT on-detector boards. Additionally, the DCT boards will be also used in the new BI RPCs that will be installed as part of the Phase-II upgrade. In total, 51 DCTs per sector will be used along with 32 SL boards. The DCT is an FPGA-based board controlled by the off-detector barrel SL board, which sends and receives data to/from the DCT through a bi-directional fiber. The DCT board is at the prototype development phase, with the first prototype recently fabricated. In advance of the prototype fabrication, a test bench has been under development with the purpose of perfoming extensive tests during the prototyping phase of the DCT and, later on, to provide a standardized method of testing for the mass production phase. To this purpose the LpGBT-FPGA is utilized to emulate the communication with the SL and the LpGBT-Emulator to emulate the functionality of the LpGBT ASIC.

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