UNIVERSITY OF TEXAS ARLINGTON

Demonstrator system for the high-luminosity upgrade of the ATLAS hadronic Tile Calorimeter electronics

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On behalf of the Tile Calorimeter Upgrade Team

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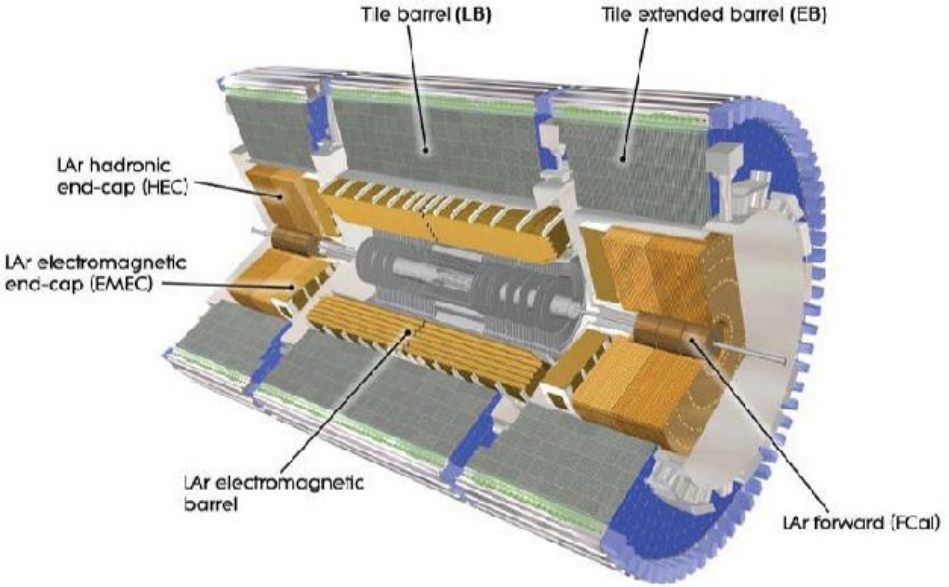
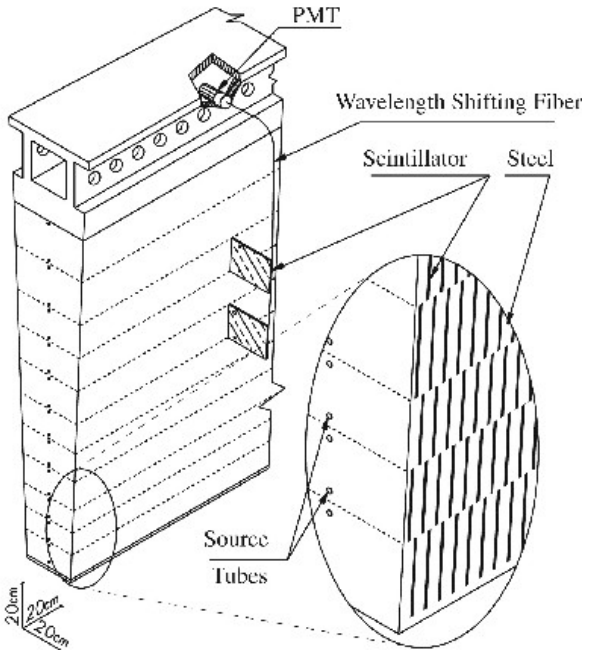
Tile ATLAS Tile Calorimeter





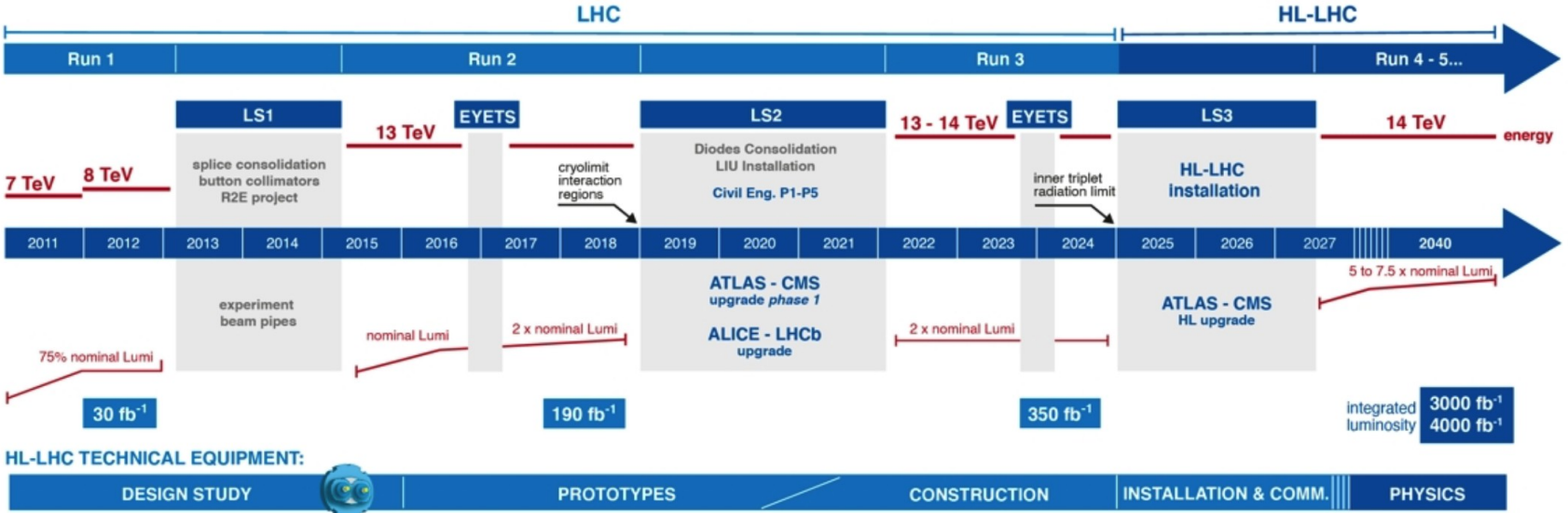
- Measures hadronic energy and Missing Transverse Energy
- Segmented calorimeter of steel plates and plastic scintillators tiles
- 2 WLS fibers per tile
- 2 PMTs per cell
- Granularity (eta, phi) 0.1 x 0.1 for the two inner radial layers (A, BC), 0.1 x 0.2 for the outer radial layer (D)

- Coverage: |eta| < 1.0 (LB)

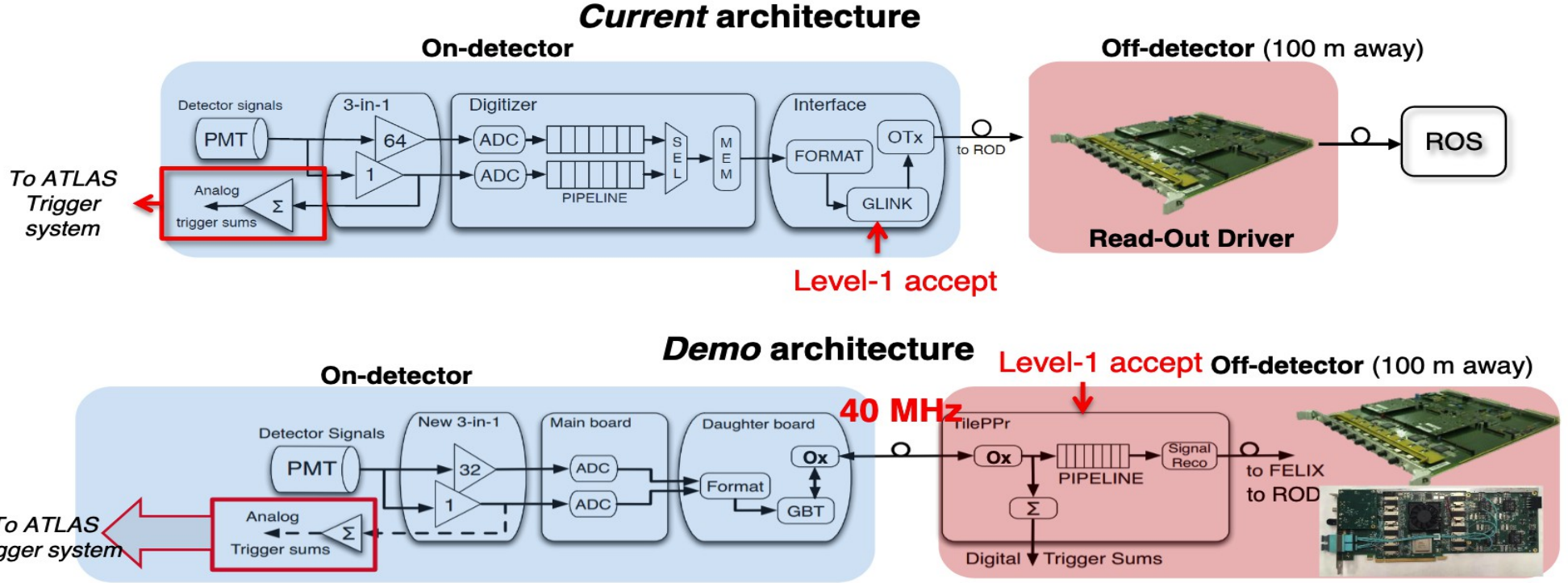
  0.8 < |eta| < 1.7 (EB)
- Resolution $\frac{\sigma}{E} = 50\%/\sqrt{E} \oplus 3\%$
- 4 readout partitions
- Each partition has 64 modules
- About 10k readout channels

Tile Phase-II Upgrade for HL-LHC

- Complete replacement of on-detector and off-detector electronics
  - To be compatible with full digital TDAQ and trigger processing at 40 MHz and to fulfill Phase-II radiation requirements
  - And due to radiation and time aging (20x higher than legacy)
  - Moreover redundancy in data links and powering will be granted
- About 10% of the most exposed PMTs will be replaced due to radiation and time aging
- Upgrade of LVPS system to reduce single point failure: one DC/DC converter powers 1/8th of a Tile module
- Regulated High Voltage to be distributed remotely from off-detector



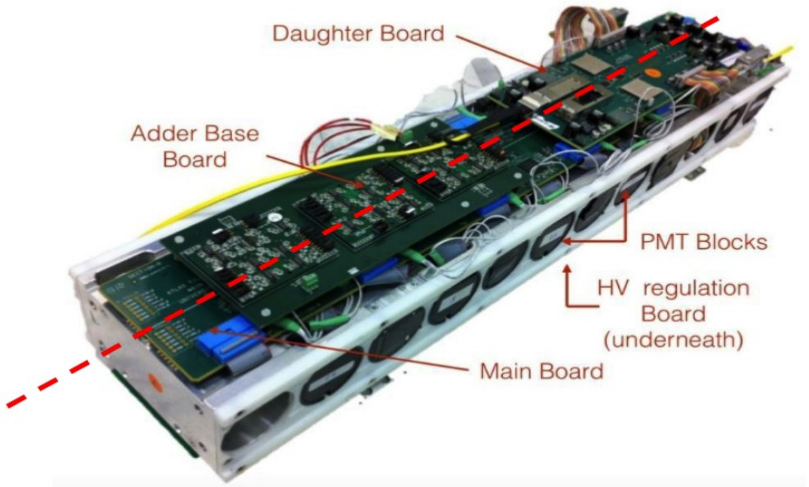
Demonstrator Readout Architecture

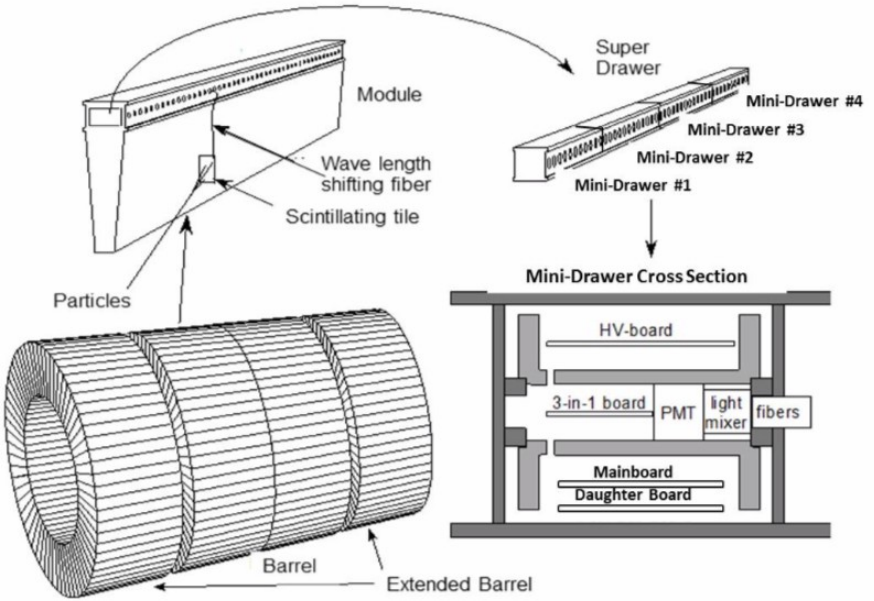


- Clock and readout architecture as for HL-LHC
- On-detector electronics transmit full digital data at 40 MHz
- Memory buffer are moved to off-detector electronics
- Redundancy in data links and power distribution
- LHC clock distribution through high-speed links from PreProcessor
- Keeps backward compatibility with current TDAQ system

Demonstrator Module

- Long Barrel module with four MiniDrawers (MDs) powered by one Low Voltage Power Supply
- Each MD has 2 independent sections for redundant readout
  - 12 PMTs and 12 Front-End Boards (FEBs) to read 6 cells
  - 1 adder board with up to 3 adder cards
  - 1 MainBoard and 1 DaughterBoard
  - 1 HV distribution board



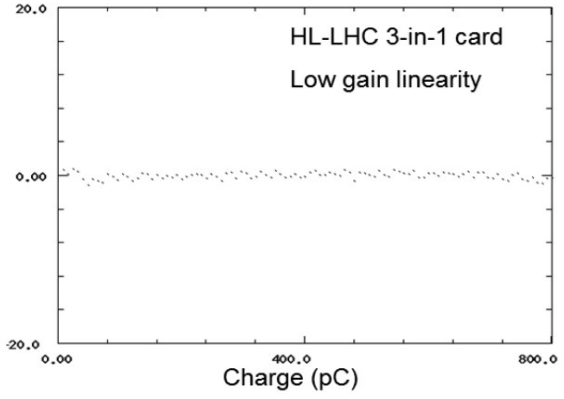


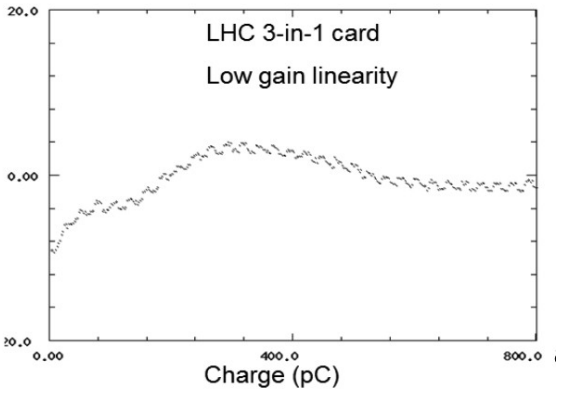
Active dividers and FEBs

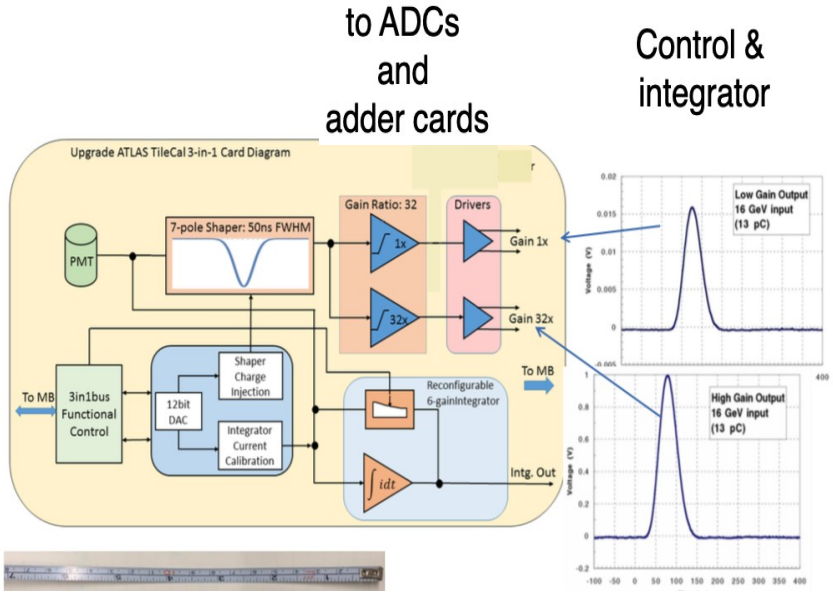
HV for PMT dynodes through transistors (active dividers).
Good linearity up to 100uA current

Front-End-Boards: Based on the well understood 3-in-1 card of the legacy system

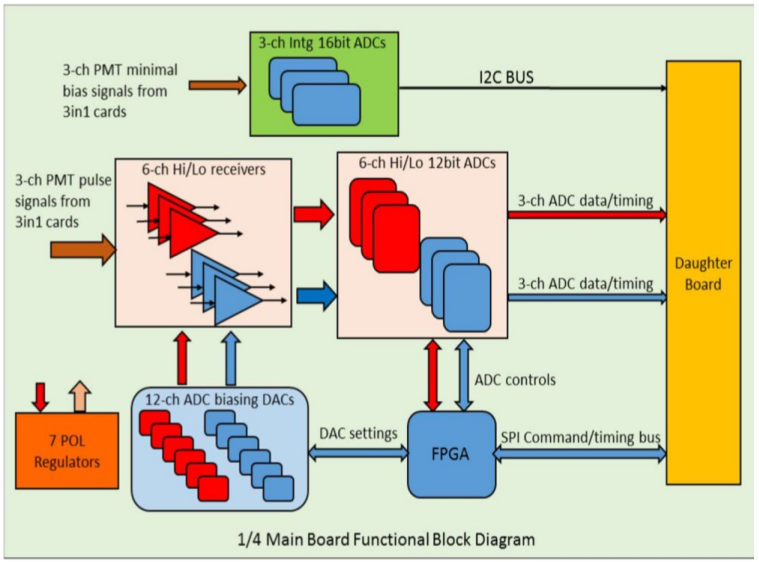
- PMT pulse shaping, 2 gains output and high precision slow integrator for Cesium calibration and luminosity measurement.
- Copy of Low gain for analog trigger
- Calibration through built-in Charge Injection System



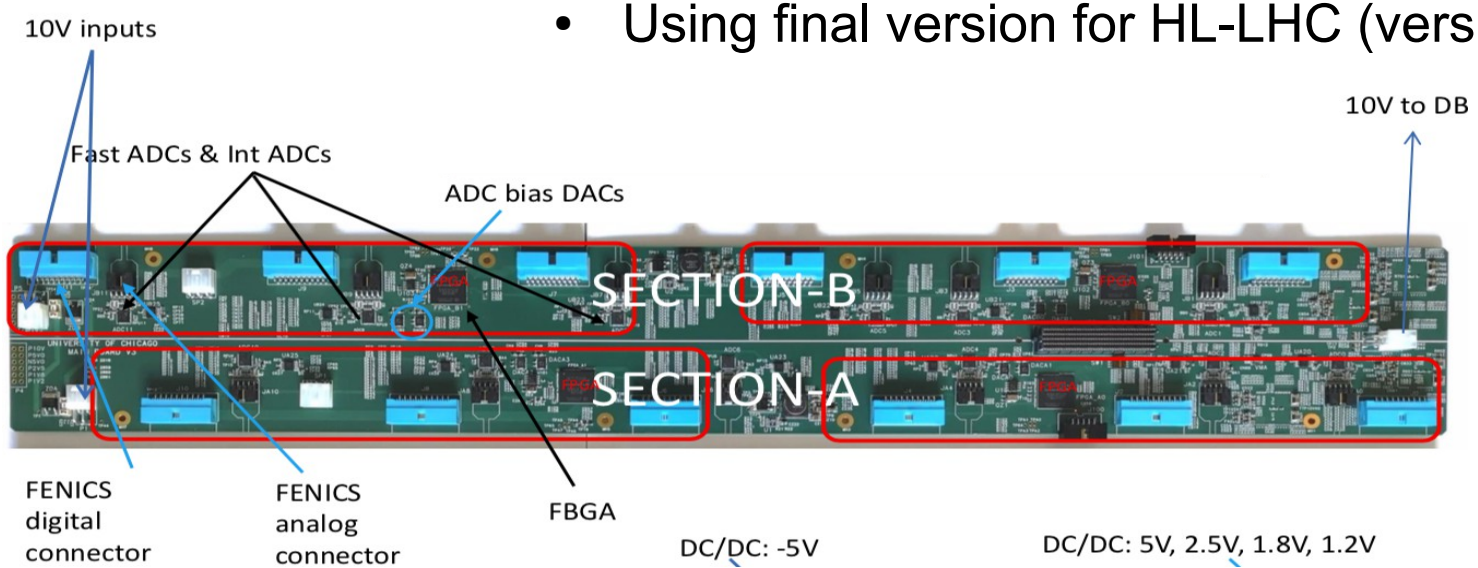




Main Board

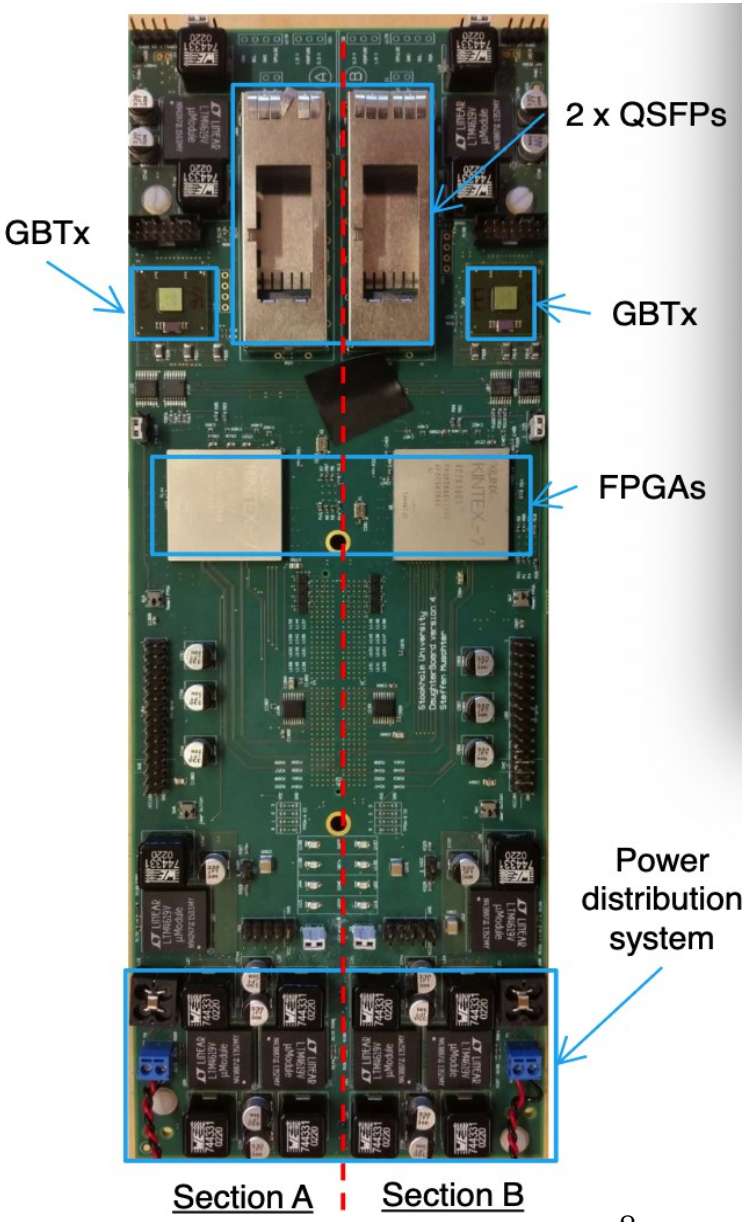


- Provide control, power and digitizer interface for 12 FEBs @ 40MHz and transmission to DaughterBoard
- Four quadrant with digital control and calibration capabilities through 4 Altera Cyclone IV FPGAs, 3 PMTs per quadrant. One PMT is readout by:
  - 12-bit dual ADCs @ 40 MSps for 2 gains
  - 16-bit SAR ADCs @ 50 kSps for slow integrator readout
- Divided into 2 independent section for power redundancy
- Using final version for HL-LHC (version 4)



Daughter Board

- High-speed links to off-detector electronics
  - Data collection, formatting & transmission to the back-end
  - Clock & command distribution to FEBs
  - Data link double-redundancy
- DaughterBoard v4 installed in Demonstrator
  - 2 GBTx chips for LHC clock recovery and distribution + 2 QSFP modules.
  - 2 Kintex 7 FPGAs for communication and data processing
- Possibility of replacing with latest DBv6
  - Kintex UltraScale FPGA with SEL tolerance
  - Added 2 Microsemi ProASIC3 FPGAs to interface the GBTx.
  - Improved clocking schema for driving the high-speed transceivers



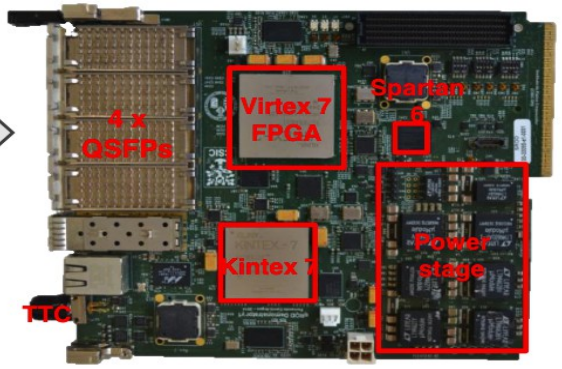
PreProcessor Demonstrator

- Off-detector readout with high-speed transmission
  - Data processing and LHC clock distribution
  - Interface with ATLAS readout
- Double AMC board: 4 QSFPs, Virtex 7, Kintex 7 and Spartan 6
  - Readout of up to 4 MDs (1 upgrade module)
  - Operated in a 2-slot ATCA shelf
  - Communication with TTC and legacy RODs systems and FELIX
- Possible replacement by Compact Processing Module, final HL-LHC readout system capable to read up to two modules

Compact Processing Module


Demonstrator module
(4 x Minidrawers)

4.8/9.6 Gbps



PPr Demonstrator

800 Mbps

4.8 Gbps

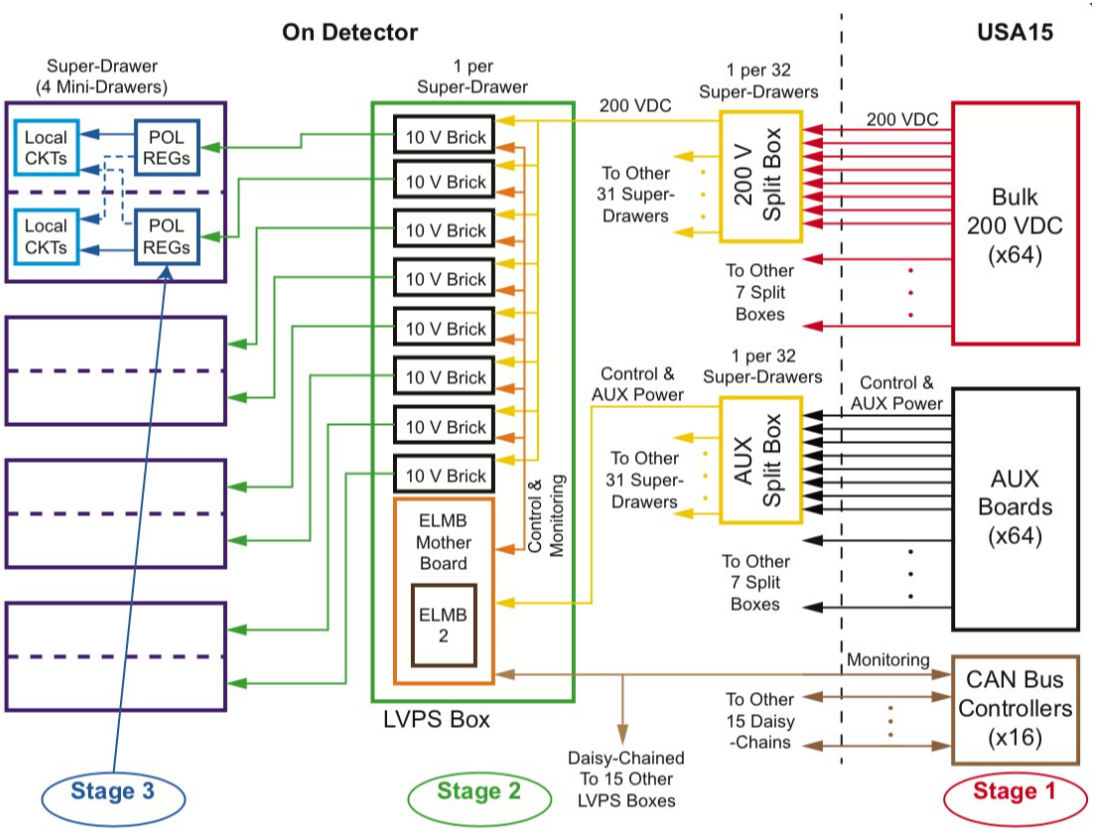

Legacy ROD

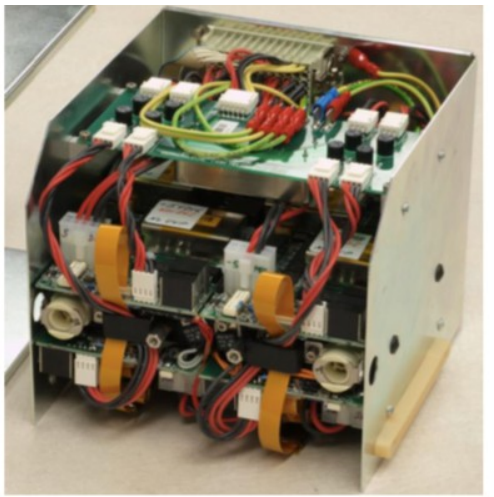

FELIX emulator

Low Voltage system

Three stage power system based on current system

- Design with better reliability, lower noise and improved radiation tolerance
- One DC level brick with +10V
- Redundant power distribution: 2 individual bricks per MD, 8 bricks in LVPS Box
- Control through ATLAS slow control system ELMB2
- Fully integrated into ATLAS DCS system

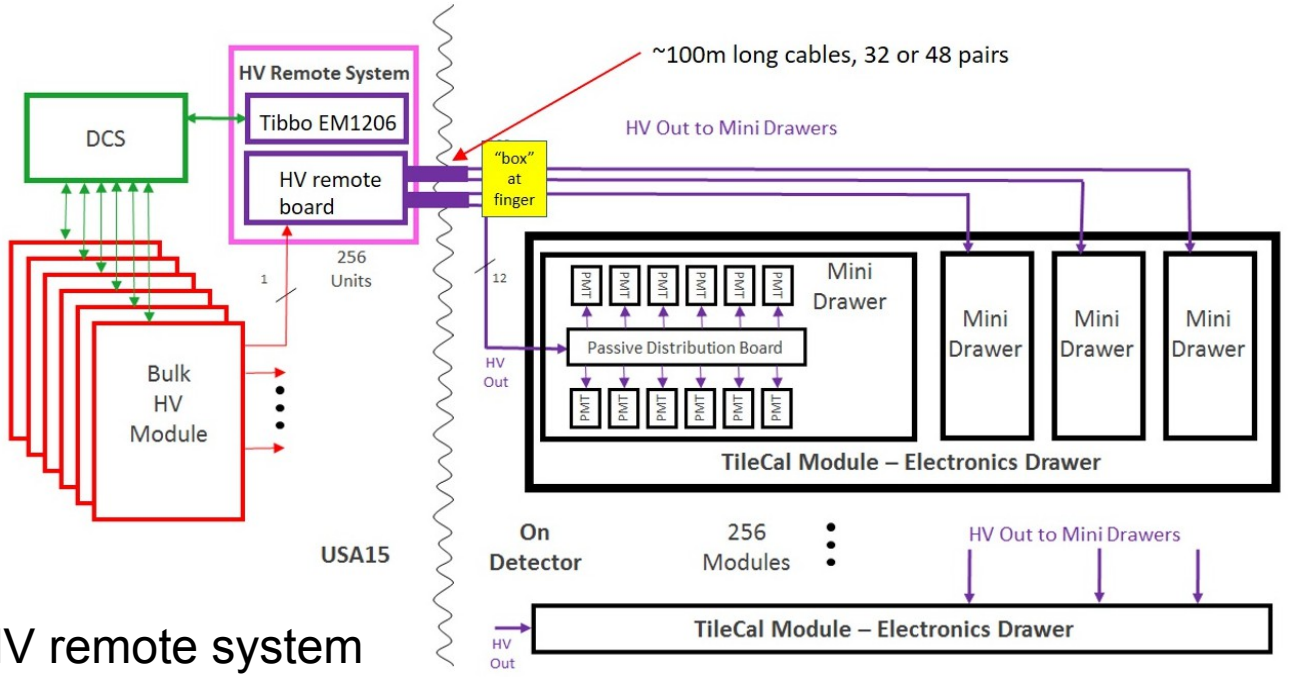




LVPS

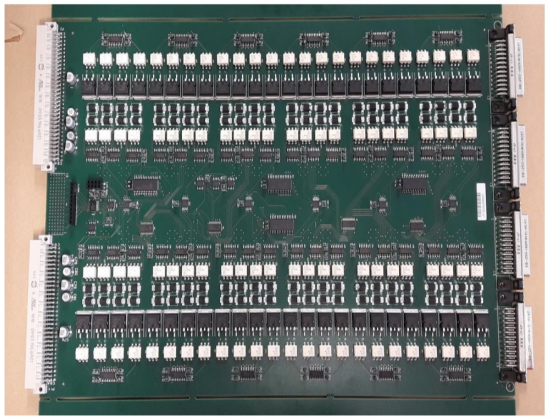
High Voltage system

- Off detector HV distribution and regulation (HV remote) installed in ATLAS service cavern (USA15)
  - No radiation issues. Always accessible for maintenance
- 100m long HV cable with 48 pairs of wires from USA15 to demonstrator
  - 4x 12 channels prototype with HV micro HV Opto for control and monitoring of 48 HV channels. Possible replacement with final HV remote system with 48 channels
  - 1 HV passive bus board per MD



HV remote system

48 ch HV remote board

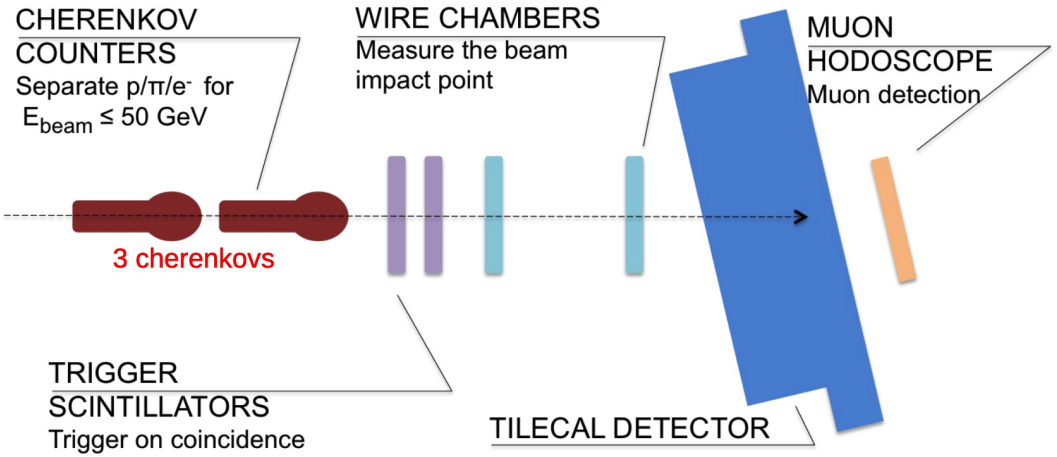


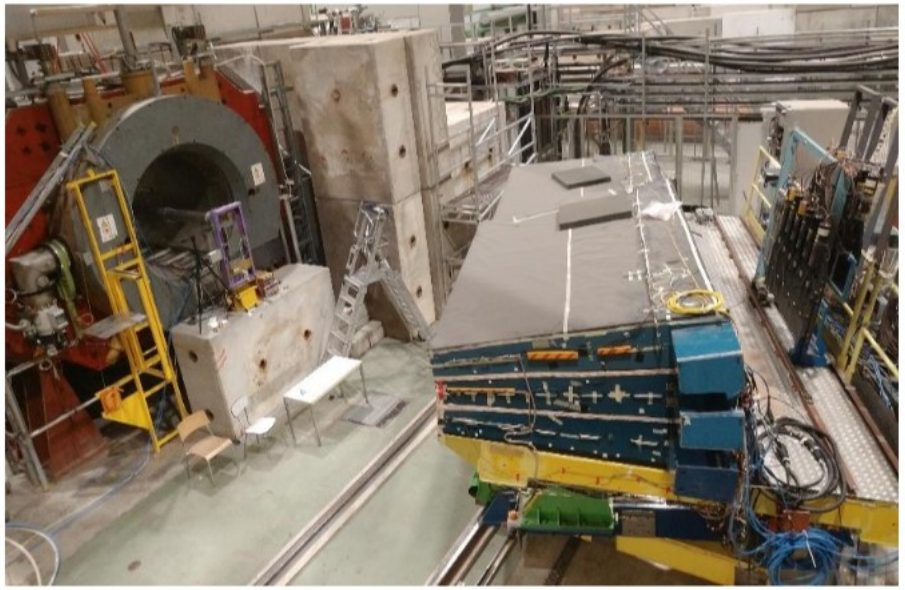
Demonstrator @ test beam

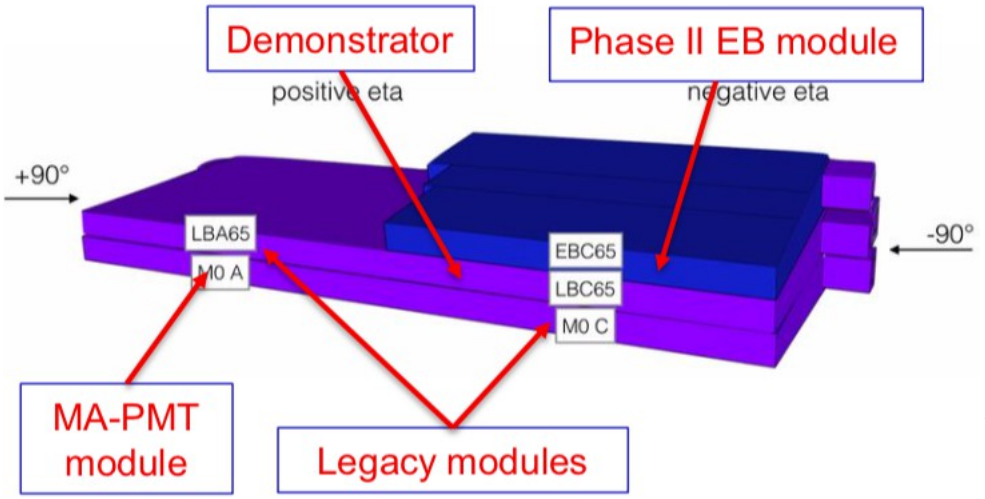
Typical setup, three Tile modules stacked on a movable table

- Tile Demonstrator in ½ of the Long Barrel module (middle raw)
- On top Extended Barrel with phase II upgraded electronics
- On bottom drawer with Multi-Anode PMTs and a legacy drawers
- Recorded electrons, muons and hadrons data at different energies, angles and positions

H8 beam facility at CERN SPS North Area

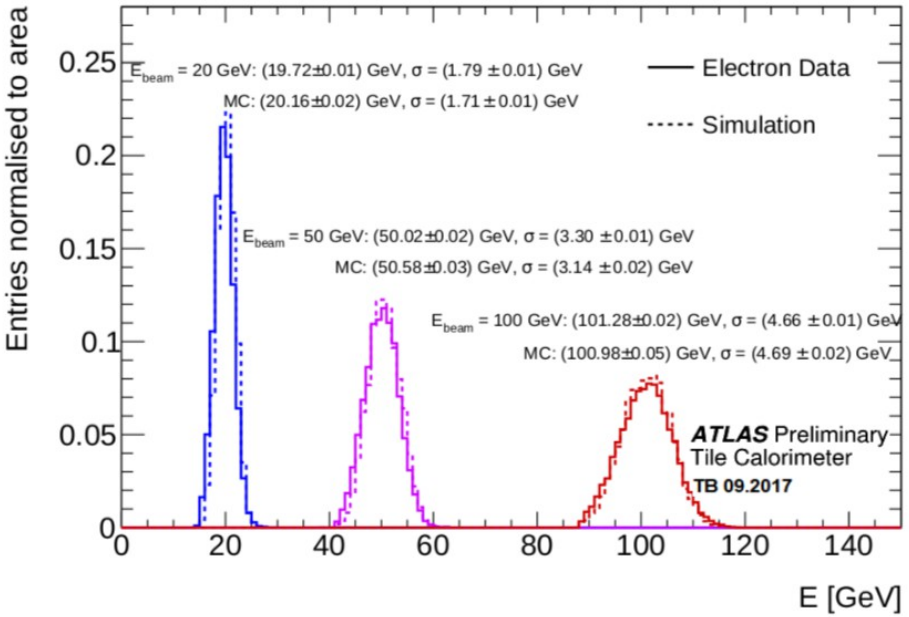




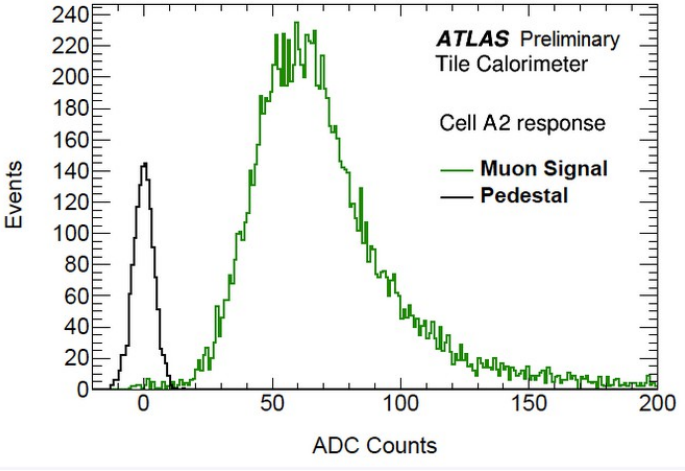


Results from test beam

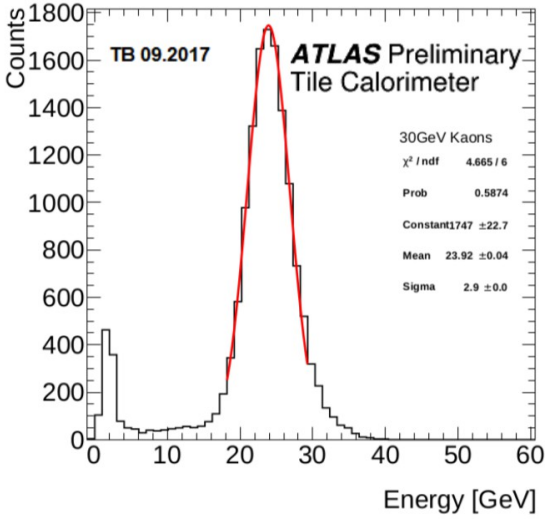
Checking the calibration at different electrons beams energies (2017)



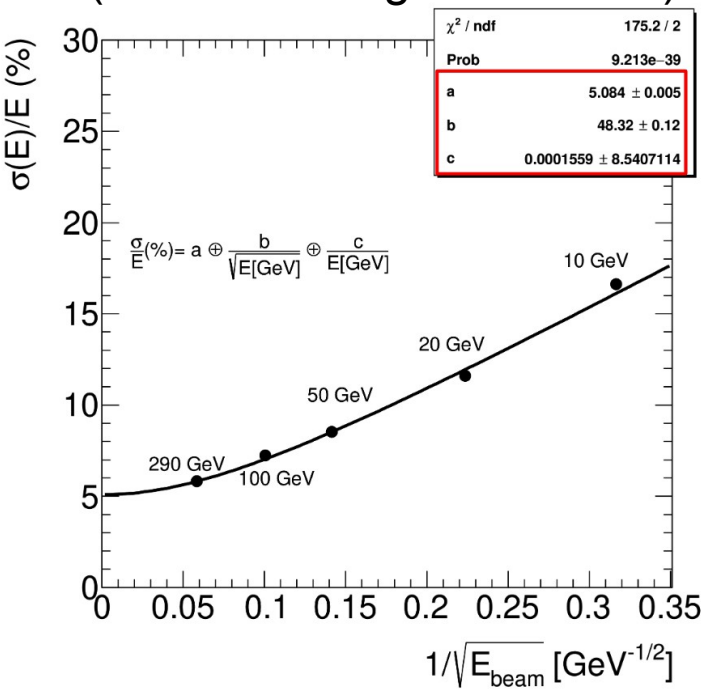
Projective Muons (2017)



Low energy hadrons (2017)



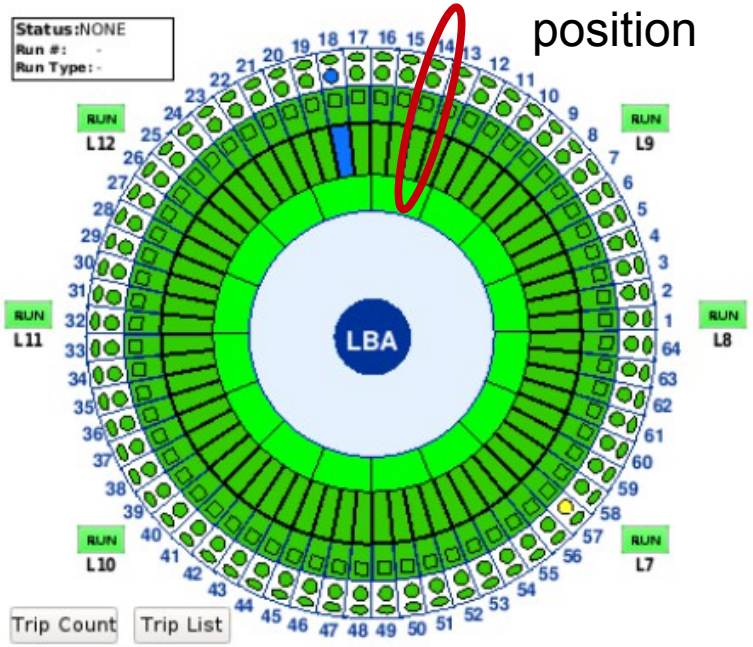
Energy resolution for pions (without leakage correction)

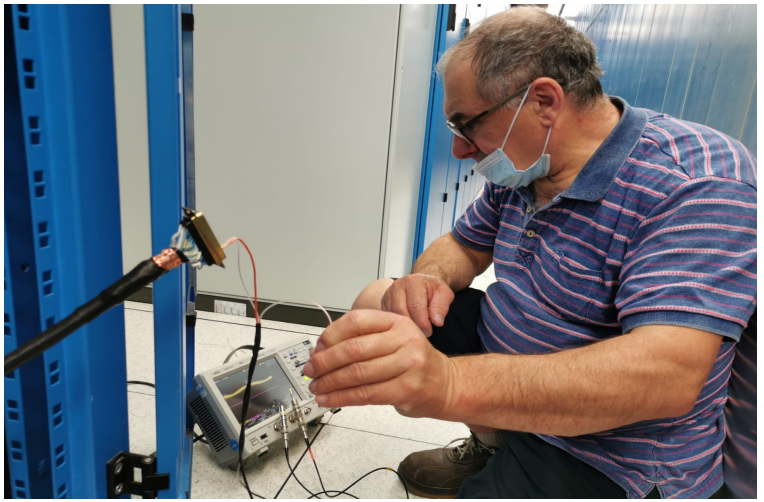


Demonstrator @ ATLAS

- Inserted in LBA14 during summer 2019
- Discovered some mechanical interference with MiniDrawers which lead to small modifications
- Powered (LV, HV) and monitored from DCS and calibrated using the TDAQ
- Stable performance, low noise and good CIS and laser signals
- Commissioned trigger towers output system to L1Calo

Inserted in top position



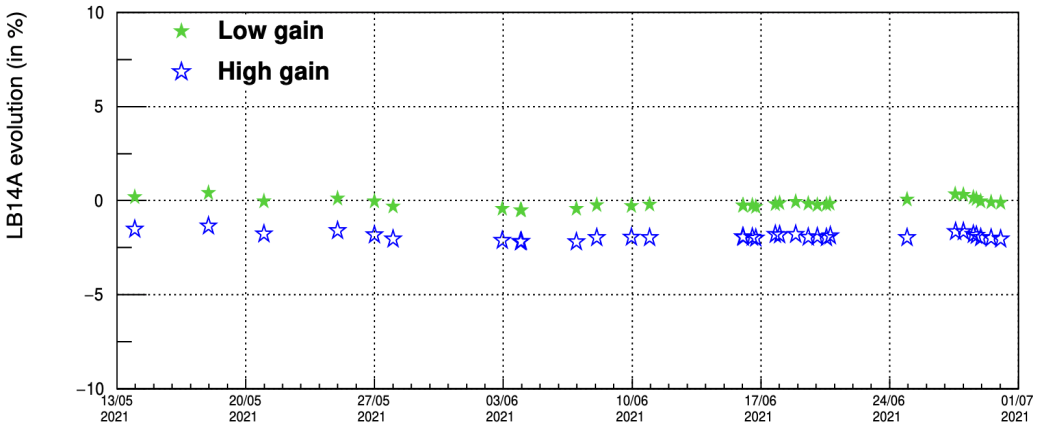


Commissioning the trigger in USA15

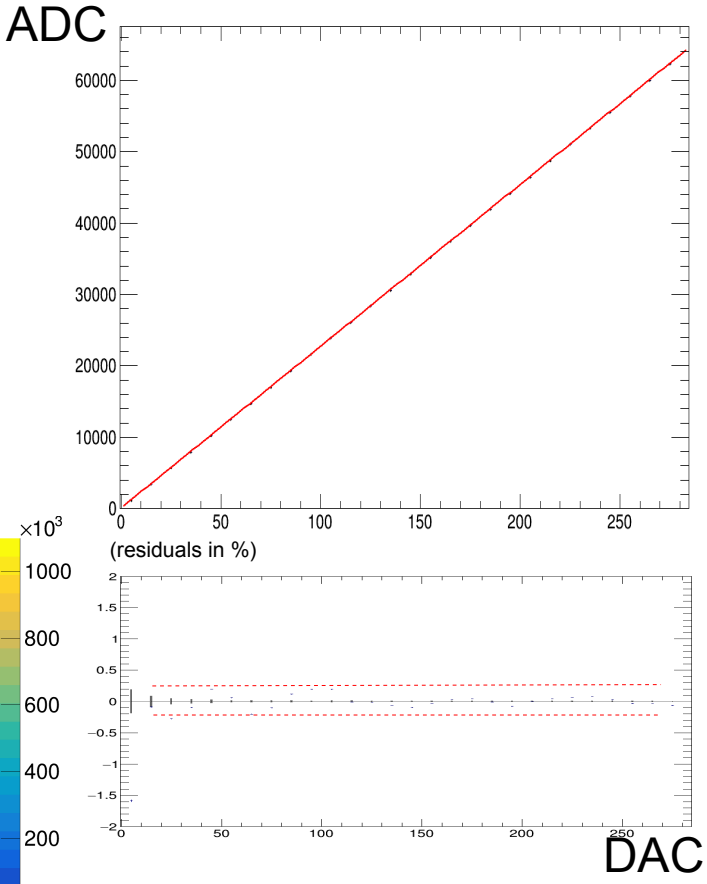
Inserting the demonstrator in ATLAS cavern

Performance results

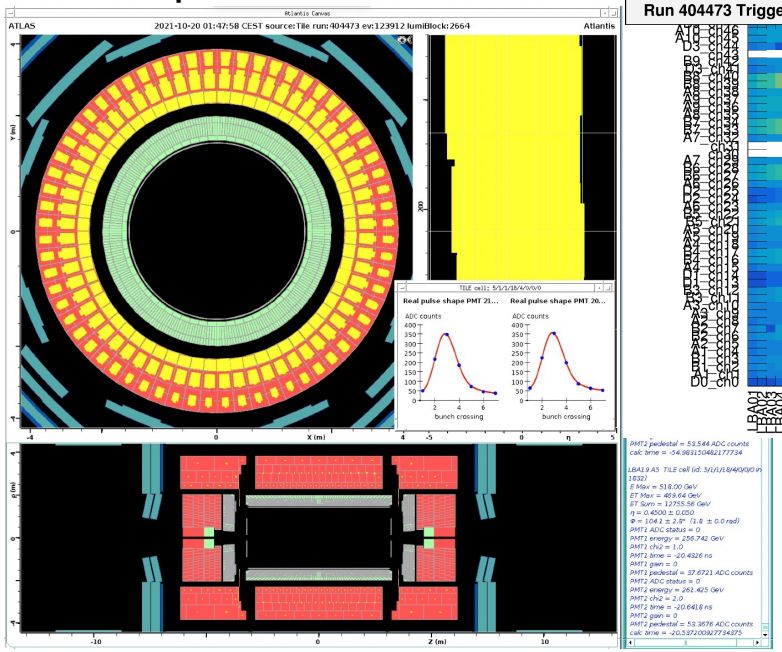
Laser time stability of demonstrator PMT response



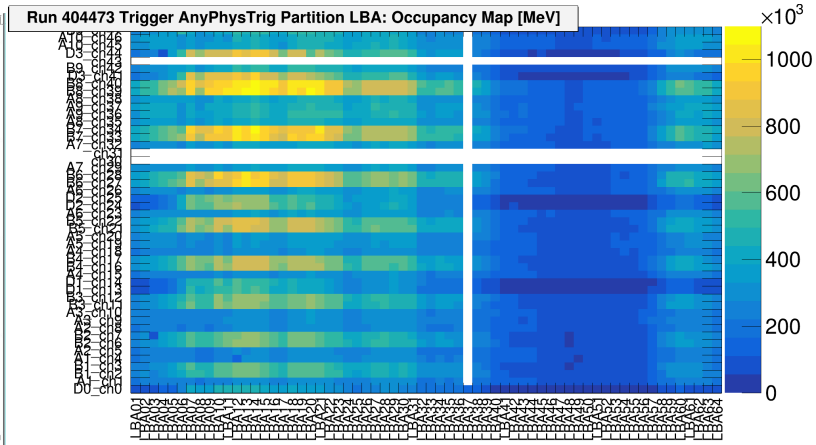
Integrator readout linearity



Beam splash event



Demo (LBA14) in occupancy plot



- Very good calibration performance
- Recorded cosmic data and LHC splash events

→ **Tile demonstrator performs at least as good as legacy drawers**

Summary

- Hybrid demonstrator module stying in ATLAS for Run 3
  - Latest HL-LHC electronics versions when possible
  - Operated with PreProcessor demonstrator prototype
- Keeping backward compatibility with current system
  - Sampling & transmission of data at 40 MHz
  - High-speed redundant links with fixed latency for clock distribution and readout
  - Analog trigger tower signal transmitted to L1Calo and data transmitted to RODs
- Test beam campaigns from 2015 to 2018 proved the good performance of the demonstrator
- Full integration of the Tile demonstrator in the current ATLAS DAQ and DCS systems