A First-Level Calorimeter Trigger for LHC Experiments - Design Studies, and Beam Tests of a First Prototype Trigger System

A.T. Watson
I.P. Brawn, R.E. Carney, Y. Ermolin, J. Garvey, R.J. Staley
School of Physics and Space Research, The University of Birmingham, Birmingham B15 2TT, UK.

E. Eisenhandler, M. Landon
Department of Physics, Queen Mary and Westfield College, London E1 4NS, UK.

C.N.P. Gee, A.R. Gillman, R. Hatley, V. Perera
Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire, OX11 0QX, UK.

N.N. Ellis
CERN, 1211 Geneva 23, Switzerland

Introduction:

First-level triggering for LHC proton-proton collider experiments poses significant experimental challenges. At a luminosity of 10^{34} cm^{-2} s^{-1} the inelastic proton-proton collision rate will be approximately 1 GHz. With a bunch-crossing interval of 25 ns this corresponds to approximately 25 collisions per bunch-crossing. The level-1 accept rate will be limited by the readout time of the front-end electronics to less than 100 kHz, requiring a rejection factor of 10^4 - 10^5. Physics signatures will be based upon combinations of high-p_T leptons, photons, partons and weakly-interacting particles, and therefore the trigger must be sensitive to these particles. This paper describes tests of a first prototype calorimeter trigger processor and developments in the design of a complete first-level calorimeter trigger system.

Trigger Algorithms:

The choice of algorithms is based upon extensive and ongoing physics simulation studies. These have been described elsewhere [1-3]. The inputs to the algorithms are transverse-energy (E_T) sums from "supercells" in the electromagnetic and hadronic calorimeters, of transverse granularity 0.1×0.1 in pseudorapidity-azimuth and summed in depth. The most complex algorithms are required for the electromagnetic cluster trigger (Figure 1). The trigger requires an electromagnetic cluster E_T greater than a cluster threshold as well as electromagnetic and hadronic isolation sums less than isolation thresholds. The trigger windows slide and overlap so as to cover the calorimeters fully. Studies indicate that such an algorithm gives acceptably sharp trigger thresholds and rates of a few $\times 10^4$ Hz for a range of trigger conditions satisfying the requirements of LHC pp experiments [1-5].

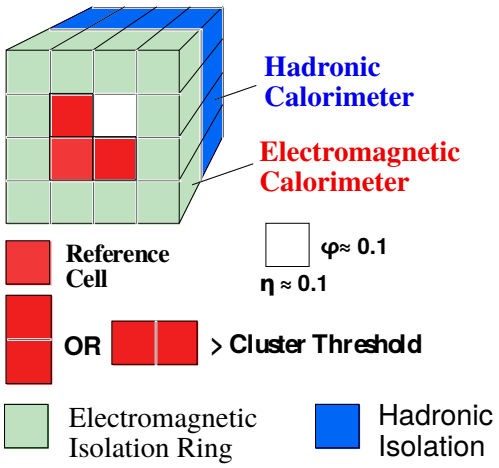

Figure 1: e/γ trigger algorithm

Trigger Prototype:

In order to investigate and demonstrate the implementation of such trigger algorithms, an ASIC has been constructed to implement the electromagnetic part of the algorithm shown in Figure 1 (hadronic processing was excluded to reduce cost). The ASIC is a 0.8μ CMOS gate array operating in pipeline mode. It takes as input 16 8-bit linear ADC values and calculates cluster and

isolation sums, which are compared with two sets of thresholds. In addition the sum of the 16 input values is computed, an operation required as input to the jet trigger. The ASIC delivers the 12-bit energy sum and the two trigger decision bits with latencies of six and seven clock cycles respectively. It has been described in more detail elsewhere [3].

The ASIC was tested in a cluster processor demonstrator system using a prototype LHC calorimeter. The system contains nine ASICs and fully processes 3×3 overlapping windows, requiring inputs from 6×6 trigger cells. Two backplanes were used, one with high-density Teradyne connectors (320 signal pins plus 80 grounds) for the data and clock connections and the other using a simple control/addressing protocol to interface to VMEbus. The module contains 256-deep circular buffers to capture time-slices of the input ADC data and the ASIC processing results. Comparison of the results with the inputs enables the performance of the trigger hardware to be studied in detail.

Beam Tests:

Data were recorded in CERN test beams with both the RD-3 barrel ("Accordion") and endcap ("Spanish Fan") liquid-argon calorimeter prototypes. Analysis of the "Spanish Fan" data is still at an early stage, so the following results come from the barrel calorimeter tests. In addition other tests have been performed with the RD-33 ("TGT") liquid argon calorimeter prototype.

Trigger cells of granularity approximately 0.1×0.1 were formed by analogue summation of signals from the calorimeter cells. The signals were digitised using a linear flash-ADC system sampling at the LHC bunch-crossing frequency of 40 MHz (some data were recorded at the original LHC frequency of 67 MHz) and passed to the cluster processor operating at the same speed. Data were taken with beam energies between 10 GeV and 300 GeV and a mixture of electron and pion beams, over a wide range of beam positions. Data were recorded both stand-alone, and also through the RD-3 data-acquisition system, to enable comparison with the full calorimeter data.

Figure 2 shows the trigger threshold curve obtained with 50 GeV electrons compared with the expectations from an ATLAS Monte Carlo. Since the beam spot-size was small compared with a trigger cell (about the size of a single calorimeter cell, whereas the trigger cell was 4×4 calorimeter cells) data from a number of runs with beams in different positions within the trigger cell were combined to produce this threshold curve. A good agreement was found between the observed and expected performance of the cluster algorithm.
Figure 2: Threshold curves from test data compared with Monte Carlo

The reliability with which the trigger processor executed the algorithms was studied by comparing the ASIC results with the expectation based upon the input ADC data and the trigger and isolation thresholds.
Figure 3: Performance of the ASIC cluster threshold

Figure 4: Performance of the ASIC isolation threshold

The performance of the ASICs in forming cluster and isolation sums and comparing with thresholds is illustrated in Figures 3 and 4. In Figure 3 the cluster sum, reconstructed from the input data, is plotted for events with and without the corresponding trigger bit set. Here the isolation threshold was set high to permit a clean test of the clustering. In Figure 4 the isolation sums are similarly plotted for events with clusters above the cluster threshold. In both plots it can be seen that the execution of the trigger algorithm at the full LHC clock speed was faultless.

Bunch-Crossing Identification Studies:
Figure 5: Pulse shape from Accordion calorimeter

Figure 5 shows a pulse from the Accordion calorimeter, after digitisation by the trigger FADC. A key feature is that the pulse occupies about four LHC beam-crossings in time. For the final trigger, filtering is therefore needed to identify the peak pulse-height and timing, and to suppress off-peak data which would otherwise contribute to (or veto) triggers in other bunch-crossings.

We have been studying the use of digital filtering for this purpose. Using software simulation, a range of algorithms has been studied, based upon convolution of the data from several samplings followed by peak-finding applied to the results of the convolution. Using data recorded with the Accordion calorimeter prototype as input, it was found that simple peak-finding always gave correct identification of pulses down to five counts (approximately 6 GeV), with little improvement being found from using more complicated filtering. Small pulses are the most difficult to filter, and studies in this area are continuing. Lower electronic system noise and higher-resolution ADCs would permit the performance of all algorithms to be improved.

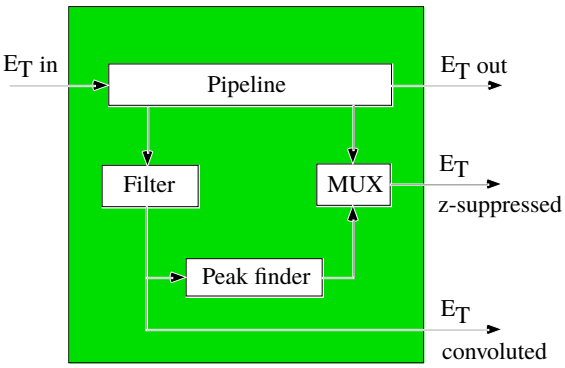

Figure 6: Block diagram of Bunch-Crossing Identification module

A first-prototype bunch-crossing identification module has been constructed and tested with the "Spanish Fan" endcap calorimeter prototype. The module, which filters data from a single channel, consists of a five-element deep pipelined Finite Impulse Response (FIR) filter followed by a five-element programmable comparator (peak-finder). It is illustrated in Figure 6. By setting the parameters of the filter and peak-finder appropriately, a range of algorithms could be tested in real-time at the full LHC bunch-crossing rate. The next trigger prototype will include similar bunch-crossing identification capabilities for all input channels, using Xilinx FPGAs for the digital signal processing.

Towards a Full LHC Calorimeter Trigger:

The current prototype has demonstrated that algorithms with the performance needed for LHC first level triggering can be implemented using currently-available ASIC technology and operated at the necessary speed . In order to construct a full system, however, a greater degree of integration is needed [6]; the current module processes only 9 channels, so using this modularity a full-scale 4000-channel trigger would require approximately 450 such modules. It is straightforward to process a larger area of the calorimeter in a single ASIC, but the pin counts required for parallel data input quickly become prohibitive. For example, an ASIC fully processing 4×4 trigger cells would require ~800 I/O pins alone, and a module with four such ASICs would require ~2000 backplane connections for inputs.

One solution to this problem would be to use serial input of data to the ASICs. This would provide an eightfold reduction in the number of I/O connections, but would require a corresponding increase in the bandwidth per connection. Current CMOS ASIC technology could not accept data at these rates. However, after pedestal subtraction, bunch-crossing identification and applying a noise threshold to the trigger cell E_T sums (typically 1 GeV) the occupancy of the calorimeters is expected to be only a few percent. Transmission of only zero-suppressed data would therefore reduce the bandwidth, but the resulting asynchronous data would then require bunch-crossing tagging and matching. Although having a greater latency, one advantage of this technique is that it would be inherently self-synchronising.

In order to demonstrate the viability of such a solution, as second trigger prototype is being constructed. In this system the digitised calorimeter pulses are pedestal-subtracted and applied to a bunch-crossing identification filter. The non-zero data are then tagged, serialised and transmitted optically at a rate of 160 MBd.

The cluster-finding ASIC converts the incoming serial bitstreams to parallel data, matches the tags and them passes the re-synchronised data to the trigger algorithm block. Note that while data transmission is asynchronous, the trigger decision itself is fully synchronous.

Design studies for this system are well advanced. Detailed system simulations indicate that the asynchronous transmission introduces negligible data loss and no data corruption. To reduce the non-recurrent engineering costs a dual-mode ASIC is being designed, which will include all necessary system functionality. Beam tests with prototype LHC calorimeters will be performed in mid-1995.

Acknowledgements:

We gratefully acknowledge the considerable help we received from RD3, both in allowing us to use signals from their calorimeter and in performing the beam tests.

This work is supported by the UK PPARC.

References:

[1] N. Ellis et. al., *Level-1 Trigger System*, ATLAS note DAQ-NO-005
[2] A. Watson, *Physics Simulation Studies of the First-Level electron/photon Trigger*,
RD27 note 13
[3] I.P. Brawn et. al., *Beam Tests of a Prototype Level-1 Calorimeter Trigger for LHC Experiments*, RAL-94-020, (Submitted to Nuclear Instruments and Methods).
[4] ATLAS Letter of Intent, CERN/LHCC/92-4
[5] CMS Letter of Intent, CERN/LHCC/92-3
[6] V. Perera, *A First-Level Calorimeter Trigger Processor for the LHC*, RD27 note 8