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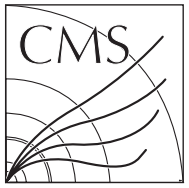

The Compact Muon Solenoid Experiment

Conference Report

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Study of a Triggered, Full Event Zero-Suppressed Front-End Readout Chain operating up to 1 MHz Trigger Rate and Pileup of 300 for CMS Outer Tracker upgrade at HL-LHC

Simone Scarfì, Gianmario Bergamin, Alessandro Caratelli, Luigi Caponetto, Davide Ceresa, Geoffrey Galbit, Sandhya Jain, Kostas Kloukinas, Yusuf Leblebici, Benedetta Nodari and Sebastien Viret on behalf of the CMS Tracker Group

Abstract

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Presented at *TWEPP2019 Topical Workshop on Electronics for Particle Physics*

PROCEEDINGS OF SCIENCE

Study of a Triggered, Full Event Zero-Suppressed Front-End Readout Chain operating up to 1 MHz Trigger Rate and Pileup of 300 for CMS Outer Tracker upgrade at HL-LHC

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The CMS Outer Tracker at HL-LHC will have to cope with pileup of 300 events per bunch crossing and a trigger rate of up to 1 MHz. The front-end electronics readout chain consists of readout ASICs connected to a data concentrator ASIC featuring zero-suppression. This contribution presents the methodology and the analysis work for the buffer sizing and exception handling featuring a robust data readout synchronization, with an event loss probability lower than 0.1 % at the highest pileup condition and a power density lower than 100 $\mathrm{mW/cm^2}$.

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1. Front-end readout chain for CMS Outer Tracker

The CMS Outer Tracker readout electronics at the HL-LHC will have to cope with 300 pileup (PU) events per bunch crossing (BX) for the innermost modules, close to the collision point. Pileup represents the number of proton-proton collisions per BX. A first level (L1) trigger rate of 750 kHz and a latency of 12.6 µs are required for efficient full event selection [1]. Upon the reception of a L1 trigger from the back-end, on one module 16 Macro Pixel ASICs (MPA) [2] combine and collect data from 16 Short Strip ASICs (SSA) [3] and provide the zero-suppressed full event data to two concentrator ASICs (2 CICs [4]). The input event rate is 32 Gbps, while the output bandwidth per module is 1.28 Gbps. The limited output bandwidth and the random nature of trigger arrival times require a temporary on-chip storage on MPAs and SSAs ASICs. The block diagram in Figure 1 depicts a high-level picture of the front-end readout chain.

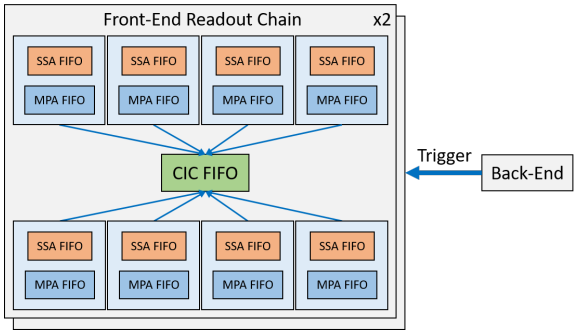

Figure 1: CMS Outer Tracker half-module readout chain.

This paper describes the methodology used for properly sizing the FIFOs in the three ASICs. The main points taken into consideration during the implementation have been:

- SEU robustness at chip level;
- SEU robustness and synchronization at multichip level;
- buffer inefficiencies below 10^{-6} for a PU of 300 and a trigger rate of 1 MHz.

The development and simulation of the different ASICs has been carried out using a System-Verilog and Universal Verification Methodology (UVM) multichip framework [6, 7], allowing to verify the ASICs' functionality at clock cycle accuracy with single event upset (SEU) injection, and a configurable PU and trigger rate.

2. FIFO sizing methodology

This section presents the FIFO implementation at the system level. The queueing theory, described in [5], relates the buffer inefficiency with the input/output (I/O) rate ratio (also called service rate (R)) for different buffer sizes (1, 2, 4, 8, 16 and 32 buffer stages) as shown in Figure 2. When the I/O rate ratio is fixed by the system architecture, as in the case of this paper, the buffer sizing depends only on the acceptable system inefficiency.

This methodology has been employed for the sizing of each FIFO in the multichip front-end readout chain to obtain an overall inefficiency below 10^{-6}.

3. ASICs readout architecture for triggered data

This section explains in detail the FIFO architecture for the front-end ASICs (MPA, SSA) and for the data concentrator ASIC (CIC). In Figure 3 the FIFO architecture of SSA and MPA is shown.

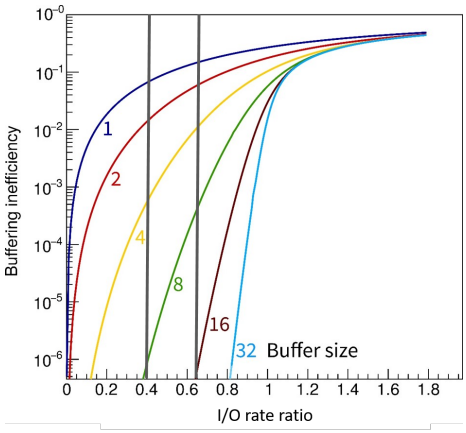

Figure 2: Buffer inefficiency with respect to I/O rate ratio.

The SSA needs to store in a FIFO several events before sending out to the corresponding MPA, a fixed size data packet containing the full raw data event. For the SSA FIFO the input rate is represented by the trigger rate, approximately 1 MHz, while the output rate is represented by the frequency of the data packet transmission (from SSA to MPA), which is given by construction by one serial data line operating at 320 MHz divided by the size of an event packet in bits (192 bits).

The service rate (R) is given by the following formula:

$$R = \frac{\text{Input Rate}}{\text{Output Rate}} = \frac{1\,\text{MHz} \times 192\,\text{bits}}{320\,\text{MHz} \times 1\,\text{line}} = 0.6 \tag{3.1}$$

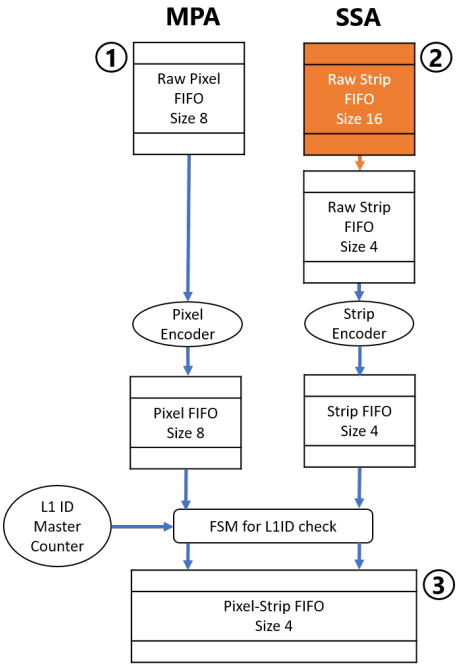

Figure 3: FIFO-based architecture of the front-end ASICs.

Using Figure 2, in order to have a buffer inefficiency below 10^{-6} a FIFO length of 16 is required. The same applies for the Raw Pixel FIFO in the MPA, but in this specific case the input rate depends on the cluster occupancy. Therefore, one must look at the cluster occupancy at PU 300 to size the FIFO for the worst case conditions. The Monte Carlo simulation of minimum bias events at PU 300 over the CMS Outer Tracker barrel geometry [8], allowed extrapolating the expected cluster occupancy for the innermost barrel layer, as shown in Figure 4.

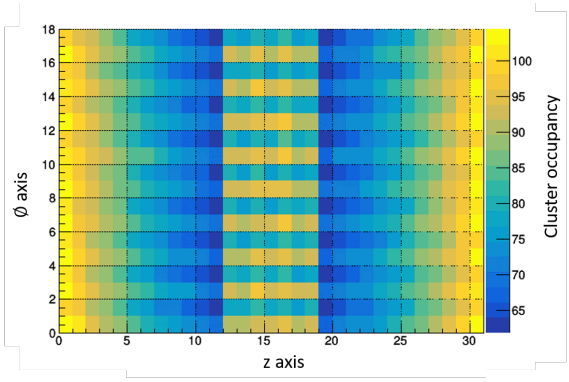

Figure 4: Cluster occupancy at PU 300 in the innermost barrel layer (cylinder external surface).

The highest cluster occupancy per module, where one module features two sensors on top of each other, is 110 clusters, but only one layer is read out by the MPAs. The maximum cluster occupancy is thus 55 clusters per 16 MPAs, i.e. four clusters per MPA. Therefore, the input rate is given by the trigger rate, approximately 1 MHz, multiplied by the cluster occupancy per MPA. On the other hand, the output rate is given by the frequency of the Pixel Encoder that encodes one cluster per cycle at 40 MHz.

Thus, assuming a worst case local cluster occupancy of 16 clusters per MPA, the service rate (R) is given by the following formula:

$$R = \frac{\text{Input Rate}}{\text{Output Rate}} = \frac{1\,\text{MHz} \times 16\,\text{clusters}}{40\,\text{MHz} \times 1\,\text{cluster}} = 0.4 \tag{3.2}$$

Using again the graph in Figure 2, in order to have a buffer inefficiency below 10^{-6} a FIFO length of 8 is required. The same approach can be used for all the other FIFOs in the system.

All the FIFOs are implemented as random access memory using library latches and can then be read using pointers allowing to save power. Master Counters are used to count the number of received triggers. These counters are triplicated to guarantee a robust synchronization between different ASICs, even in presence of SEUs, and the Finite State Machines (FSM), that are also triplicated, rely on them to match the correct data packet to be sent out. The same approach has been used for the Data Concentrator architecture in the CIC shown in Figure 5, where the FSM implements an exception handling mechanism able to deal with out of sync front-end ASICs. In this case, the CIC flags them to the back-end, and, later on, it can be configured to ignore data coming from the problematic front-end ASICs. After developing the analytical approach, the full readout chain has been simulated to take into consideration all the possible effects due to a complex and long chain of FIFOs. Spanning 25 ms with a PU of 300 and a Poisson distributed trigger rate

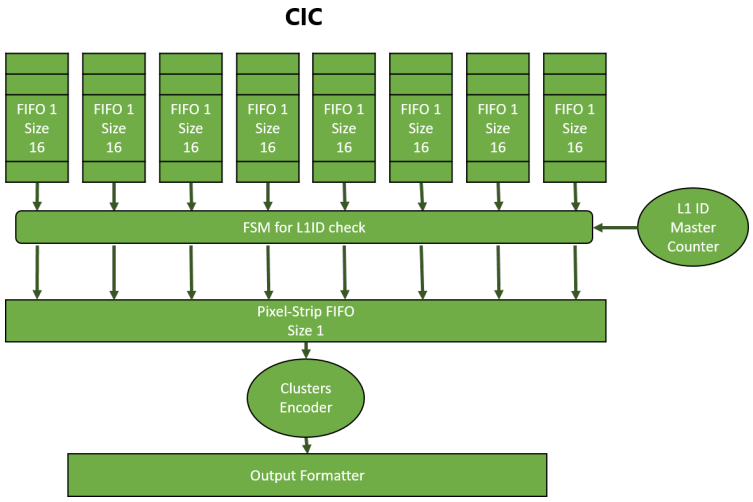

Figure 5: FIFO-based architecture of the Data Concentrator ASIC.

of 1 MHz a buffer inefficiency below 5×10^{-6} has been found. This value is slightly higher than the calculated one, due to the complexity of the system.

4. Conclusions

This paper presents the methodology used for sizing the data FIFOs across all the three ASICs in the CMS Outer Tracker front-end readout system. The analytical approach represents well the system, but a simulation with a well developed verification framework is needed to prove everything is taken into account.

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