PROCEEDINGS OF SCIENCE

TIGER: a custom readout electronics for the BESIII CGEM detector

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TIGER (aka Torino Integrated Gem Electronics for Readout) is the ASIC designed at INFN-Torino for the front-end electronics of a cylindrical triple GEM detector, proposed to replace the inner tracker of BESIII spectrometer (Beijing Electron Spectrometer). The high luminosity of the collider, operational at the Institute of High Energy Physics in Beijing (IHEP), allows to measure states of charmonium and open charm, to carry out light hadrons spectroscopy and to study τ lepton physics, but it caused aging and degradation problems to the tracking performance. The 64-channel chip in analog-digital mixed mode has been designed using CMOS 110 nm UMC technology in order to be exported to China. Each channel has two branches: branch E for charge measurements and branch T for time measurements.

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1. Introduction

BESIII (Beijing Electron Spectrometer) is an experiment operational at BEPCII (Beijing Electron Positron Collider), a double ring multi-bunch collider working in the energy range from 2 to 4.6 GeV. The high luminosity of the collider, about 10^{33} $cm^{-2}s^{-1}$, gives access to a rich physics program, including the spectroscopy of exotic charmonium states, light hadrons and τ physics.

A superconducting solenoid magnet provides a central field of 1.0 T. The spectrometer consists of a 9-layer Resistive Plate Counter (RPC)-based muon chamber system with a spatial resolution that is better than 2 cm, a CsI(Tl) crystal calorimeter with an energy resolution that is better than 2.5% and a position resolution better than 6 mm for 1 GeV electrons and gammas, a Time-of-Flight system with an intrinsic timing resolution better than 90 ps and a Helium-gas based multilayer drift chamber (MDC).

The main tracking detector is composed of an outer chamber and an inner one joined together at the endplates, sharing the same gas volume. The MDC has a spatial resolution of 130 μm in rϕ plane (azimuthal) and 2mm in the z-coordinate (polar) and a momentum resolution of 0.5% at 1 GeV [1].

Luminosity increase is speeding up the aging of the inner tracker (IT). Due to the huge beam-related background, the inner chamber has been suffering from aging problems, with gain decreasing of 4% per year [2]. Since BESIII will run at least up to 2022, the inner chamber shall be replaced.

A Cylindrical Gas Electron Multiplier (CGEM) detector has been proposed for the replacement [2]. The detector is made of three coaxial triple GEM layers with cylindrical shape. All layers have the same structure consisting in five electrodes: Cathode, GEM1, GEM2, GEM3 and the Anode for the readout. Such a detector will match the requirements for momentum resolution (0.5%) and radial resolution (130 μm) of the existing drift chamber and will improve significantly the spatial resolution along the beam direction (< 200 μm) with a very small material budget (less than 1.5% of X_0). The readout combines the charge centroid method, to identify the position of the fired strips, and the so called micro-TPC technique to reckon how the magnetic field affects the electronic avalanche [2]. Taking into account strong constraints in terms of space, power consumption and spatial resolution, an analog readout method was chosen, developing a custom ASIC to provide charge measurements down to 1 fC with a sensor capacitance of 100 pF and time measurements with a time resolution of 5 ns at 1 fC.

2. CGEM-IT readout electronics

A block diagram of the CGEM -IT readout electronics is shown in Figure 1. The readout chain can be divided in: on detector electronics, comprising eighty Front-End Boards (FEBs) hosting 160 ASICs, and off detector electronics, consisting of data processing units and ancillary devices in order to provide TIGER with timing and configuration data and to collect from TIGER the records of the particle detection events.

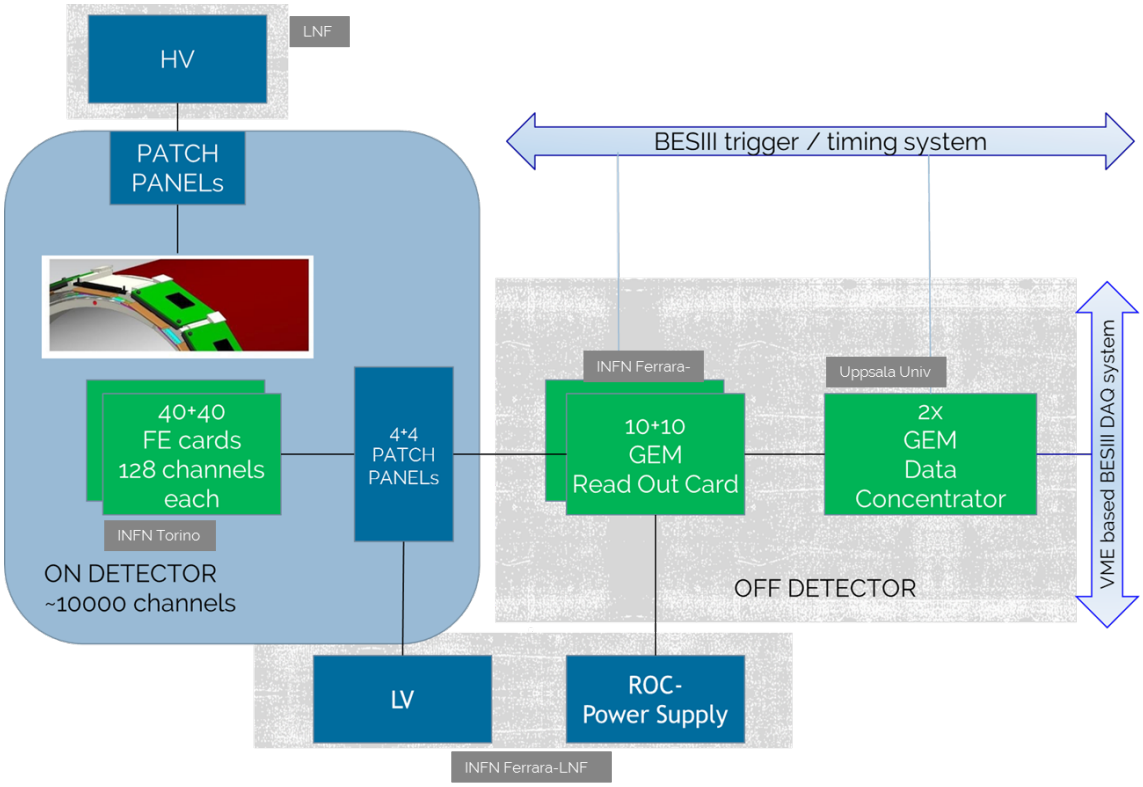

Figure 1: Scheme of CGEM Inner Tracker readout electronics

In detail, GEM Read-Out Cards (GEMROC) transfer over optical fibers at 2 Gbit/s data towards VME based GEM Data Collectors. Data are gathered in 16 kB Link FIFOs and an event builder module is used to sort, frame and send over the Local Bus to the Data FIFO. The chain is completed by Low-Voltage and High-Voltage distribution system to power TIGER FEBs and the CGEM detector, respectively. The design of voltage distribution systems copes with the fact that CGEM Inner tracker will not be accessible after insertion, so the systems have to assure reliability.

3. TIGER

In order to achieve the spatial resolution of about 130 μm, an analogue readout was chosen, loosening the strip pitch to 650 μm and reducing the total number of channels to ten thousand with respect to digital readout.

TIGER, a 64 channels front-end mixed mode ASIC (Figure 2), was designed in CMOS technology 110nm UMC, in order to be exported to China. Besides time and charge constraints,

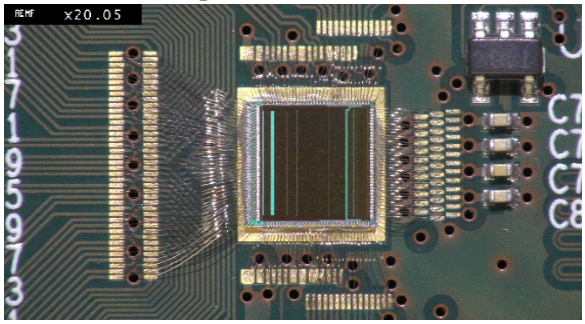

Figure 2: A TIGER chip bonded on a test board

it fulfils the requirements of a dead time less than 1 μs, with 60 kHz rate per channel, considering a safety factor 4×, and of a power consumption per channel about 10 mW. Each TIGER should provide time and charge measurement featuring a fully digital output and being SEU-tolerant. The input stage amplifies the charge sensitive detector current and feeds two independent continuous time shapers. In the fast shaper, the peaking time is matched to the expected charge collection time with the purpose of providing an optimal timing performance. The peaking time of the slow shaper is chosen 160 ns in order to improve the charge resolution, Each shaper is followed by a voltage mode discriminator whose threshold can be tuned with a 6 bit DAC. Two low power TDCs are provided. The coarse time information is obtained by counting the transitions of the chip master clock. Four Time-to-Amplitude converters are employed to refine time resolution [3].

The test setup for TIGER prototype characterization is shown in Figure 3. TDCs operation was assessed in terms of quantization error and jitter. A scan over dynamic range was carried out sweeping the internal test-pulse. A look-up-table is used to store the gain and the offset correction for all the channels. The TDC quantization error after calibration results of 30-35 ps. Jitter measurements were carried out using internal calibration circuit test-pulse (e.g. 10 fC) sweeping input capacitance on channel 62. A typical measurement is shown in Figure 4 for time branch, resulting in a value less than 2 ns.

Noise was evaluated for each input capacitance through a sigmoid fit from a typical 500 points threshold-scan with fixed test-pulse (10 fC), both for energy and time branches, repeating measurement fifty times. Gain was evaluated on channel 63 using an external pulse generator. A gain of 10.4 mV/fC was obtained in agreement with simulations [4]. An unexpected shift on the amplifier baseline was observed on time branch, not affecting operation. It is well reproduced in post silicon simulations and its caused by a fragility in the baseline holder circuit biasing.

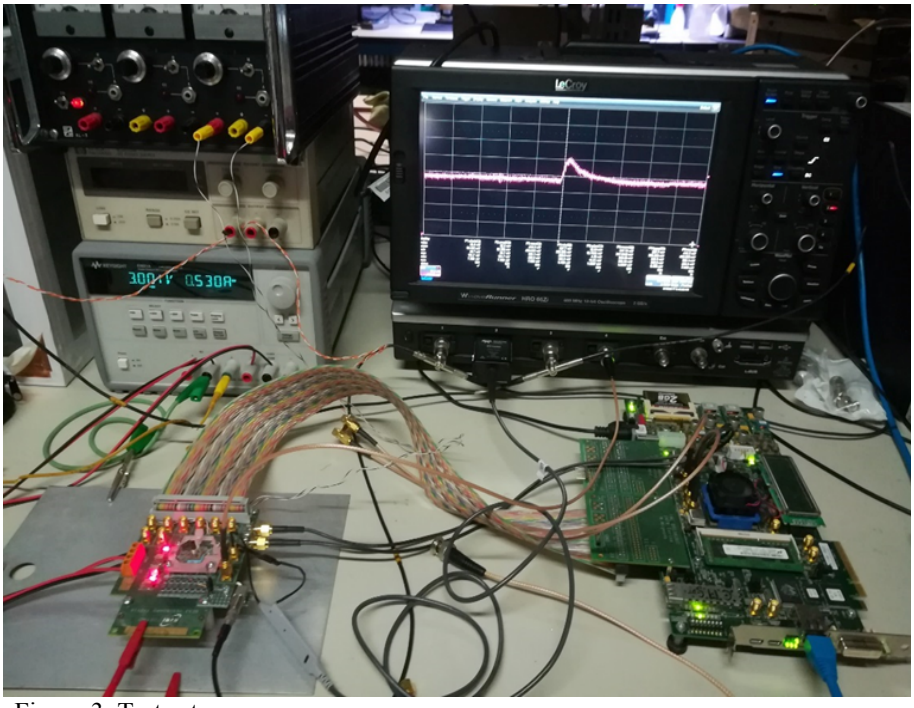

Figure 3: Test setup

Calibration of Sample and Hold circuit was carried out with an external generator, showing a linear dynamic range of about 500 mV.

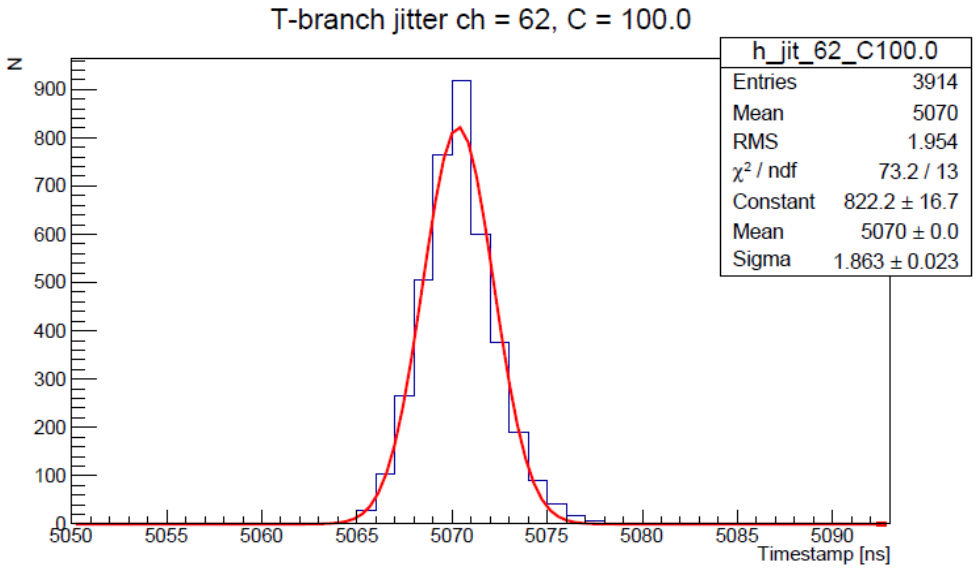

Figure 4: Jitter of Time Branch measured on channel 62 with a capacitance of 100 pF

In order to assess sensitivity to grounding or system level power, first tests were conducted on GEMs, acquiring first signals with a ^{90}Sr source (Figure 5) and cosmic rays.

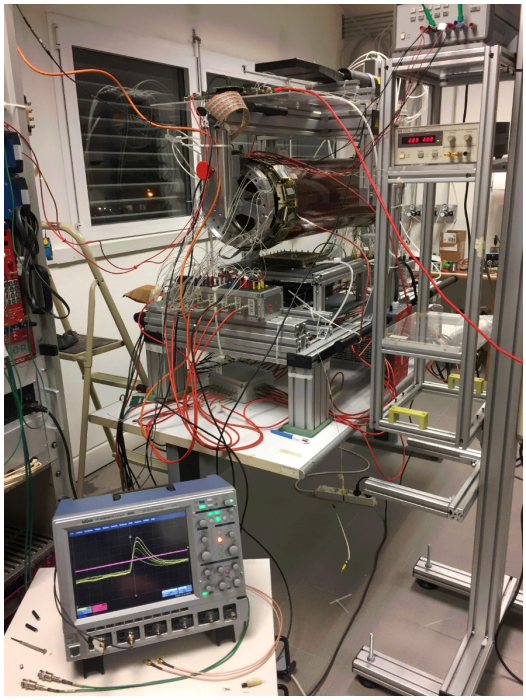

Figure 5: First signals acquired with TIGER

CONCLUSIONS

The first characterization results assessed the full functionality of the silicon up to 200 MHz clock frequency, the SPI-based configuration and multi-link LVDS SDR/DDR data

transmission. The time-based readout (time tagging and time-over-threshold measurement) with a dual-TDC was checked, with a residual quantization error below 40 ps r.m.s. First estimates of noise, gain dispersion (over multiple channels) and linearity of the front-end are promising. A minor revision is planned without the need of a second prototype to correct an unexpected shift on the amplifier baseline, well reproduced in post silicon simulations. The test campaign with the full-scale detector is a fundamental step to assess the performance of the on-detector electronics, as it explores a realistic grounding and noise pick-up environment. First results are assuring us the readiness of the design for the production tapeout, foreseen for Summer 2017.

Acknowledgements

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