

# The performance and operational experience of ATLAS Semiconductor Tracker in Run-2 at LHC



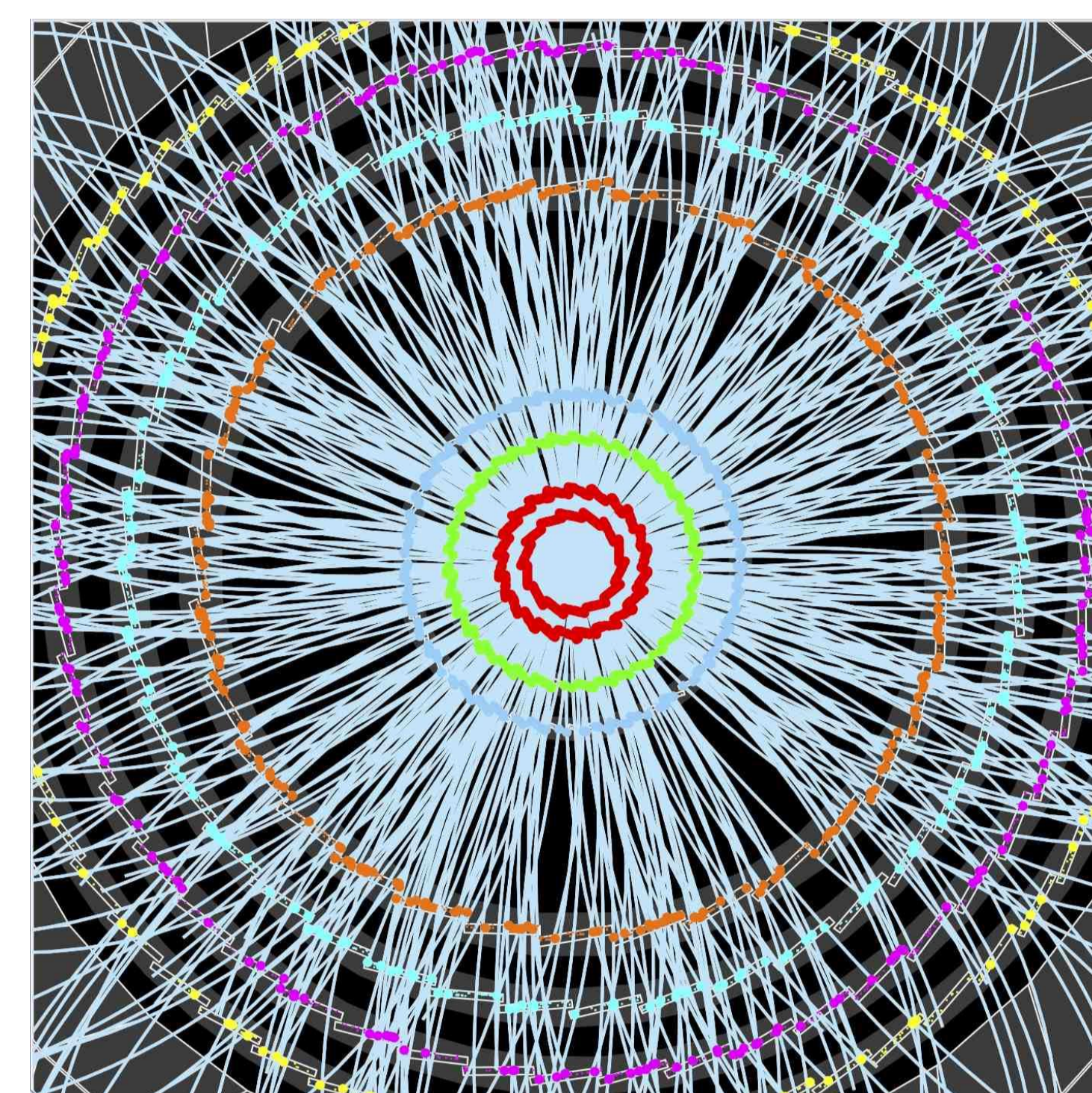
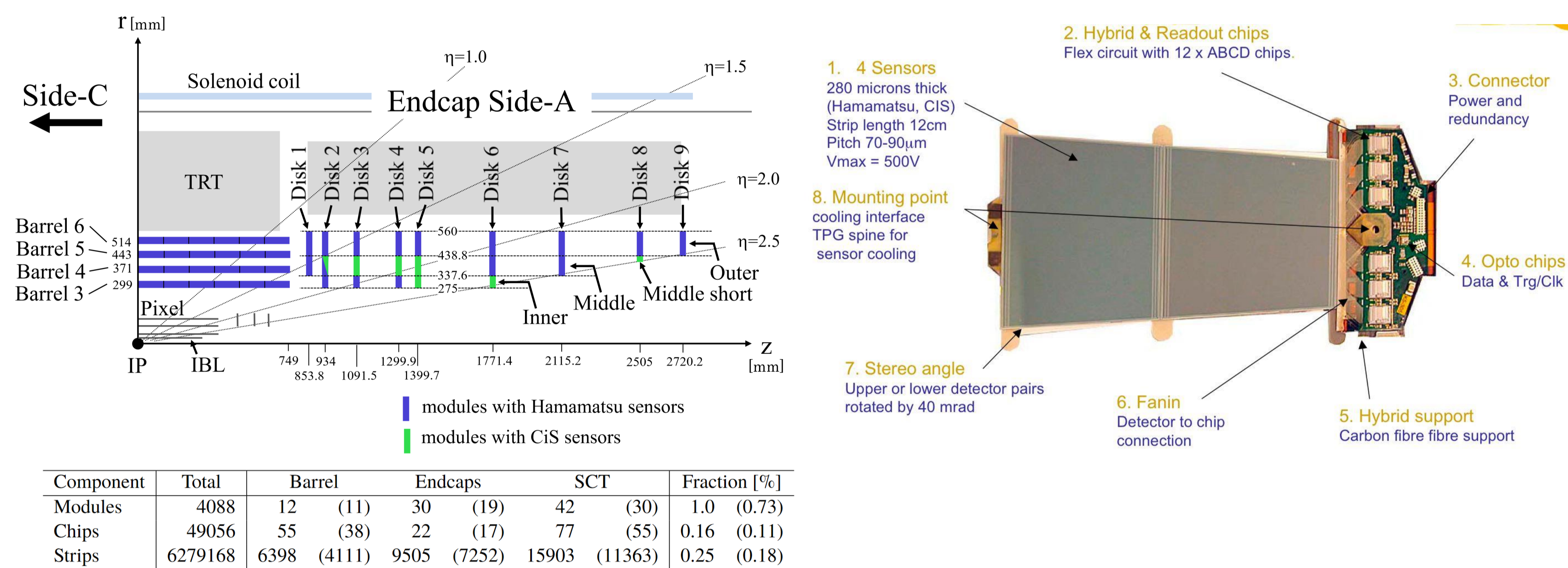
European Physical Society conference on high energy physics 2021  
Online conference, July 26-30, 2021

## The Run 2 at LHC

Results from  $pp$  Run 2 (2015-2018): 156 fb<sup>-1</sup> @ 13 TeV. Peak luminosity: 2·10<sup>33</sup> cm<sup>-2</sup>s<sup>-1</sup>.

Twice the design LHC luminosity: **higher pileup**, up to ~60  $pp$  interactions per events possible instead of 23, leading to up to **~2% hit occupancy** (SCT design 0.2-0.5%).

## The semiconductor tracker (SCT)

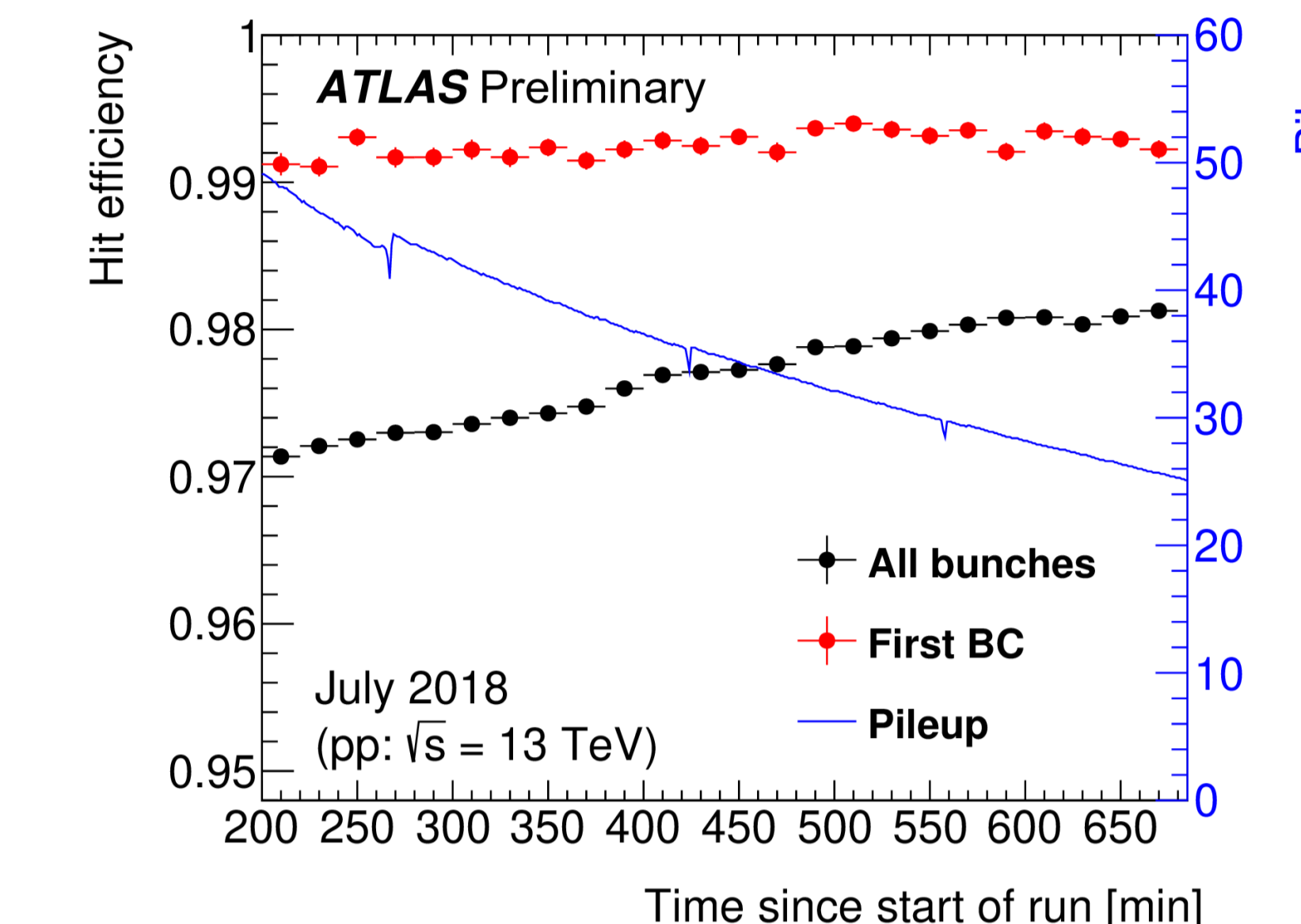


## Performance

**Hit Efficiency** for a track with  $N_{cluster}$  and  $N_{hole}$  associated defined as

$$\epsilon = \frac{N_{cluster}}{N_{cluster} + N_{hole}}$$

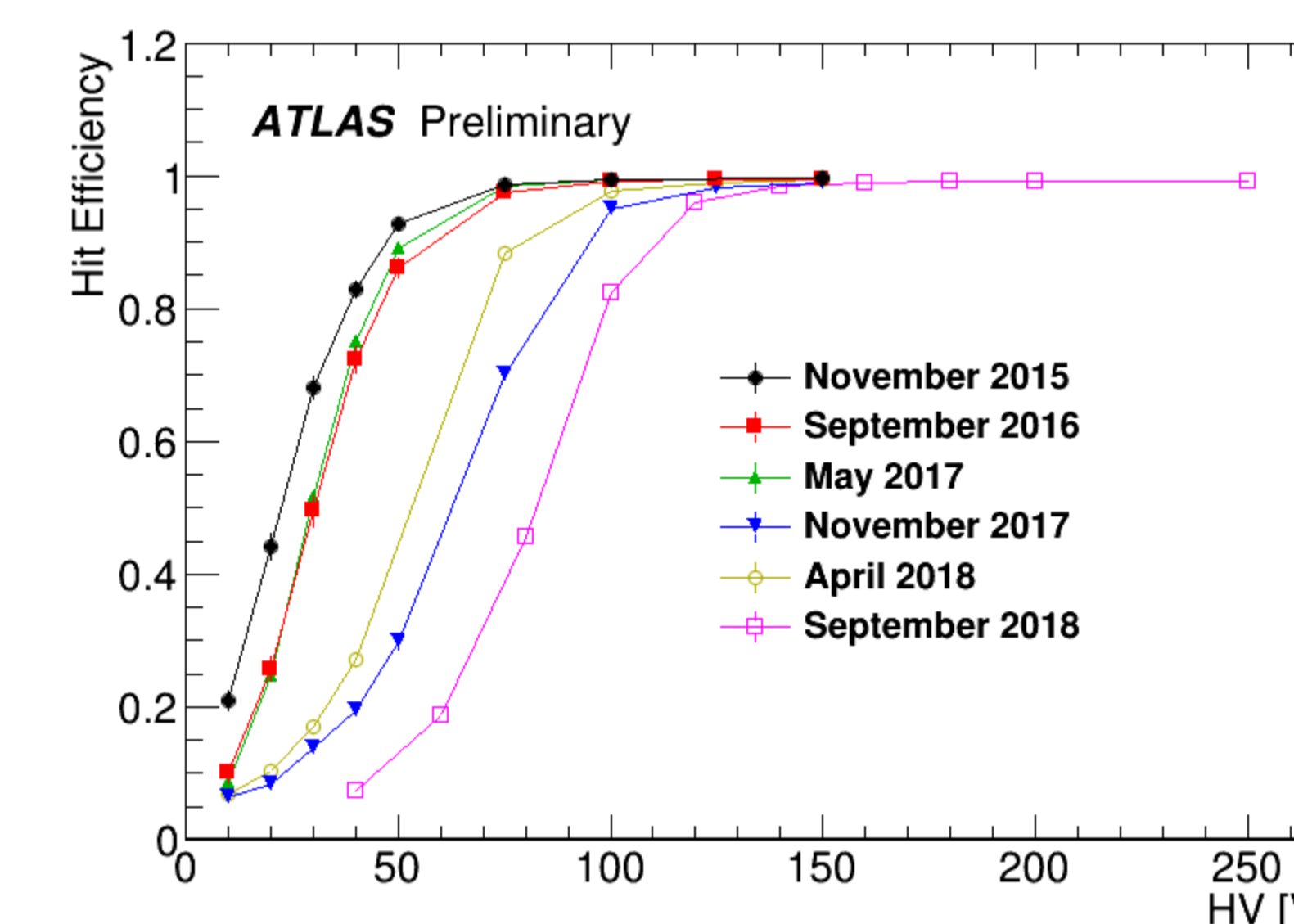
Affected by the "01X" read mode: real hit lost, if present in preceding bunch.  
Negligible impact on tracking (1% hit loss).



Pileup affects hit efficiency (left). The **intrinsic hit efficiency (~99%)** obtained by the first bunch in a train.

## Radiation Damage

Effect of radiation damage on the modules: number of donors decreases, acceptors increases → **Type Inversion** from  $n$ -bulk into  $p$ -bulk material, expected around second half of Run 2. Taken into account in the design, built to endure up to 700 fb<sup>-1</sup> @ 14 TeV.



After type inversion, increase in efficiency with HV was slower (left). **Operational HV** was therefore **increased**.

## Calibration

Goal: Maintain hit efficiency >99% and **noise occupancy < 5x10<sup>-4</sup>**. Methods:

- Analogue optimisation
- Trim range scan
- Response curve
- Optical
- Digital tests

## Data Acquisition (DAQ)

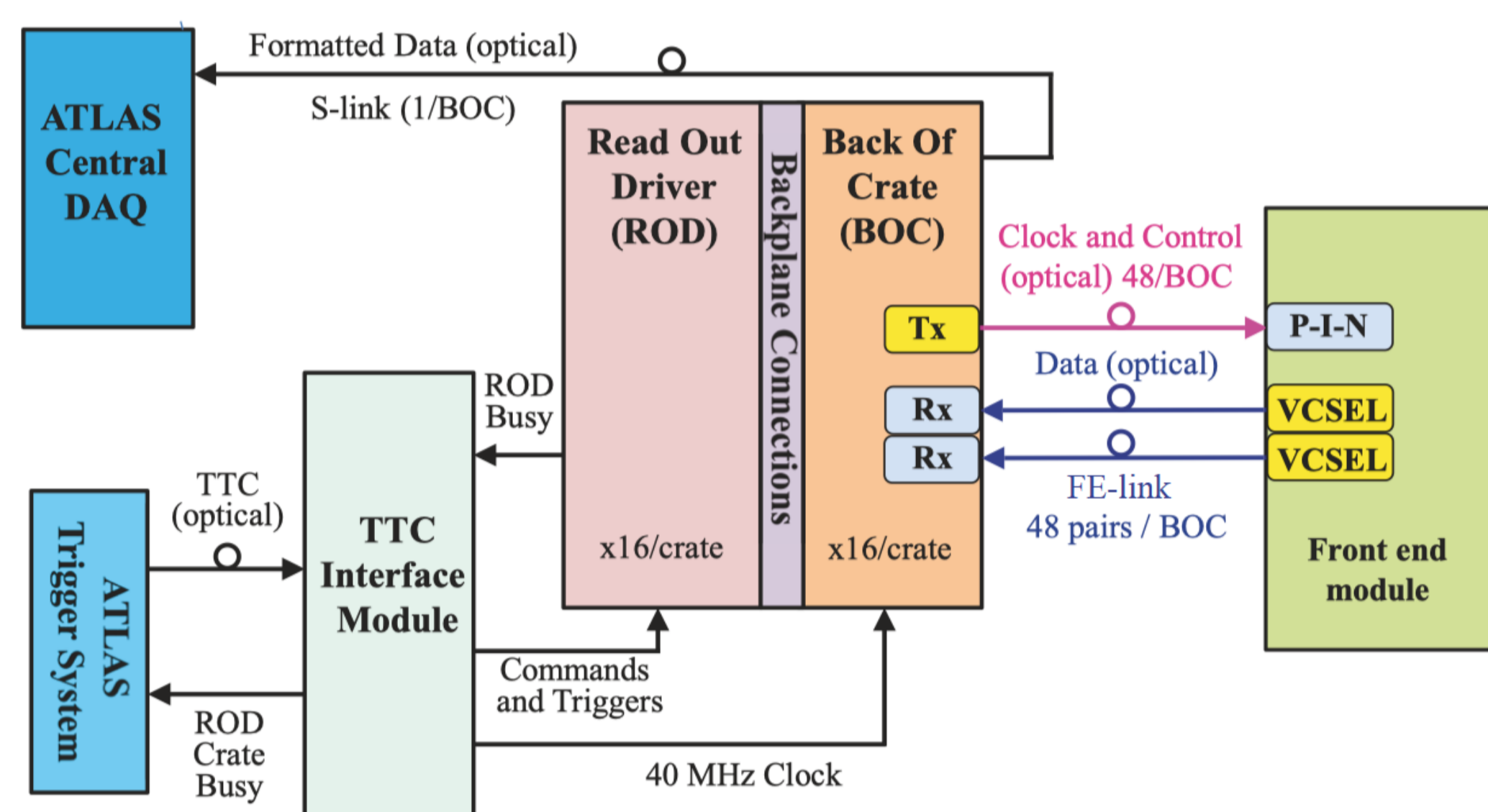
Need to overcome bandwidth limitations.

**S-links Expanded** from 90 RODs w/ 48 modules → to **128 w/ 36** modules

**Cable Remapping**: limit data load on each ROD to get a flatter occupancy distribution across S-links.

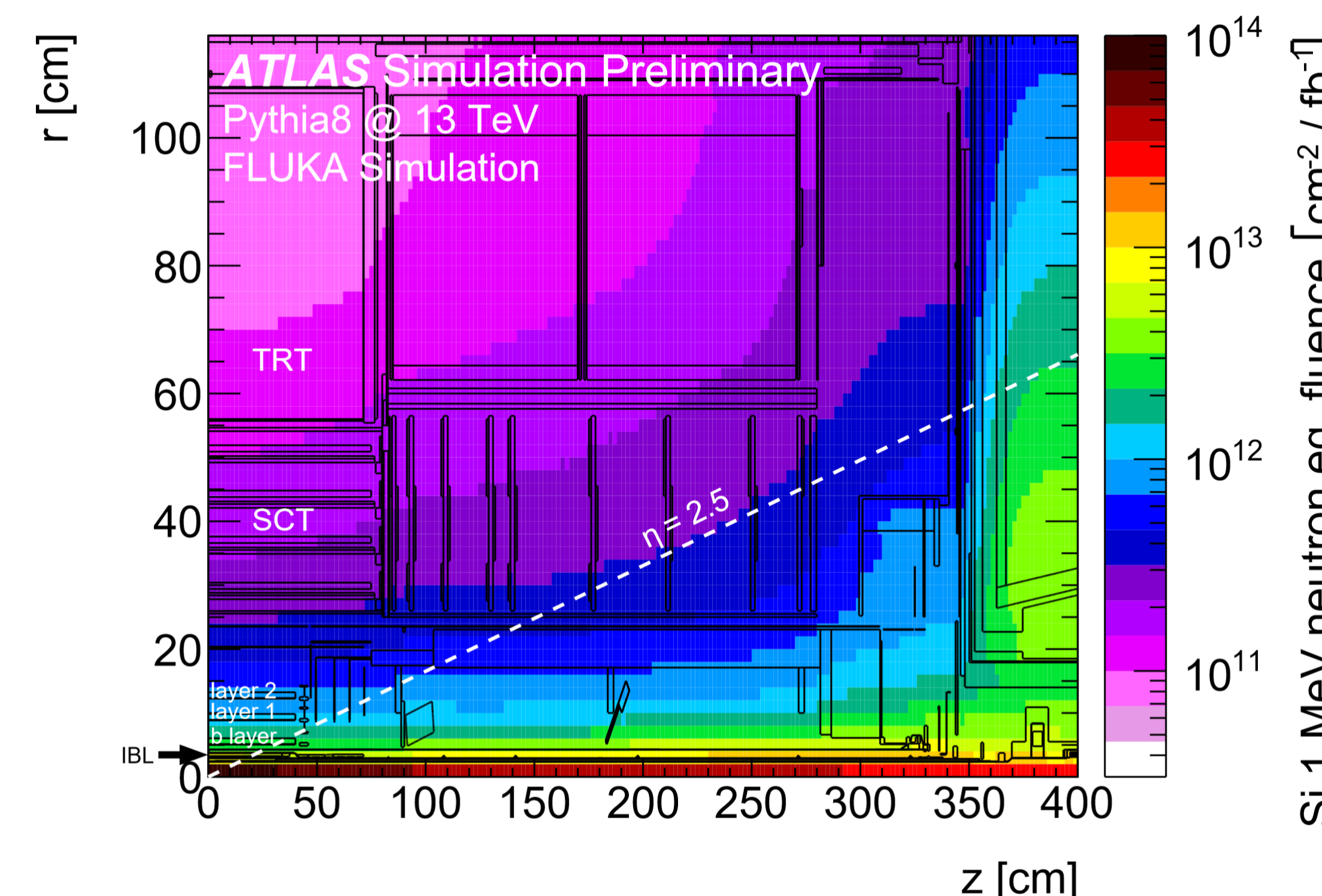
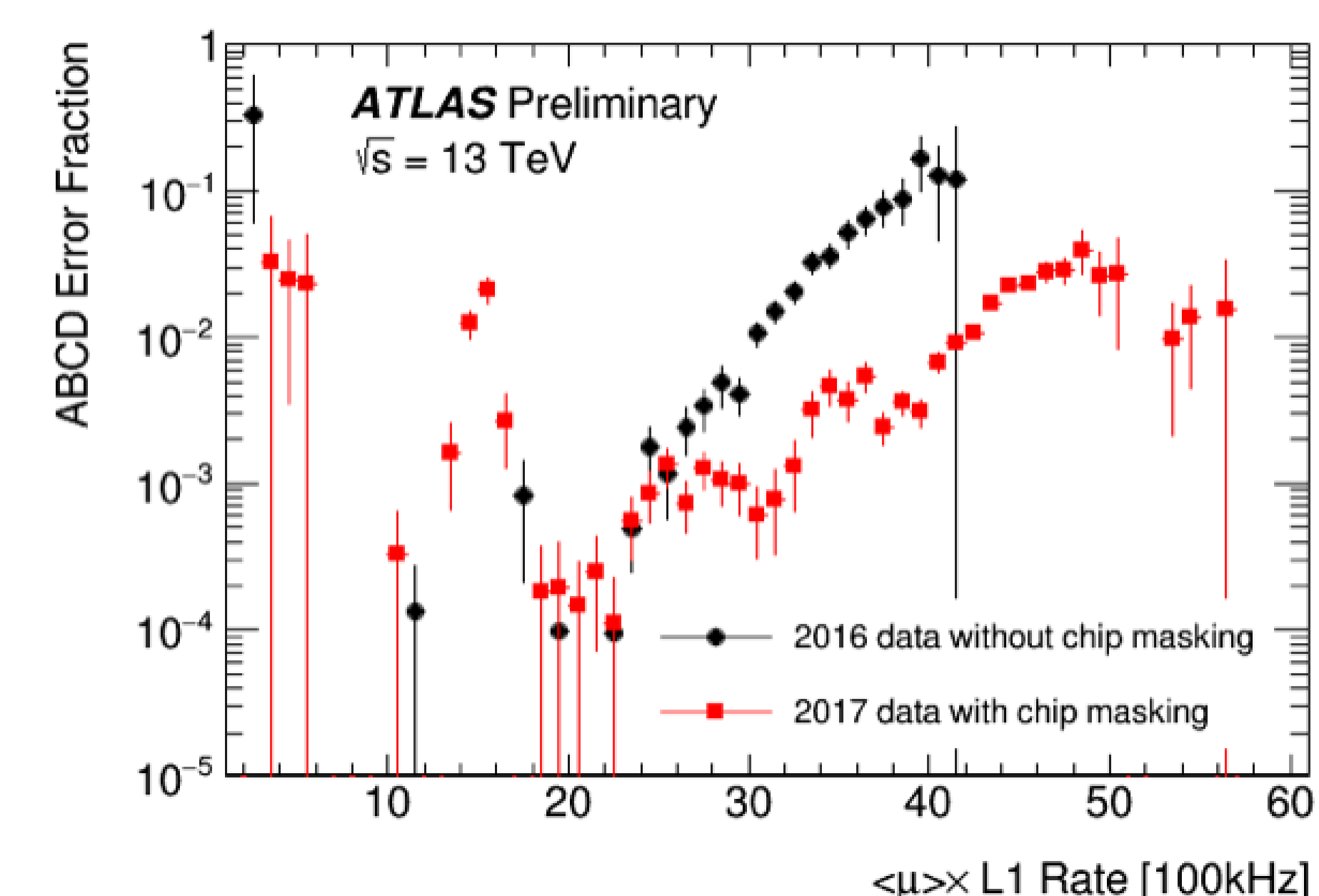
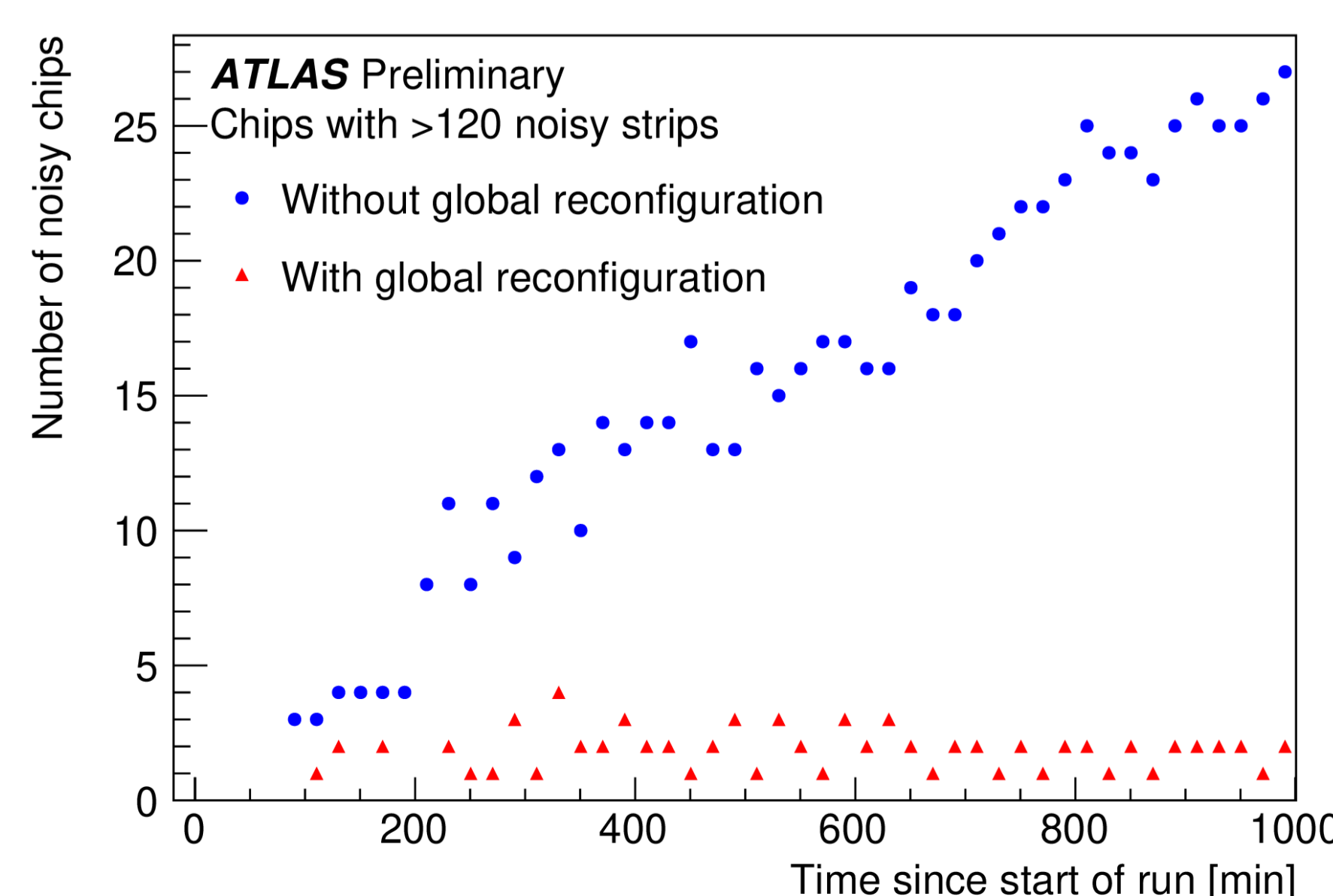
**Data Compression**: veto hits from preceding bunch crossing ("01X" read mode). Up to 16 strips clusters packed into a single 16-bit word: **~25% data size reduction**.

High pileup causes chip errors and makes modules noisy, increasing bandwidth use. Implemented **Chips Masking** during operation, recovering modules on the fly when pileup conditions improved.



A **Global Reconfiguration** to the entire SCT DAQ takes 1.2 seconds, recovering desynchronized modules getting noisy. It is regularly applied during data taking, for negligible data loss.

Average **SCT downtime in Run 2: <0.1%**.



Agreement between simulation (figure above and table below) and dedicated radiation monitoring systems:

- Total ionising dose (TID) →  $p$ -MOSFET transistors
- Non-ionising energy loss (NIEL) →  $p$ - $i$ - $n$  diodes

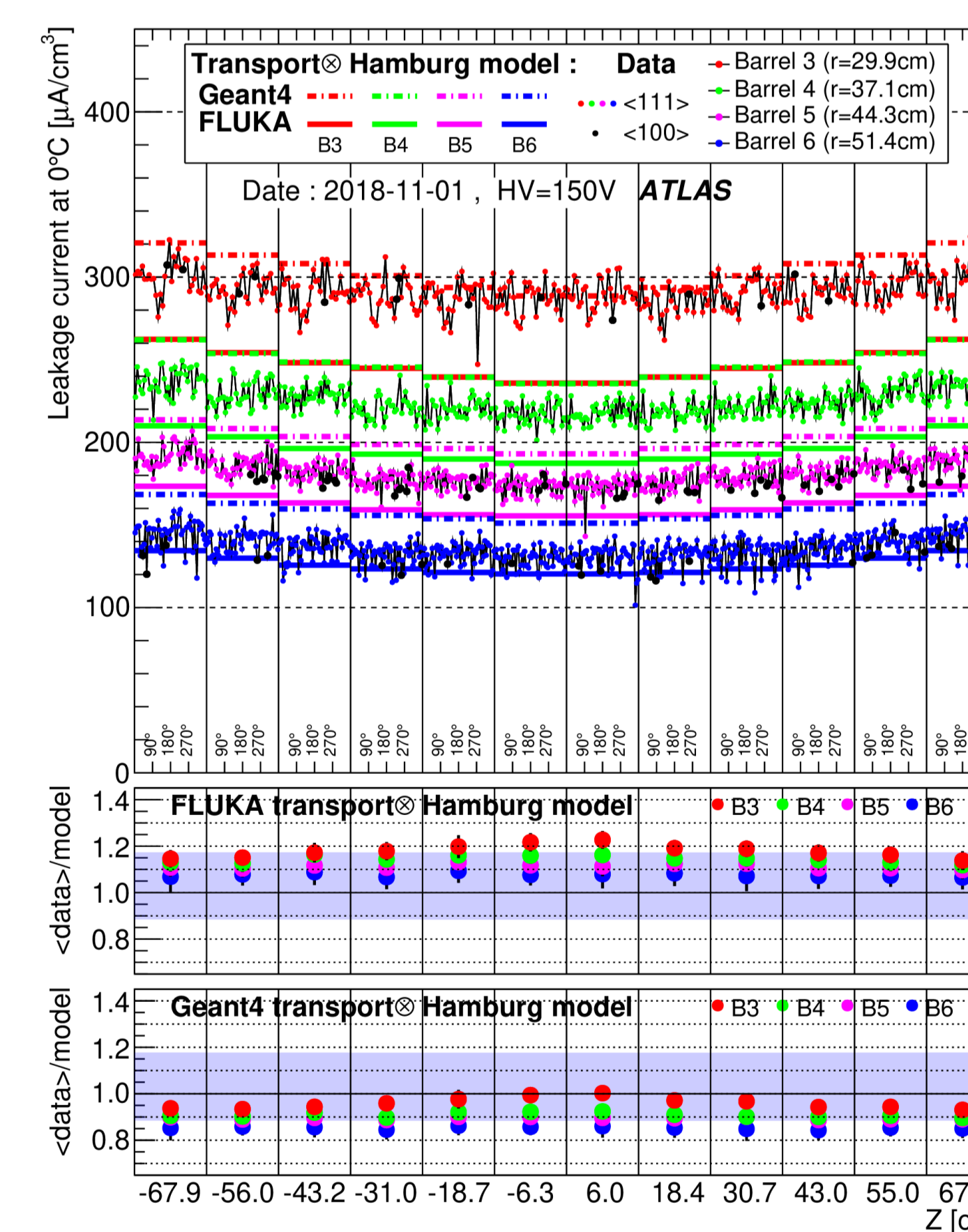
**Total fluence: 5.6 · 10<sup>13</sup> 1 MeV equivalent thermal neutrons.**

$ r _{index}$	$z$ [mm]	Barrel 3 ( $r = 299$ mm)	Barrel 4 ( $r = 371$ mm)	Barrel 5 ( $r = 443$ mm)	Barrel 6 ( $r = 514$ mm)
1	61.9	4.30	3.41	2.85	2.45
2	184.0	4.37	3.46	2.87	2.47
3	308.7	4.47	3.51	2.92	2.52
4	431.2	4.53	3.58	3.00	2.57
5	555.3	4.65	3.71	3.09	2.66
6	679.1	4.80	3.84	3.20	2.76

Disk	$z$ [mm]	Inner ( $r = 304.6$ mm)	Middle ( $r = 396.5$ mm)	Outer ( $r = 499.4$ mm)
1	853.8	-	3.86	3.07
2	934.0	5.12	3.89	3.08
3	1091.5	5.20	3.98	3.19
4	1299.9	5.27	4.14	3.31
5	1399.7	5.37	4.21	3.40
6	1771.4	5.69	4.47	3.67
7	2115.2	-	4.94	4.01
8	2505.0	-	5.74	4.66
9	2720.2	-	-	5.33

**Leakage Current** is thermally generated electron-hole pairs. If too large, might cause thermal runaway, forcing to lower HV, hence reducing the hit efficiency.



Normalised **leakage currents** per unit volume for all barrel modules (above) during Run 2 show **consistent  $I_{leak}$  within ~3%**.

Over the course of Run 2 it **increased ten fold** in agreement with predictions **within 30% uncertainty**.

**Reference:**  
To be published.

**Full Calibration Time: 1.5 hours**, typically every few weeks.

**Noise levels increased by 10-20%**. Still sufficiently low compared to the **threshold of 1 fc**.

## Conclusion

**SCT operated stably throughout Run 2**, with several new improvements: additional RODs and BOCs, more aggressive data compression, automatic recovery mechanisms for modules and RODs, improved cooling, calibration time reduced.

Leakage current and **Full Depletion Voltage** are accurately monitored, and more results are not listed here.

**Available for 99.9% of integrated luminosity**, achieved a **data quality efficiency of 99.85%**, thanks to the low **noise occupancy**, kept **below 5x10<sup>-4</sup>** and high **hit efficiency ~99%**.

Safe and stable operation is expected until end of Run3, with an integrated luminosity of ~200 fb<sup>-1</sup> with similar pileup levels.

**"Operation and performance of the ATLAS semiconductor tracker in LHC Run 2"**.