LOW-COST MODULAR PLATFORM FOR CUSTOM ELECTRONICS IN RADIATION-EXPOSED AND RADIATION-FREE AREAS AT CERN

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Abstract

The CERN control system is comprised of multiple layers of hardware and software that extend from the hardware deployed close to the machine, up to the software running on computers that operators use for control and monitoring. A new centrally supported service is being developed for the layers closest to the accelerator: Distributed I/O and the Fieldbus, targeting both radiation-free and radiation-exposed areas. A key aspect of this project is the selection of industrial standards for the layers, which are currently dominated by custom, in-house designed solutions. Regarding the Distributed I/O layer, this paper describes how we are adapting an industrial crate standard to be suitable as the low-cost modular hardware platform for remote analog and digital I/O applications in radiation-exposed as well as radiation-free areas. We are designing a low cost 3U chassis with a standardized backplane accompanied by a radiation tolerant, switched-mode power supply and an FPGA-based System Board that houses the Fieldbus communication interface.

INTRODUCTION

In the years 2024–25, CERN's Large Hadron Collider (LHC) will undergo a major upgrade [1]. The High Luminosity LHC (HL-LHC) will provide instantaneous luminosities a factor of five larger than the LHC nominal value. To achieve the physics targets several new technologies will be introduced to the accelerator and many systems will be renovated to increase the overall machine availability by 20 %.

The HL-LHC will place challenging demands on data acquisition to/from the accelerator components which need to be controlled and diagnosed, such as the new Nb_3Sn magnets. The need for larger amounts of diagnostics information will result in a requirement for more throughput in the lower layers of the control system and will therefore affect the electronics in this tier and the communication links used to send the information up the controls stack. The current custom electronics–based controls architecture comprises the following three hardware layers (Fig. 1):

- **Front-end Tier:** a powerful computer in various form factors (VME, PICMG 1.3, MTCA.4, *etc.*) that can host a variety of reusable electronic cards to control accelerator components by sending and receiving data and carrying out calculations in real-time.
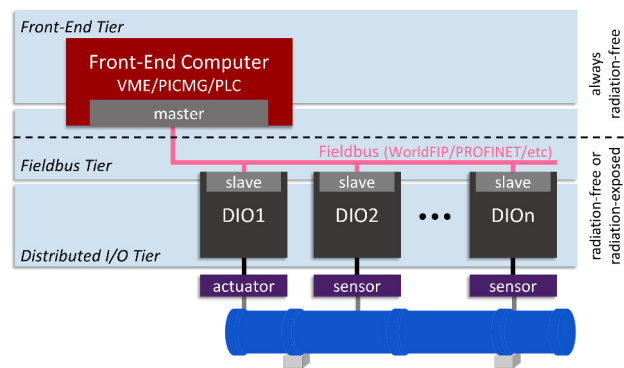
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Figure 1: Lowest layers of CERN's accelerator control system.

- **Fieldbus Tier:** a networking solution that ensures communication between the master in the front-end layer and a set of slaves in the distributed I/O tier

- **Distributed I/O Tier:** electronic modules that interface directly with an accelerator equipment in radiation-exposed or radiation-free areas, controlled by the master in the front-end tier over the fieldbus. These are usually FPGA–based boards sampling digital and analog inputs, driving outputs and performing various safety-critical operations.

Historically, in the front-end and fieldbus layers there has been a lot of standardization, sharing and reuse of design effort between equipment groups. However, in the distributed I/O layer, the lack of a generic, modular solution with simple and robust inter-module communication resulted in many custom-made developments in different form factors around CERN. With the Distributed I/O Tier (DI/OT) project we are designing a low-cost, reusable, modular hardware platform that can be easily customised to serve the requirements of various accelerator subsystems in both radiation-exposed and radiation-free areas. Introducing a standardisation in the distributed I/O layer of the control system automatically allows all users to benefit from modules designed by other groups or institutes. The main difference from the front-end tier modular electronics is less complexity, a simpler interface between boards hosted within a single crate and the provision of a radiation-tolerant variant of the hardware kit.

DISTRIBUTED I/O TIER HARDWARE KIT

A fundamental requirement for the DI/OT hardware platform, is basing it on existing industrial standards. The study

phase (described in [2]) concluded that a 3U[1] crate compliant with the CompactPCI Serial (CPCI-S.0) specification [3] is best suited for the requirements of accelerator applications at CERN. The standard features a robust connector targeting transportation applications and a fully passive backplane, which makes it suitable for systems in radiation-exposed areas.

The full DI/OT ecosystem depicted in Fig. 2 consists of a CPCI-S crate; an off-the-shelf CPCI-S 300W power supply; RaToPUS, a 100W radiation-tolerant switched-mode power supply; a radiation-tolerant System Board; a non-radiation-tolerant System Board and a set of interchangeable fieldbus communication mezzanines. The fieldbus mez-
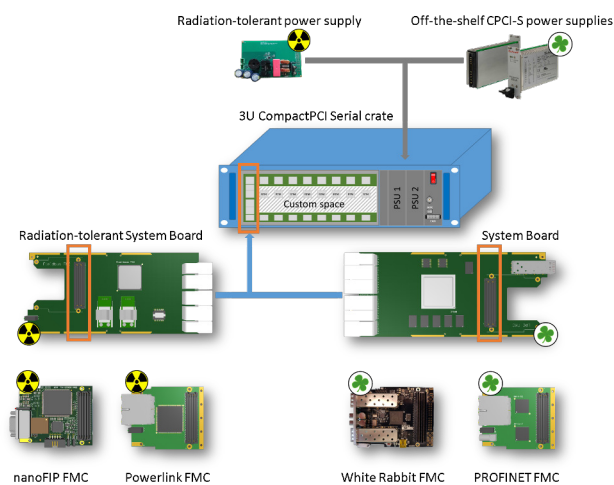

Figure 2: Distributed I/O Tier hardware kit.

zanines are designed in compliance with the ANSI/VITA 57.1-2008 FPGA Mezzanine Card (FMC) standard. They implement various communication technologies ensuring control and data exchange with the front-end tier computer. Several protocols are supported to cater for different needs of installations in radiation-exposed (WorldFIP, Ethernet-POWERLINK) and radiation-free areas (White Rabbit, PROFINET). The System Board is an FPGA-based card which acts as the crate controller. On one side it features an FMC connector to host one of the fieldbus communication mezzanines. On the other side, it is equipped with the backplane connector to interface with all other boards in the crate – the so called Peripheral Boards. A small fraction of its FPGA resources is dedicated to implementing general crate monitoring services (temperatures, voltage and current levels, fan speeds) while the rest of it is free to the user to implement any application-specific early data processing algorithms.

A user of the DI/OT ecosystem would assemble a desired configuration from the aforementioned components depending on the chosen communication protocol and area where it is going to be deployed:

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[1] 1U = 44.45 mm

- **radiation-exposed:** DI/OT crate with RaToPUS, radiation-tolerant System Board and either WorldFIP or Ethernet-POWERLINK FMC mezzanine;

- **radiation-free:** DI/OT crate with any off-the-shelf CPCI-S power supply, non-radiation-tolerant System Board, any of the available FMC mezzanines.

An instance of DI/OT hardware would be further customised by adding application-specific Peripheral Boards and FPGA firmware running on the System Board.

CRATE SPECIFICATION

The fact that the DI/OT crate complies with the CPCI-S specification, enables designers to use off-the-shelf crates for lab prototyping as well as standardizes the voltages, connectors and monitoring interfaces. However, the crates currently available on the market are not suitable "as-is" for wide deployments in CERN accelerators mainly due to limited boards real estate and elevated kit cost. To overcome those, an Open Hardware crate and CPCI-S backplane are designed in the frame of the project [4].

The crate enclosure (Fig. 3) is assembled using 3U sub-rack components compatible with the IEC 60297-3 and IEEE 1101.10-1996 mechanical standards. These are low-cost aluminum elements available in the products portfolio of all major crate vendors. Furthermore, to allow more efficient passive cooling, especially for the crates deployed in radiation-exposed areas of accelerator tunnels, the dimensions of the front space of the System Board and Peripheral Boards is increased. Comparing to the standard CPCI-S configuration, where the zone for each card is limited to $100\,\text{mm} \times 160\,\text{mm} \times 4\,\text{HP}$[2], the DI/OT crate can host longer, 220 mm, and wider, 6 HP, front boards. To make it possible a customized backplane was designed, with additional spacing between the slots, and mounted deeper in the chassis.
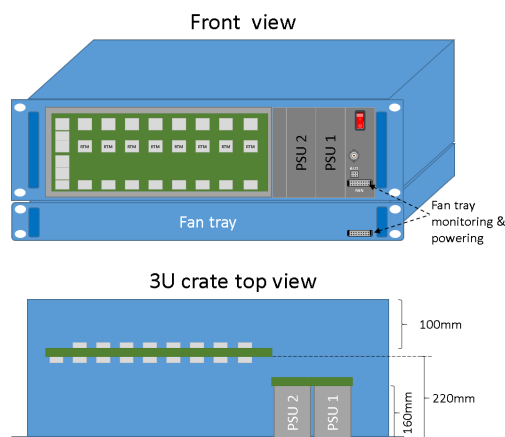

Figure 3: DI/OT crate mockup.

The application-specific Peripheral Boards can interface directly with sensors and actuators through their front panel.

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[2] 1 Horizontal Pitch(HP) = 5.08 mm

Alternatively, the chassis and the backplane offer a possibility to host Rear Transition Modules (RTMs). The RTMs are usually fully passive boards that provide an interface with external equipment through a direct RTM connector to the corresponding Peripheral Board. This way, in case of an emergency intervention, one can replace a faulty front board without the need of de-cabling. To further increase the availability of DI/OT systems, the crate provides dual modular redundancy power supplies in load-sharing configuration.

DI/OT systems deployed in radiation-free areas may feature complex and powerful digital circuits requiring forced airflow for heat dissipation. The DI/OT hardware kit includes an optional 1U fan tray that could be mounted either below or above the main 3U crate. For reliability reasons, electronics deployed in radiation-exposed areas rely mostly on passive, conduction cooling. To enable more power-consuming electronics to be deployed in radiation environments, the DI/OT kit provides a radiation-tolerant fan control module. Both powering and monitoring of the fan tray are provided through a single connector.

DI/OT CPCI-S Backplane

The 9-slot DI/OT backplane was designed in KiCad [5], a free and open source EDA (Electronics Design Automation) suite, according to the CompactPCI Serial specification. Figure 4 presents a 3D render of both sides of the backplane design. The project is licensed under the CERN Open
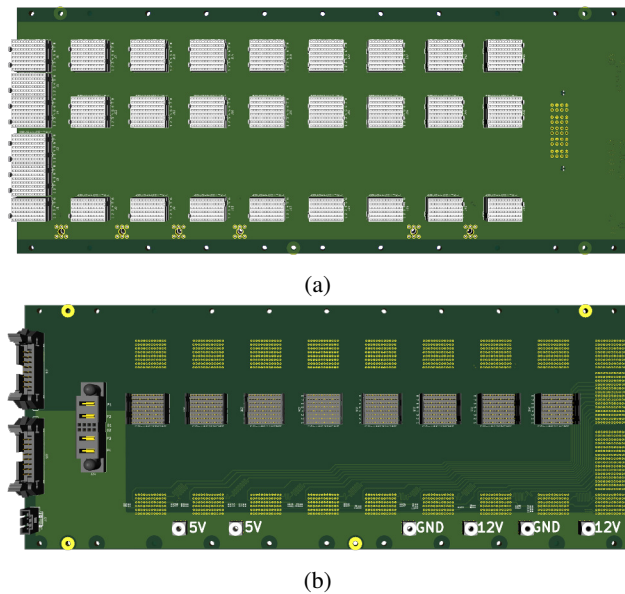

(a)

(b)

Figure 4: DI/OT backplane front(a) and back(b) 3D render.

Hardware License and published in the Open Hardware Repository [4]. Therefore, not only does it serve the needs of CERN DI/OT applications, but has the potential of becoming a powerful platform that can be easily and freely used as a base for further modifications and customization.

The DI/OT backplane features a set of Amphenol Airmax connectors following the CPCI-S standard. The System

Slot is populated with a full range of 6 connectors, P1 to P6 (where P1 is the lowest, close to the bottom edge of the board), while Peripheral Slots have only P1, P4 and P6. P1 and P6 are used for communication with the System Slot, while P4 is defined in the standard as rear board connector and interfaces directly a Peripheral Board with its Rear Transition Module (RTM). While CPCI-S manufacturers provide backplanes of various number of slots, the most widely spread configuration furnishes 9 slots and the DI/OT backplane follows this trend. It provides interfaces between 8 Peripheral Slots and the System Slot by a set of differential pairs in a star topology and a number of multi-drop single-ended lines. Although the topology of all interconnections (Fig. 5) has been preserved as specified by CPCI-S, their definition has been generalised and abstracted from the communication protocols. Instead of using complex busses like PCI-Express, USB and SATA a simple inter-board communication technology (such as high-speed SPI) with automatic identification of hardware modules is supported by the System Board FPGA firmware. This choice is more suitable especially for electronics in radiation-exposed areas, where the complexity of a system must be reduced as much as possible.
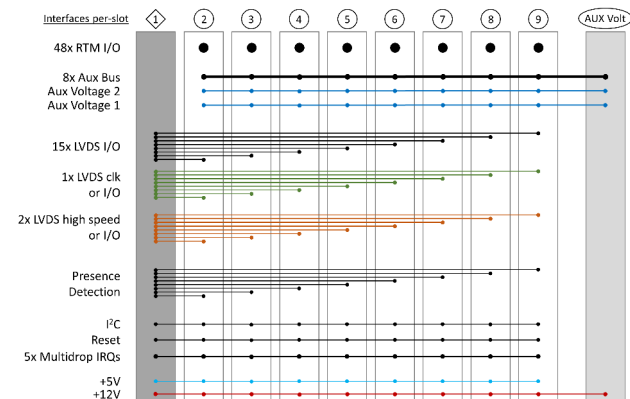

Figure 5: DI/OT backplane topology
(1: System Slot; 2-9: Peripheral Slots).

The DI/OT backplane provides a star topology of 144 LVDS lanes in total (18 LVDS lanes per Peripheral Slot), as can be seen in Fig. 5. They are used as differential or single-ended I/Os to implement communication between the System and Peripheral Boards. Out of those, 1 LVDS lane per Peripheral Slot is reserved for the distribution of low-jitter clock and 2 LVDS lanes are designated for high-speed communication (using FPGA Multi-Gigabit Transceivers). Additionally, a set of the following shared, single-ended lines is available. The *Reset* line is driven by the System Slot and lets the System Board reset all the Peripheral Boards in the crate. A set of 5 multidrop lines (*Multidrop IRQs* in Fig. 5) can be used as interrupt lines of 5 priorities, or for any other one-to-many signaling. Despite the fact that DI/OT applications do not require a hot-plug functionality, a star of single-ended presence detection signals and a service I²C

bus (shared among all the slots) is available. Those will be used for Peripheral Board identification and thus automatic discovery of a running DI/OT crate configuration.

Regarding powering, the DI/OT backplane preserves full compatibility with CPCI-S and offers extensions. In the default scenario, each board receives through the P1 connector two rails: +5V (standby power) and +12V (payload power). The former is of very limited power (up to 10 W combined through all slots) while the second shall be considered as the main power source for digital and analog circuits. Depending on the needs of a particular board, it shall be equipped with local Point-Of-Load (POL) DC/DC or linear regulators to produce the voltages required to its operation.

Furthermore, the DI/OT backplane provides the means for additional distribution of two auxiliary voltages to all Peripheral Slots. The typical CERN Peripheral Board will be equipped with an analog front-end to interface with very precise measurement circuitry (*e.g.* for measuring the position of magnets with micrometer accuracy). This requires some low-power bias voltage (*e.g.* +15V, -15V). To limit the complexity of the whole system, the DI/OT backplane provides an *AUX Volt* connector in the back. It is meant to host an auxiliary power supply card that accepts +12V and produces with local DC/DC or linear regulators the desired voltages (*AUX Voltage 1*, *AUX Voltage 2* in Fig. 5). The auxiliary voltages are then provided to all Peripheral Slots using the customized distribution through P4 connectors. While 8 signaling pins of every P4 connector are utilized for low impedance auxiliary voltage power rails, another 8 signaling pins are available for custom inter-board communication and the remaining 48 signaling pins are for direct interfacing with the rear boards (RTMs).

CRATE POWER SUPPLIES

For radiation-free areas, the DI/OT crate will be equipped with off-the-shelf 300W CPCI-S power supplies. However, for radiation-exposed applications, such a straightforward approach cannot be applied. Regular, switched-mode power supplies are known to fail in radiation due to both Single Event Effects (SEE) and Total Ionizing Dose (TID). Therefore, the vast majority of radiation-tolerant electronics currently deployed at CERN is equipped with linear power supplies. Those are less complex and thus more resilient to radiation-related effects. However, linear power supplies suffer from poor efficiency, large heat dissipation and a form factor dictated by the bulky 50 Hz transformer for output powers in the order of 100 W, as required by the DI/OT.

RaToPUS, Radiation-Tolerant Power Supply

RaToPUS [6] is a 100 W AC/DC radiation-tolerant power supply mechanically compliant with the CompactPCI Serial standard (CPCI-S.0). It takes in a universal AC input (90–230 Vac, 50/60 Hz) and delivers up to 100 W on its payload channel (12 Vdc) and up to 10 W on a standby channel (5 Vdc). RaToPUS consists of two stages (Fig. 6): a non-isolated Power Factor Correcting (PFC) AC/DC stage

implemented by a PFC buck topology [7], followed by two independent, isolated DC/DC stages implemented using the Active-Clamp Forward (ACF) topology [8]. The DC link between the AC/DC and the DC/DC stages is nominally 48 V (range: 36–72 V). This way, systems that are directly powered from 48 V DC can benefit from the same design.
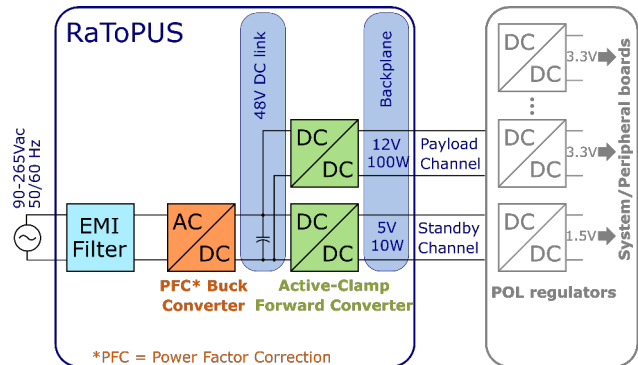

Figure 6: Radiation-tolerant power supply for DI/OT – RaToPUS.

The first prototype of the resonant-reset forward converter [9] DC/DC stage was based on a radiation-hard PWM controller chip designed at CERN for electronics in the physics experiments (FEAST 2.1 [10]). However, this straightforward approach showed limitations at the early stage of the design. The resonant-reset forward converter can require a large blocking voltage (up to 250 V) on the main MOSFET (due to its sinusoidal peaking). Considering a 50 % derating for rad-hardness against Single Event Burnouts (SEB), the MOSFET voltage rating would have been at least 500 V, for the DC link of only 48 V. The resulting parasitics (on-state resistance and parasitic capacitances) of this high-voltage MOSFET lead to large conduction and switching losses, thus yielding only a 60 % efficiency as per our experiments. Moreover, the FEAST-based controller, originally designed for low power applications (10 W), does not lend itself to the required modifications in a higher-power application (up to 100 W). The minimum specified switching frequency is 1 MHz which is too high for a 100 W power supply unless wide-bandgap devices are used. In addition, the stability of the regulation loop is heavily affected by the fact that the type-III compensation network for the error amplifier cannot be adequately modified as it is completely inside the FEAST chip, with fixed values of resistors and capacitors.

The reviewed approach for the DC/DC stage design (currently ongoing) uses an ACF topology which in consort with synchronous rectification on the secondary side can achieve a potential DC/DC efficiency of 95 %. The chosen controller integrated circuit for this stage is a standard current-mode PWM controller (UC3845) with external compensation network, soft-start circuit, and slope compensation. Various pin-to-pin compatible versions of this chip are available in a SO-8 package from different semiconductor manufacturers.
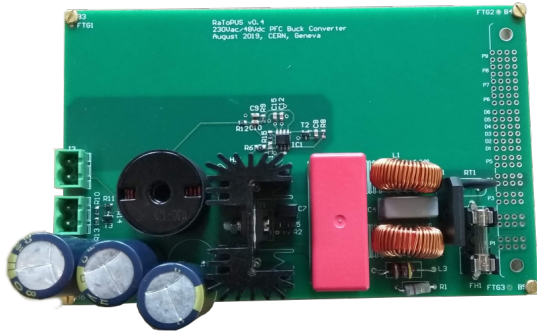
Figure 7: Prototype of PFC buck AC/DC converter, 230 Vac-to-48 Vdc.

Figure 8: DI/OT general-purpose monitoring module – MoniMod.

This makes it easy to change the controller circuit without having to redesign the PCB in case radiation tests reveal issues with a particular part.

Regarding the AC/DC stage, the first prototype of the PFC buck AC/DC converter has already been designed and is currently being tested (Fig. 7). It is based on the same controller integrated circuit (UC3845) albeit with a different compensation network.

MONIMOD, THE MONITORING MODULE

MoniMod [11] is the general-purpose, radiation-tolerant, small form factor module of the DI/OT kit. For RaToPUS it provides basic monitoring functionality (voltages, currents, temperatures) and a standard PMBus (Power Management Bus) interface to the System Board. Using PMBus ensures conformity with other off-the-shelf CPCI-S power supplies. For the 1U fan tray that can be optionally mounted on the the DI/OT crate, it provides temperature measurements, fan speed regulation and PMBus communication with the System Board.

MoniMod is based on a 32-bit Cortex-M0+ microcontroller (ATSAMD21G18). The 12-bit multi-channel ADC (Analog-to-Digital Converter) integrated with the microcontroller is used to provide voltage and current monitoring for up to three different power rails, as well as temperature monitoring by means of up to three externally connected sensors (*e.g.* LM61, PT100, PT1000). The PMBus-compatible I^2C peripheral facilitates the implementation of the PMBus protocol; most of the low-level protocol work is offloaded to the peripheral, keeping the core processor mostly free. The PWM (Pulse Width Modulation) capabilities of the microcontroller are combined with three buck converter–based drivers to enable regulating the speed of up to three 12 V fans (without needing the fans to be PWM-capable themselves). The fan speed can also be monitored, for fans that provide a tachometer. The board's small form factor of 38.1×63.5 mm makes its integration into the limited space of a standard CPCI-S PSU (Power Supply Unit) possible – this size will be further reduced by omitting the fan drivers for a PSU-specific version.
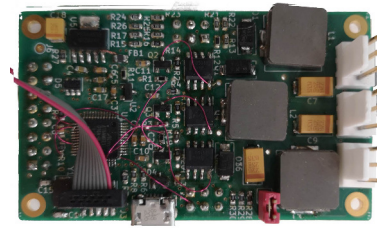
The microcontroller firmware implements a minimal subset of the PMBus protocol to provide access to the monitoring data; at the same time, suitable ad hoc extensions were added to enable switching to – and controlling – an I^2C-supporting bootloader that provides the System Board with the means to remotely update the MoniMod firmware.

The selection of the microcontroller for the MoniMod was governed by radiation tolerance requirements: the ATSAMD21G18 has been tested to respond well with respect to TID effects. Although both its core and the multi-channel ADC do intermittently misbehave once exposed to radiation, these effects can be mitigated: using the integrated watchdog can bring the system back from core faults, employing blind scrubbing can keep the ADC peripheral configuration registers in check and applying simple filtering on the measurement data will remove most SEU (Single Event Upset)-induced errors. Additional software mitigation techniques, such as control flow checking and software TMR will be evaluated. Finally, as a definitive recovery measure, a dedicated hard-reset line allows the System Board FPGA to promptly power cycle the whole MoniMod monitoring module in case it stops responding to PMBus requests. Since its functionality is not critical to the rest of the DI/OT crate, the system can afford resetting or even power cycling the whole monitoring module during operation.

At the time of writing, the first prototype of MoniMod has been produced and validated in the lab (see Fig. 8). The next steps of its development process include radiation test campaigns as well as detailed reliability studies.

FPGA-BASED SYSTEM BOARDS

For the proof-of-concept phase of the project, the DI/OT System board was based on an the already existing CERN radiation-tolerant board, the *GEFE* [12]. *GEFE* is a radiation-tolerant FMC carrier that was originally designed for the Multi-Orbit POsition System SPS (MOPOS). Since its functionality, physical dimensions and radiation tolerance matched the requirements of the DI/OT project, a modified *GEFE* was designed and used it as the very first DI/OT System Board. It features an FMC connector to host a fieldbus communication mezzanine (WorldFIP mezzanine plugged on top of the System Board in Fig. 9), a set of 6 Am-
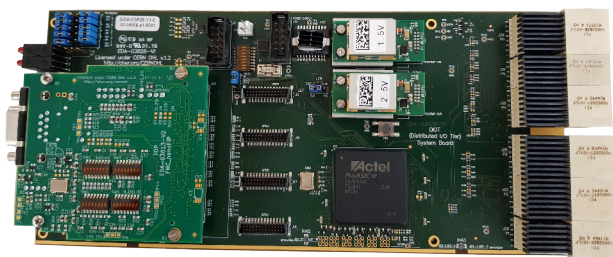
Figure 9: Proof of concept DI/OT System Board with World-FIP FMC mezzanine.

phenol Airmax backplane connectors and a ProASIC3-3000 Flash-based FPGA.

Despite the fact that ProASIC3 has proven its reliability in several CERN developments covering radiation-exposed areas, it provides quite a limited number of resources comparing to modern FPGA families. The available space is even more confined if one takes into account that all registers have to be triplicated at the synthesis stage and voters need to be instantiated to ensure resilience to single event effects (SEE). Those reasons led us into researching a different FPGA family for the final design of a radiation-tolerant System Board. An interesting alternative has been provided by *nanoXplore*. This European company has launched low-cost, radiation-hardened-by-design, SRAM-based FPGAs manufactured on the STM C65 space process. Being radiation-hard by design, those do not require triplication or voting techniques and offer block RAM memories with embedded ECC (Error Correcting Code) protection. At the time of writing, we are conducting a set of radiation test campaigns in Paul Scherrer Institute to evaluate the performance of *NG_Medium* FPGAs.

To cover the more demanding needs of systems outside of radiation, the non-radiation-tolerant variant of the DI/OT System Board was specified [13]. It will have the same form factor and a set of FMC and backplane connectors as the proof-of-concept design described earlier. However, the non-radiation-tolerant variant will be a fully featured White Rabbit [14] node and will be equipped with a much more powerful System On Chip, Xilinx Zynq Ultrascale+ ZU7 (see the project page [13] for the full specification).

FIELDBUS

In radiation-exposed areas, at the time of writing, the only fieldbus for the CERN accelerators is WorldFIP [15]. In radiation-free areas the most common protocols are PROFINET and legacy PROFIBUS. The DI/OT kit offers a selection of interchangeable communication solutions to cover the different performance and environment requirements. In radiation-free zones, the DI/OT offering includes:

- **PROFINET:** for applications requiring mainly integration with off-the-shelf Industrial Ethernet equipment;

- **White Rabbit:**, for applications requiring a redundant link for high-bandwidth and sub-ns synchronisation [16].

In radiation-exposed zones, the DI/OT offering includes:

- **WorldFIP:** for applications requiring compatibility with existing LHC equipment;

- **Ethernet-POWERLINK:** for applications requiring higher bandwidth or integration with off-the-shelf Industrial Ethernet equipment.

Radiation-Tolerant Ethernet-POWERLINK

While WorldFIP has been operating reliably since the first LHC start-up, its bandwidth is limited to 2.5 Mbps. A market review for 100 Mbps Ethernet, µs-level synchronization and up to 50 slaves per segment, explored leading Industrial Ethernet technologies such as PROFINET, EtherNet/IP and EtherCAT. It concluded to the selection of Ethernet-POWERLINK, as the radiation-tolerant fieldbus for HL-LHC accelerator applications. The selection was based on the fact that Ethernet-POWERLINK is the simplest of the Industrial Ethernet protocols which makes it feasible to implement a slave-node in a radiation-tolerant FPGA. Moreover, Ethernet-POWERLINK features an open-source implementation of its stack which gives direct access to reliable source code. A mature option for making radiation-tolerant digital designs, is using flash-based FPGAs, as is the case, for example, of the *GEFE* board described in the previous section. FPGA families like ProASIC3 have proven to be reliable for radiation levels in the order of 400 Gy TID, 1E+13 p/cm^2 HEH and for a compact design like a fieldbus slave it is the optimal solution, at the time of writing. The FPGA configuration is stored in flash-cells which are immune to SEUs in the LHC environment. The pure logic is protected from SEUs by applying triple-modular-redundancy of the flip-flops, followed by voting.
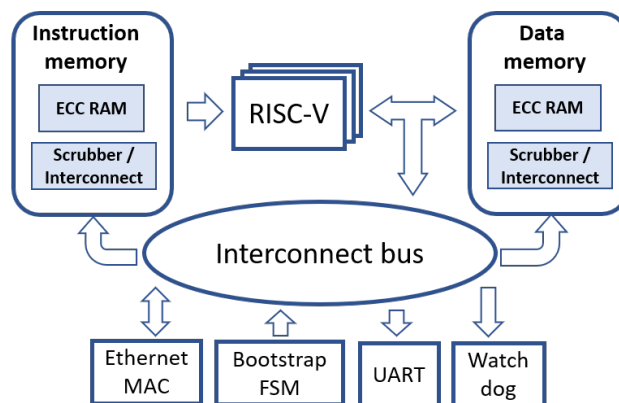

Figure 10: Simplified block diagram of the rad-tol POWERLINK implementation in FPGA.

A more complex approach to radiation-tolerant digital designs, still within flash-based FPGAs, is the instantiation of a soft-core processor inside the FPGA. While re-
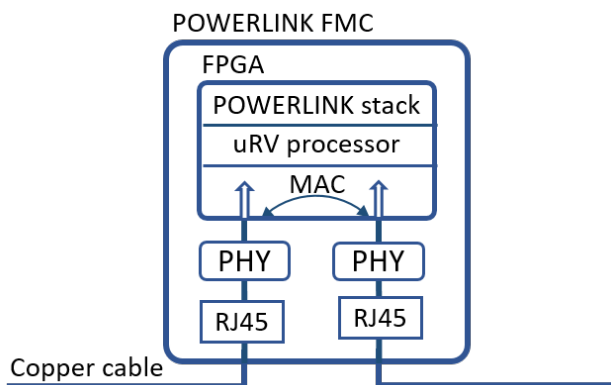
POWERLINK FMC

Figure 11: Simplified block diagram of the Ethernet-POWERLINK FMC.

placing a complex HDL design with a real-time processor running software is a wide-spread technique outside of radiation, it has not yet been established under radiation. Figure 10 shows the implementation of a radiation-tolerant Ethernet-POWERLINK stack inside a flash-based FPGA. A RISC-V core is triplicated and runs software stored in Error-Correction-Code (ECC) protected memory (instruction memory). The data for the program resides in a separate ECC-protected memory. Both memories are dual-port, one port is connected directly to the processor, while the latter one is connected to a "scrubber". The scrubber is a Finite State Machine (FSM) polling the ECC RAM, sequentially reading the entire address space. In this way, each word is exercised, avoiding the risk of error accumulation. An interconnect bus is used for the processor to communicate with several peripherals: Ethernet MAC, UART, Watchdog and the bootstrap FSM. The Ethernet MAC can directly read the data memory using its DMA engine, while writing is constrained to a specific region of the addressing space due to reliability constrains. The bootstrap FSM is used at start-up to initialize the instruction and data memory. Each peripheral and scrubbers are designed to be fail-safe and triplicated at gate level for radiation hardening purposes.

For the implementation of the physical layer, several Commercial-Off-The-Shelf (COTS) PHY chips are being validated by radiation test campaigns. The envisaged network topology adapted to the LHC needs requires the slave-nodes to be daisy-chained. As Fig. 11 shows, each slave-node is a dual-port switch.

SUMMARY

The DI/OT kit is a low-cost modular platform for custom electronics. Being generic and based on standards it offers fast integration by the users. The kit consists of a standardised simple enclosure and a fully-passive CPCI Serial backplane for eight application-specific boards and one System Board. Depending on the accelerator environment, radiation-free or radiation-exposed, it offers adapted redundant power supplies, monitoring modules, fan-trays and the FPGA-based System Board. A set of interchangeable FMC mezzanines are designed to be plugged on the System Board to provide communication with the higher-layers of the control system.

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