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THE DETECTOR CONTROL SYSTEM OF THE MUON FORWARD TRACKER FOR THE ALICE EXPERIMENT AT LHC

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Abstract

The ALICE experiment is presently finalizing its upgrade program toward the LHC Run 3 starting in 2021. The Muon Forward Tracker (MFT) is one of the new detectors developed in the framework of the ALICE upgrade program. In addition, the experiment is upgrading its whole online and offline (O^2) framework in order to dispose of the data volume from all ALICE detectors. In the context of the O^2, the slow control data are also processed together with the physics data. Therefore, the ALICE central Detector Control System (DCS) must be upgraded to operate within the O^2. The MFT DCS has been developed following the new ALICE central DCS strategy. The Finite State Machine (FSM) for hierarchical control is designed as a part of the MFT DCS. It was confirmed that the FSM has correct behaviour by changes of element states by a simulator. Furthermore, the MFT DCS successfully operates using a simplified but realistic test bench based on the final MFT elements.

INTRODUCTION

ALICE (A Large Ion Collider Experiment) is one of the LHC experiments at CERN. It focuses on the heavy-ion program to understand the Quark-Gluon Plasma (QGP), a state of deconfined quarks and gluons described by Quantum Chromodynamics.

During the first ten years of operation, the ALICE experiment has produced precise and original data in order to characterize the QGP formed in Pb-Pb collisions at LHC. Its upgrade programs toward the forthcoming LHC Run 3 in 2021 are being developed to realize measurements of rare proves allowing further study of the QGP. In the framework of this upgrade program, the Muon Forward Tracker (MFT) [1] is a new detector being installed in the forward region. In addition, the O^2 [2] is a new computing system to handle the data readout and reconstruction from all ALICE detectors together with the detector monitoring and slow control data. Finally, a totally new Detector Control System (DCS) for the MFT is being developed. In this report, we present the latest status of the MFT DCS development.

MUON FORWARD TRACKER

The MFT is a new silicon pixel detector devoted to the muon detection at forward rapidity in the range $-3.6 < \eta < -2.5$. The MFT will be installed between the collision point and the hadron absorber in front of the current muon spectrometer. The MFT improves the capability of muon tracking by track matching with the present muon spectrometer. Thanks to the high accuracy of determination of the displaced muon generation vertices by the MFT, prompt J/ψ and secondary J/ψ from B-meson decays can be separated. Moreover, a better resolution of the di-muon invariant mass spectrum can be achieved especially in the low-mass region.

The MFT consists of 2 half cones made of 5 disks (Fig. 1). Each being composed of 2 detection planes. Each plane is made of hybrid integrated circuits housing Monolithic Active Pixel Sensors (MAPS), which are a new type of sil-icon pixel detectors integrating both sensor and readout electronics in a single detection device based on the CMOS technology [3]. The MAPS allow a low material budget and effective signal collection.

A ladder has typically 2-5 sensor chips assembled on a flexible circuit made in Aluminum. A total of 280 ladders equipped with 936 sensor chips is needed for the full MFT. Each half detection plane of a disk is expediently separated into 4 zones consisting of 3 or 4 ladders. The power generation is handled locally in a Power Supply Unit equipped with DC-DC converters. A Readout Unit (RU) board collects the data from each zone.

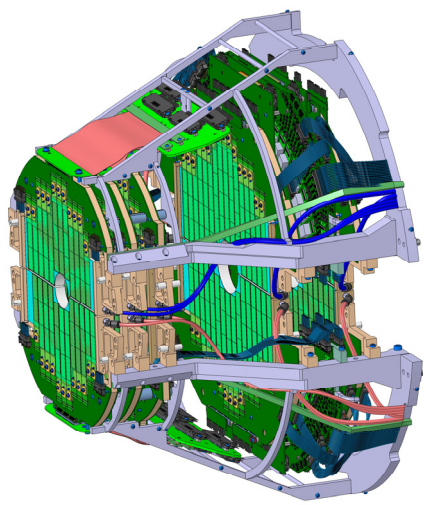

Figure 1: Schematic view of the MFT.

ALICE DCS IN THE CONTEXT OF O^2

The O2 is a new computing system in which online and offline systems are commonly merged. The slow control data share the data stream in the O2 facility with physics data from detectors. Detector conditions for each event are one of the ingredients for the data reduction in online reconstruction. Online data reduction is a very important process because the O2 farms need to handle raw data at a rate

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of 1.1 TB/s coming from the detectors. The Giga-Bit Transceiver (GBT) technology [4], which is developed by CERN, allows transfer of this large amount of data.

The ALICE central Detector Control System (DCS) must be upgraded to follow the O2 strategy. The ALICE central DCS introduces Alice Low level Front-End Device (ALFRED) [5] in the DCS data line to control data transfer with the GBT as shown in Fig. 2. The ALFRED is composed of ALF and FRED. The ALF is an interface between the FRED and detector FEE via the Common Readout Unit (CRU) on the First Level Processor (FLP). The FRED plays a role of translation of high-level words within the DCS to low-level words which are sent to the detector FEE as hexadecimal command sequences. It manages commands to multiple ALFs. Physics and detector condition data are stripped on the CRU. The communication protocol via Ethernet between the WinCC Open Architecture (OA), the FRED, and the FLPs is the Distributed Information Management system (DIM) [6], which is based on the client/server paradigm.

Also, the ALICE DCS uses specially designed ASIC for slow control integrated in the framework of the GBT, called the GBT Slow Control Adapter (GBT-SCA) [7]. The GBT-SCA integrates 16 I2C channels, 1 SPI, 1 JTAG, 32 General Purpose I/O (GPIO), 31 ADC, and 4 DAC channels.

DETECTOR CONTROL SYSTEM FOR MUON FORWARD TRACKER

The MFT DCS follows the upgrade strategy of the ALICE central DCS and the DCS framework of CERN. WinCC OA is a basis of supervisory control and data acquisition of CERN. Also, Joint COntrol Project Framework (JCOP Fw) produced by CERN is installed on WinCC OA to provide the standard DCS solutions.

General Architecture

Hardware architecture of the MFT DCS is divided into three categories, power supply, detector operation including physics data stream, and a cooling system.

Table 1: CAEN Modules for the MFT

Modules	#	Type
A4527	1	System main frame
A1676A	1	Controller for EASY system
A3486	2	48 V power supply for EASY
EASY3000	4	Crates for hostile area
A3009	12	Radiation and magnetic tolerant power supply boards
A3006	2	Radiation and magnetic tolerant power supply boards

CAEN products are used as a power supply system of the MFT as listed in Table 1. A4527 as a main frame of the CAEN system communicates with the WinCC OA through OPC. A3009 and A3006 modules supply low voltage to the PSU and the RU boards.

One FRED and 11 CRUs on 6 FLPs are installed in the data stream of the MFT DCS. 10 CRUs split raw data from the silicon sensors into physics data and DCS data and the other CRU transmits hexadecimal data between the FRED and the GBT-SCAs. The data stream of the MFT DCS is illustrated in Fig. 2.

Readout Unit Boards and Sensor Chips

The RUs are also controlled by the MFT DCS. One GBT-SCA and 2 PT1000 temperature sensors are placed on each RU. PT1000s are connected to 2 ADC ports on the GBT-SCA and their values are read each 10 seconds.

Data from the sensor chips are sent to the RUs. Then, both data of the sensor chips and the RUs are delivered to the FLP. They are split into condition data and physics data on the CRUs. And then, the condition data are transmitted to WinCC OA via the ALFRED.

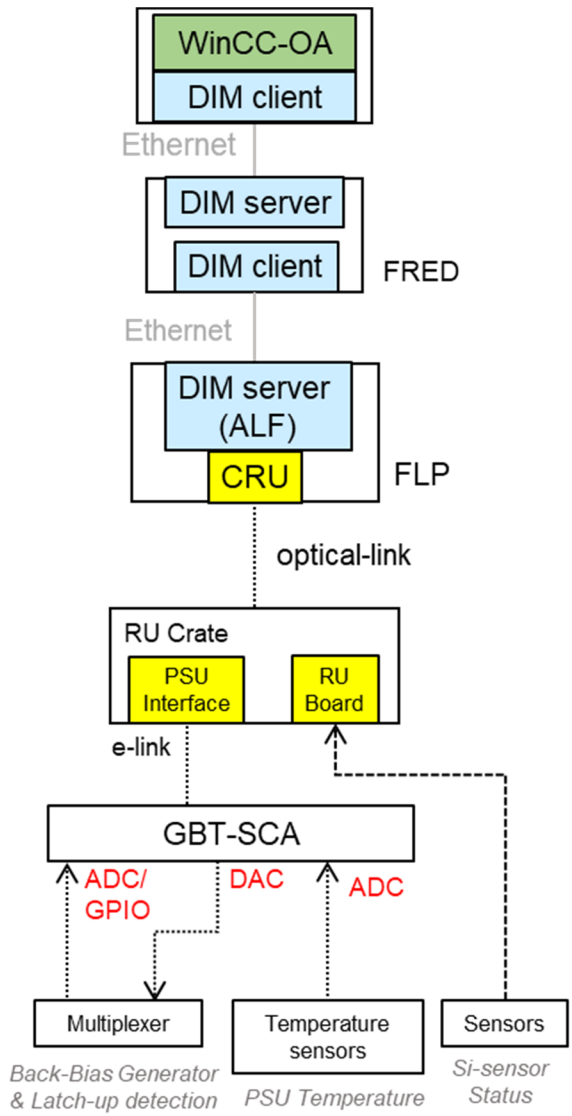

Figure 2: Data stream in the MFT DCS.

Power Supply Unit

The DC-DC converters, the back-bias generators, and the GBT-SCAs are placed on a Power Supply Unit (PSU)

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which is integrated inside the detector, very close to the active elements. Multiplexed outputs from the DAC ports and the analogue switch and buffer/blocker are employed, due to the limited space of the PSU and the limited ports on the GBT-SCA.

One DAC port is used to obtain four analogue voltages via the buffer/blocker to one zone (Fig. 3). The DAC output voltage is corresponding to the input of the latch-up detections and the back-bias generator. Then, one GBT-SCA is enough to generate power for the one detection plane working.

The multiplexed output voltage of the DAC is encoded every 10 milliseconds (Fig. 4). Only one switch is on at one time and all switches are off during transitions. Four continuous voltages at the output of the buffer/blocker (Fig. 5) are generated.

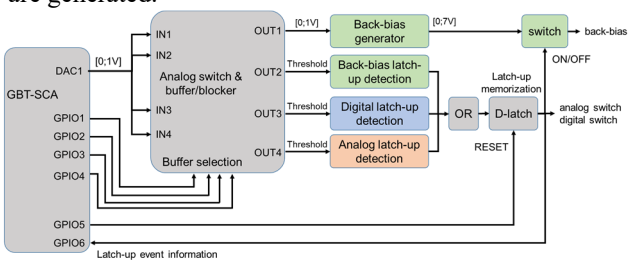

Figure 3: Image of the buffer/blocker.

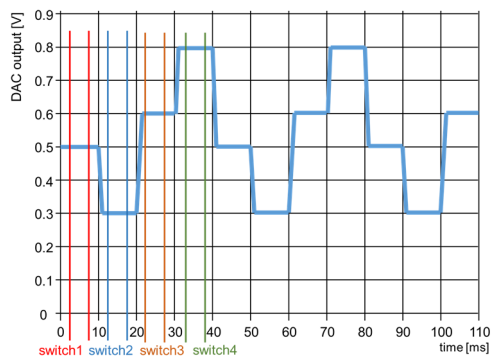

Figure 4: Multiplexed signal from a DAC port.

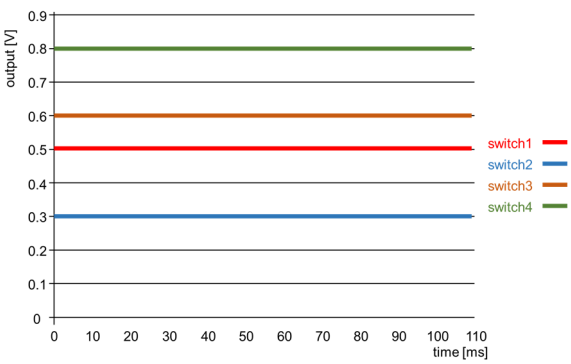

Figure 5: Buffer output voltages from analogue switch and buffer/blocker.

GBT-SCAs on the MFT DCS

20 GBT-SCAs are integrated on the PSU for the DCS of the MFT. One GBT-SCA chip is assigned to a half detection plane. The list of the used GBT-SCA ports per half-plane is shown in Table 2.

Table 2: GBT-SCA Ports in Use

Ports on GBT-SCA	#	Usage
GPIO	24	Buffer selection and latch-up monitoring
ADC (disk 0)	28	The same as ADC for disk 1 Besides, the temperature in the MFT volume, humidity, and the temperature of input cooling water to the PSU
ADC (disk 1, 2, and 3)	25	Voltages and currents of digital and analogue, the latch-up status of the PSUs, temperatures of the disks, and bias voltage
ADC (disk 4)	27	The same as ADC for disk 1 Additionally, the temperature of the MFT volume and the temperature of the output cooling water from the PSU
DAC	4	Signals for the PSU

DEVELOPMENT OF FSM

A Finite State Machine (FSM) is a core of hierarchical control of the MFT. The JCOP Fw provides tools of the FSM. The FSM tree structure is illustrated as shown in Fig. 6. Control Units are logical nodes and their states are de-fined by children's states. Device Units are physical nodes attached to device channels. A detector part and an infra-structure part are major parts in the MFT FSM. The infra-structure part is composed of the CAEN system and the cooling system.

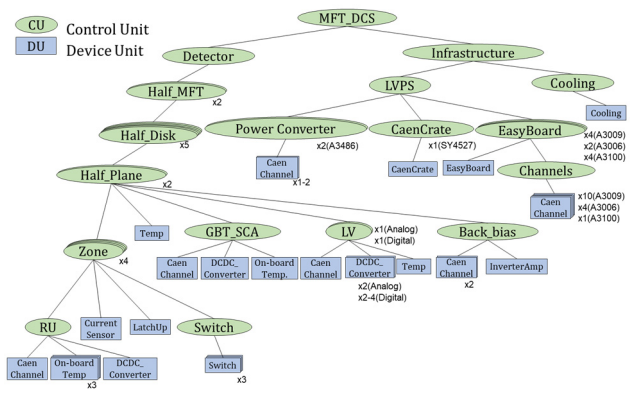

Figure 6: The tree structure of the FSM.

State diagrams are also designed for all nodes. The parent nodes need to know the children's states to transit their states accurately. Figure 7 shows the state diagram for the top node. The different states correspond to operational conditions of the detector according to the LHC status. SUPERSAFE means that the detector and channels of the

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power supply systems are OFF. The channels of A3009 and A3006 modules are ON but low voltage power for the RU boards and the sensor chips are not yet supplied in the SAFE state. Then, the FSM turns to the READY state, if physics data can be acquired with the RUs and the whole detector are ON. Whenever an error happens in any of the states of the top node, the state of the top node forcibly moves to the ERROR state.

WinCC OA provides Graphical User Interfaces (GUIs). The status of each FSM nodes can be easily known at a glance of the corresponding GUI panel. The FSM state transfer was demonstrated with a CAEN simulator (Fig. 8). The FSM state transfer is tested with a CAEN simulator and is confirmed to work properly.

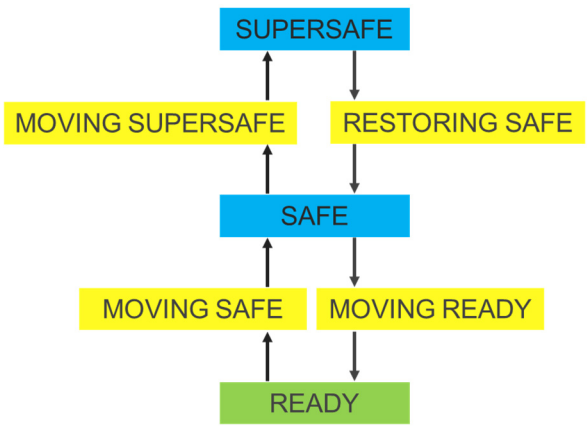

Figure 7: State diagram for the top node.

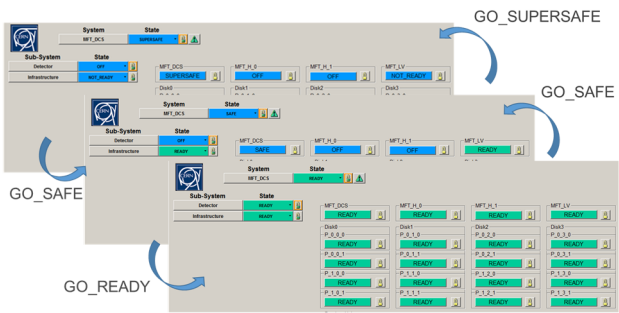

Figure 8: Simulation result of the FSM for the top node.

TEST BENCH

A test bench for implementation of the MFT DCS with the MFT hardware has been developed at Hiroshima University, Japan. The test bench has the simplest DCS chain as the one in Fig. 2.

A test to read the temperature measured with 2 Pt1000s, labelled R268 and R269, on the RU has been performed. In the data stream, a command is sent from WinCC OA to the FRED. The FRED translates the command to a sequence of hexadecimal commands to read the temperature measured with the Pt1000 sensors. Next, the sequence is delivered to the ALF and the CRU. Then, assigned ADC ports of the GBT-SCA receives the sequence and answers hexadecimal values of the temperatures to the FLP. The values are transmitted to the FRED and the FRED converts the hexadecimal values to the decimal values. WinCC OA receives the values from the FRED and displays them on the GUI (Fig. 9). Also, when the temperature exceeds the given threshold, the FSM state moves. Thus, it is confirmed that the FSM worked correctly.

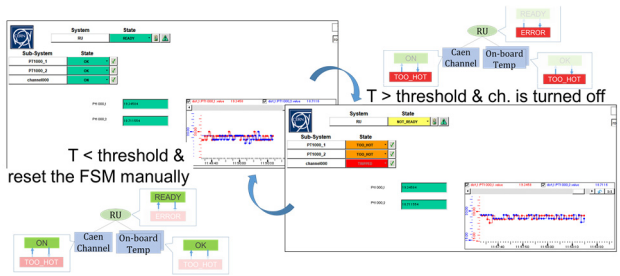

Figure 9: Result of the read the Pt1000s on the RU.

SAFETY SYSTEM

Two types of interlock systems are proposed to prevent the MFT and its electronics from damages. One is software interlock and the other is hardware interlock.

The FSM carries the responsibility of the software interlock. The software interlock is implemented for possible problems which are not serious. If the temperature exceeds a threshold of over-heating, the corresponding power supply is turned off (Table 3).

Detector Safety System (DSS) takes charge of the hardware interlock operation as a common system for all ALICE sub-detectors. The DSS is programmable by Programmable Logic Controller (PLC). The hardware interlock turns off all power supplies for the MFT if crucial problems such as failures on the cooling system occur.

As for the cooling system of the MFT, the pressure, temperature, flow rate of water and air cooling are monitored. In particular, the pressure of the water-cooling is less than atmospheric pressure to prevent from water leakage. The parameters of the cooling system are not controlled but monitored.

Table 3: Interlock States

Interlock Status	Temp. Status	Criteria
OK	Normal	$T < 30$ °C
WARNING	Hot	$30 \leq T < 50$ °C
ERROR	Too Hot	50 °C $\leq T$

CONCLUSION

The MFT is a new silicon pixel detector improves the capability of muon tracking by track matching. The MFT DCS follows the upgrade program of the ALICE central DCS.

The FSM is designed for the MFT. The simulation test has been performed, and it shows the FSM worked as designed. Also, the test to read the temperature values measured with 2 Pt1000s on the RU via the data stream including the ALFRED with the FSM has been performed. It is confirmed that the temperatures are displayed on the user interface via the DCS chain and the FSM states moves correctly. Also, hardware interlock using the DSS and the

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software interlock with the FSM are proposed and designed.

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