The Data Acquisition System for the ATLAS Phase-II Tile Calorimeter Demonstrator

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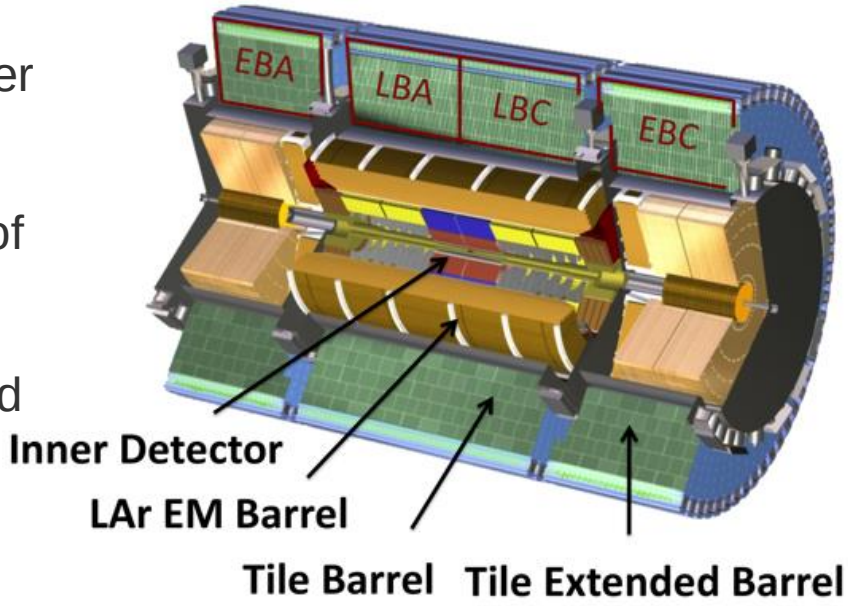
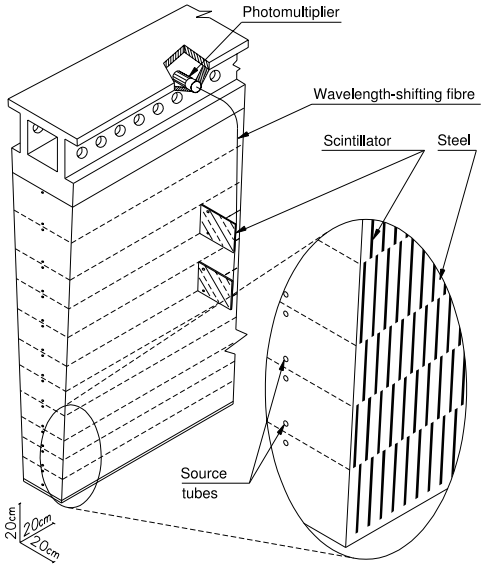
ATLAS Tile Calorimeter

- Central part of the ATLAS hadronic calorimeter (|η|<1.7)
- Contributes to the measurement of energies of hadrons, jets, τ-leptons and E_T^{miss}
- Sampling calorimeter made of steel plates and plastic scintillator tiles
  - WLS fibers and 2 PhotoMultiplier Tubes (PMTs) per cell
  - Granularity of Δη × Δφ = 0.1 × 0.1 in most cells
  - Dynamic range from ~10 MeV to ~2 TeV per calorimeter cell
- Divided in 4 partitions: EBA, LBA, LBC, EBC
  - Each partition has 64 wedges modules
    - One module hosts up to 45 PMTs
    - Electronics is located in extractable "*drawers*" at the outermost part of the module
  - 9852 PMT channels for the complete readout

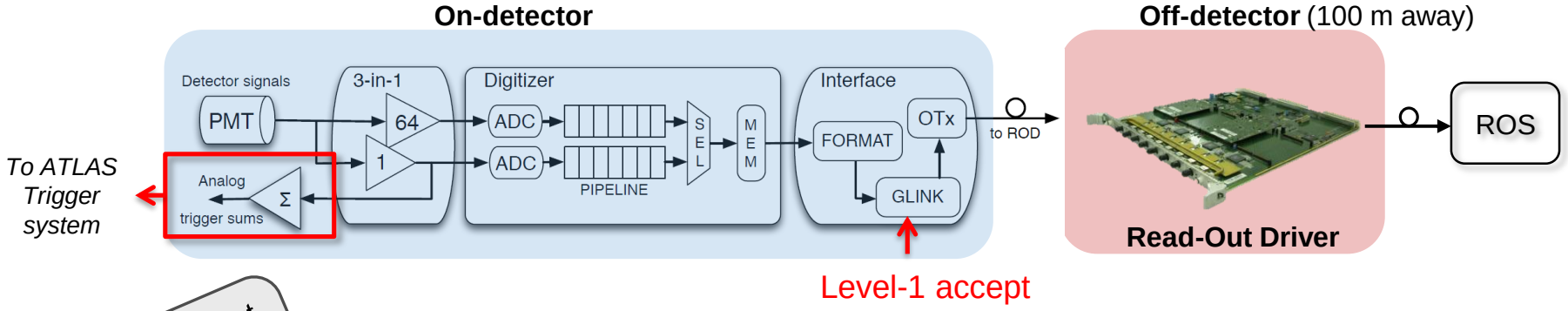




TileCal readout architecture at the HL-LHC

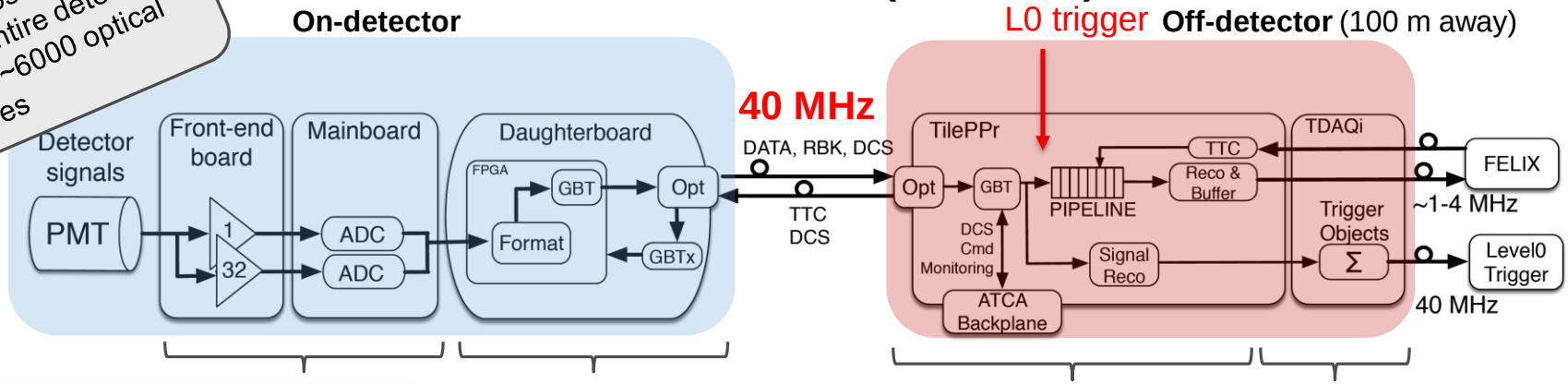
- High Luminosity LHC will achieve instantaneous luminosities a factor 5-7 larger than the LHC nominal value around 2027→ ATLAS Phase-II upgrade

Current architecture (2011-2024)



HL-LHC architecture (2027-2040)

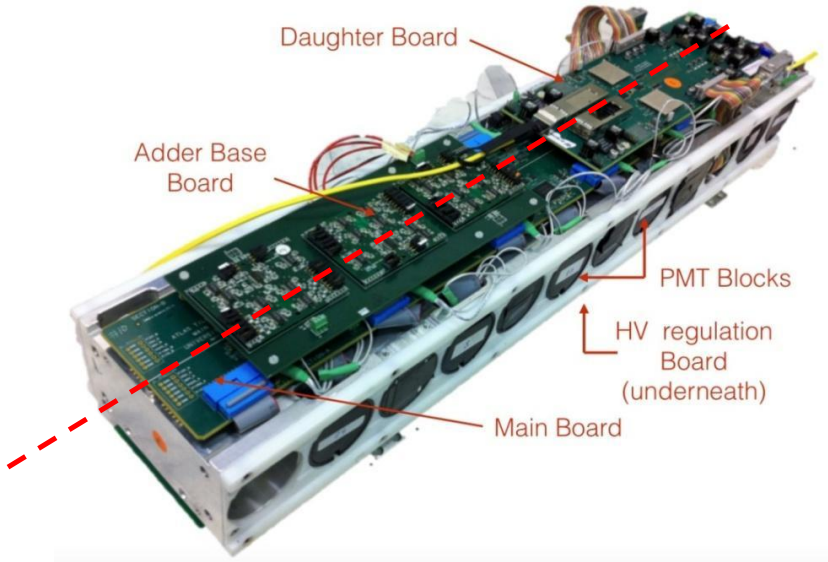
40 Tbps to read out the entire detector and ~6000 optical fibres

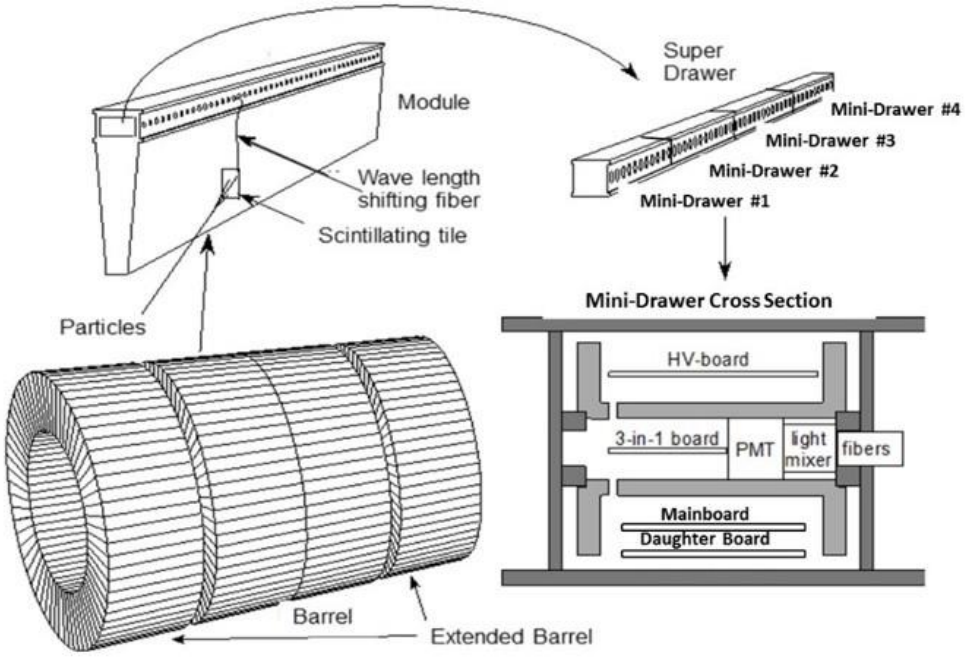


-Shaping -Amplification (2 gains) -Digitization -Calibration for electronics	- High-speed communication - Slow control and clock distribution - Data packing	- Data acquisition - Clock distribution - Pipelines buffer - Online energy & time reco	- Trigger objects computation - Interface with ATLAS TDAQ subsystems

Upgraded mechanics

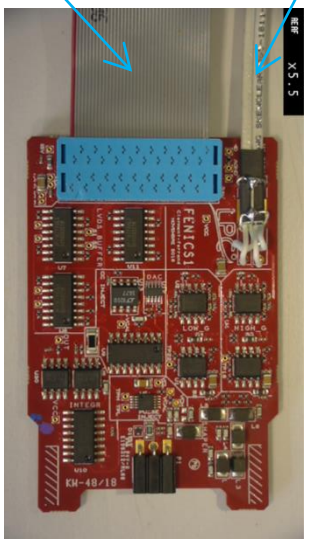
- New mechanic substructures focus on facilitate accessibility during maintenance
- Different configuration for Long and Extended Barrel modules:
  - **4 mini-drawers for Long Barrel modules → 45 PMTs : *Demonstrator module***
  - 3 mini-drawers + 2 micro-drawers for Extended Barrel modules → 32 PMTs
- Each mini-drawer has 2 independent sections for redundant cell read out
  - 12×PMTs & 12×Front-End Boards (FEBs) → read out 6 TileCal cells
  - 1×MainBoard, 1×DaughterBoard, 1×HV distribution board, 1×Low Voltage Power Supply





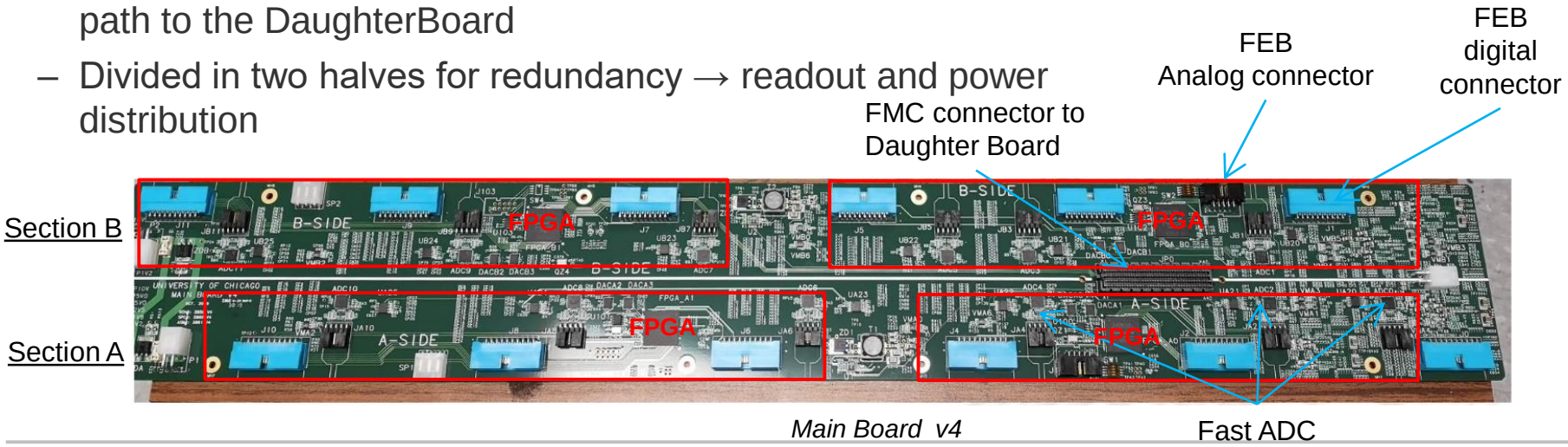
Upgraded on-detector electronics

- Front-End Boards: FENICS
  - Provides PMT pulse shaping with 2 gain amplifications
  - Integrator readout for luminosity measurements and Cs calibration
  - Built-in Charge Injection System for electronics calibration
  - Special version used for Demonstrator which provides analog trigger signals → *Upgraded 3-in-1 cards*



FENICS card

- MainBoard:
  - Digitizes signals coming from 12 FEBs
    - 12-bit dual ADCs @ 40 MSps for 2 gain signals
    - 16-bit SAR ADCs @ 50kSps for integrator readout
  - Provides digital control and configuration of FEBs + high-speed path to the DaughterBoard
  - Divided in two halves for redundancy → readout and power distribution



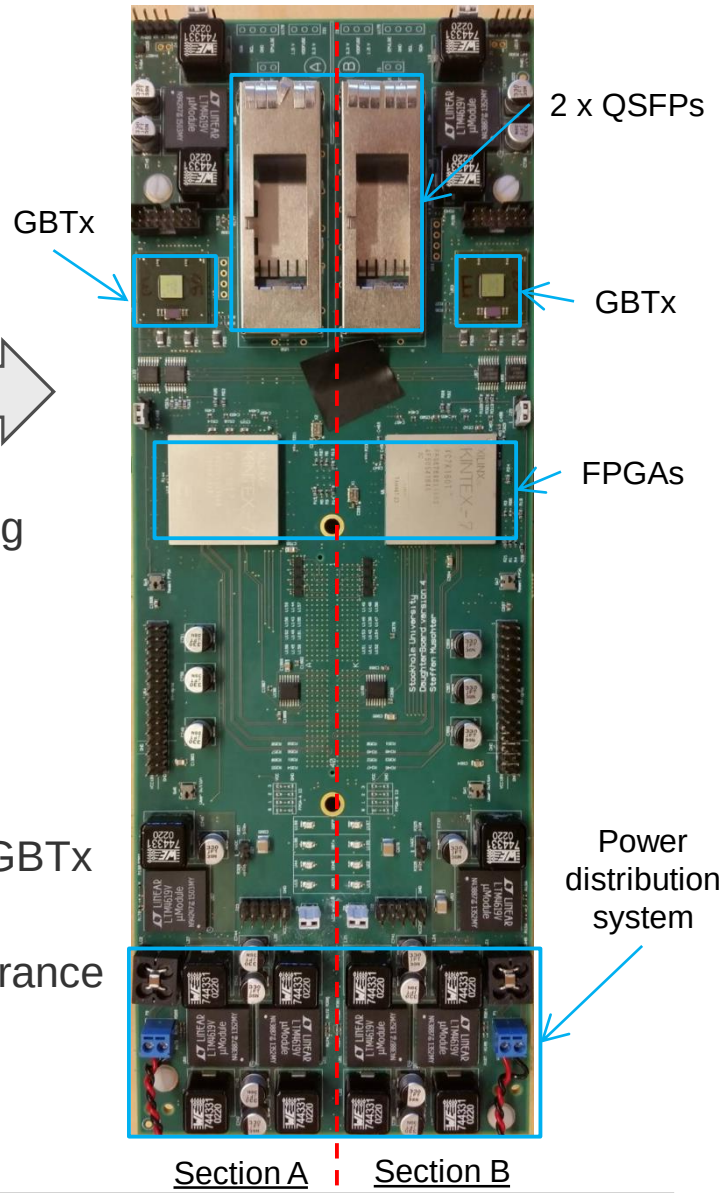
Main Board v4

Upgraded on-detector electronics (cont.)

- High-speed interface with the off-detector electronics
  - Collects PMT digitized data from Mainboards
  - Data transmission to off-detector electronics
  - Clock and command distribution to FEBs
  - Implements data link redundancy

- DaughterBoard v4 installed in Demonstrator
  - 2 × GBTx chips for LHC clock recovery and distribution
  - 2 Kintex 7 FPGAs for communication and data processing
    - Each side serving 6 PMTs
  - 2 × QSFP modules

- DB version 6 being qualified
  - Added 2 x Microsemi ProASIC3 FPGAs to interface the GBTx and FPGAs
  - Moving Kintex UltraScale FPGA family because SEL tolerance
  - Improved clocking schema for driving the high-speed transceivers

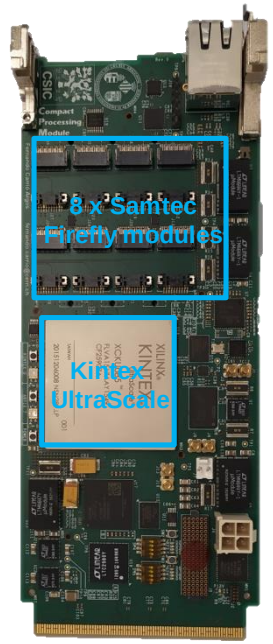


Off detector electronics: PreProcessor Demonstrator

- Off-detector readout based on FPGAs and high-speed connectors
  - Processing and data handling from on-detector electronics
  - Distribution of the LHC clock towards the on-detector electronics
  - Interface with the ATLAS readout system
- Double AMC board hosting 4 QSFPs, Virtex 7, Kintex 7 and Spartan 6
  - Capable of operating 1 upgraded TileCal module → up to 4 Mini-drawers
- Bridge between the upgraded electronics and the legacy ATLAS TDAQ system
  - Communication with the Timing, Trigger and Control system for the LHC
  - ReadOut Drivers
  - FELIX system

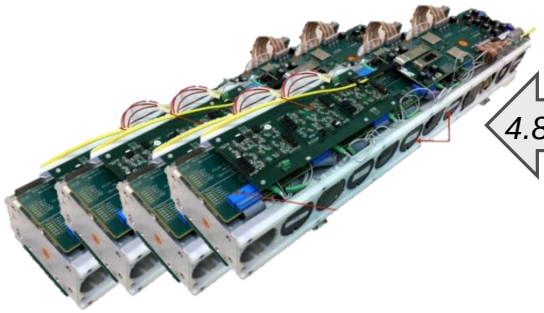
  } *Event readout*

Final version



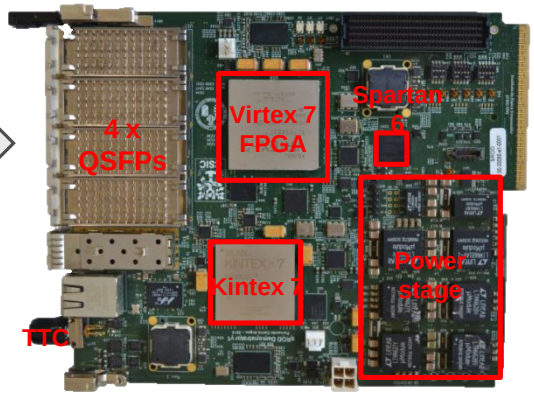
Compact Processing Module

- Next generation for HL-LHC already designed and under development



Demonstrator module (4 x Minidrawers)

4.8/9.6 Gbps



PPr Demonstrator

800 Mbps

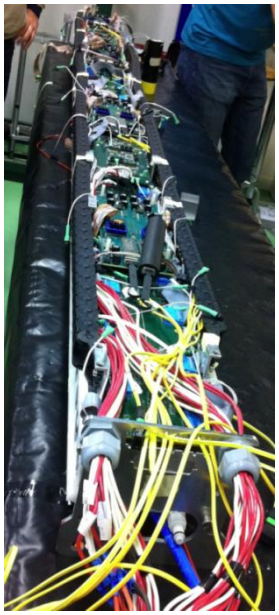
Legacy ROD

4.8 Gbps

FELIX emulator

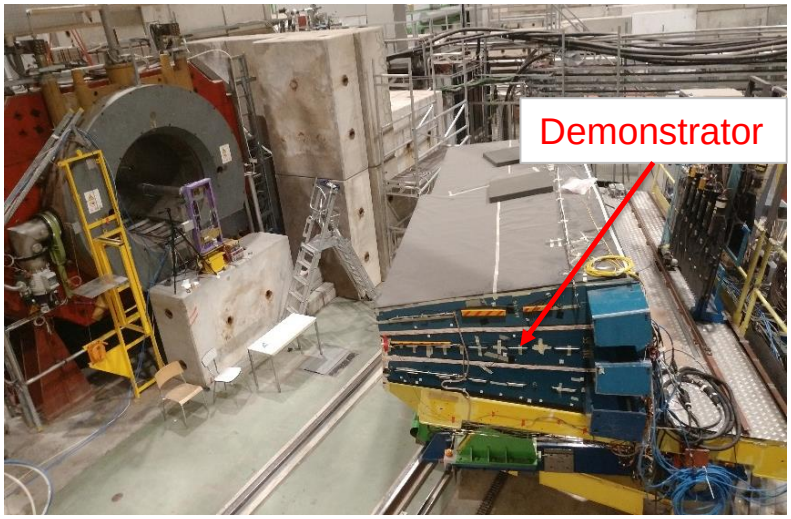
Demonstrator construction and test beams

- Constructed a Long Barrel module in 2015
  - 4 mini-drawers populated with the latest versions of the upgraded readout electronics & mechanics
- Seven test beam campaigns between 2015 and 2018 at SPS accelerator
  - Detector modules equipped with upgraded and legacy electronics for performance comparison
  - Beams of Hadrons, Electrons and Muons were used to study the calorimeter response and S/N performance of the new electronics

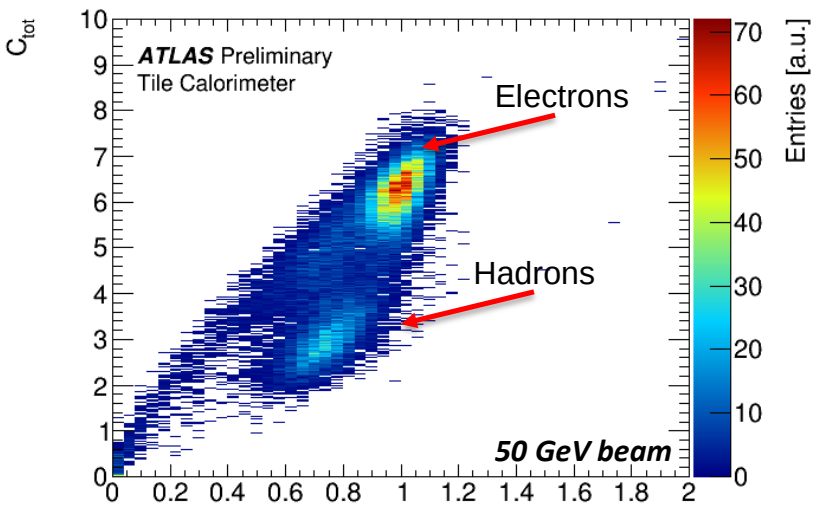


First Demonstrator

Assembly of the Demonstrator



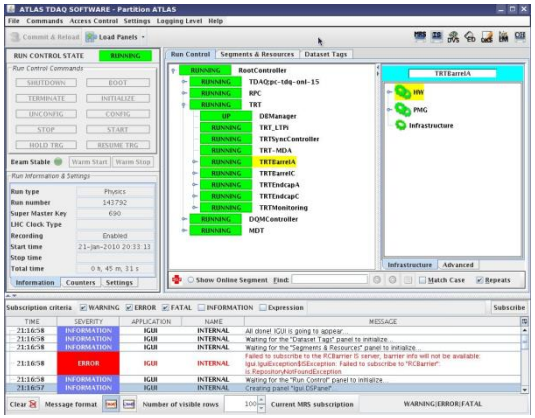
Test beam setup at SPS



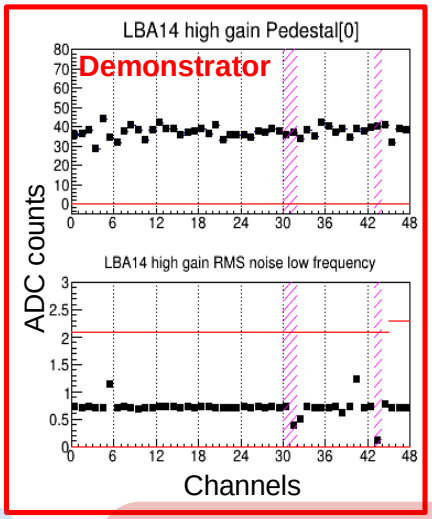
Scatter plot of C_tot vs C_long

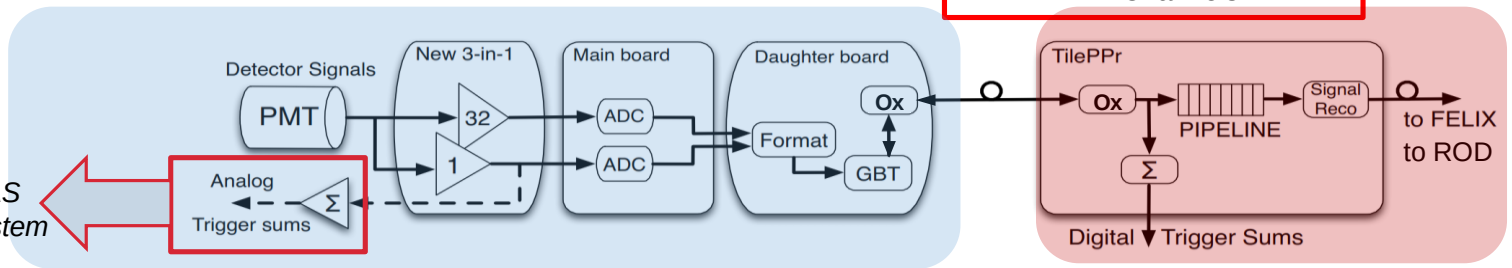
Insertion in ATLAS experiment

- Demonstrator module inserted in ATLAS July 2019
  - Exercised during the LHC Long Shutdown 2 (2019-2021)
- Operating with backward compatibility with the current ATLAS DAQ system
  - Receiving clock and configuration commands from legacy TTC
  - Transmitting event data to ATLAS DAQ as other Tile module
  - Providing analog cell sums to the ATLAS trigger system
- Fully integrated with the TDAQ software
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - Event builder and offline reconstruction
- Good and stable performance with lower noise levels than the legacy Tile modules



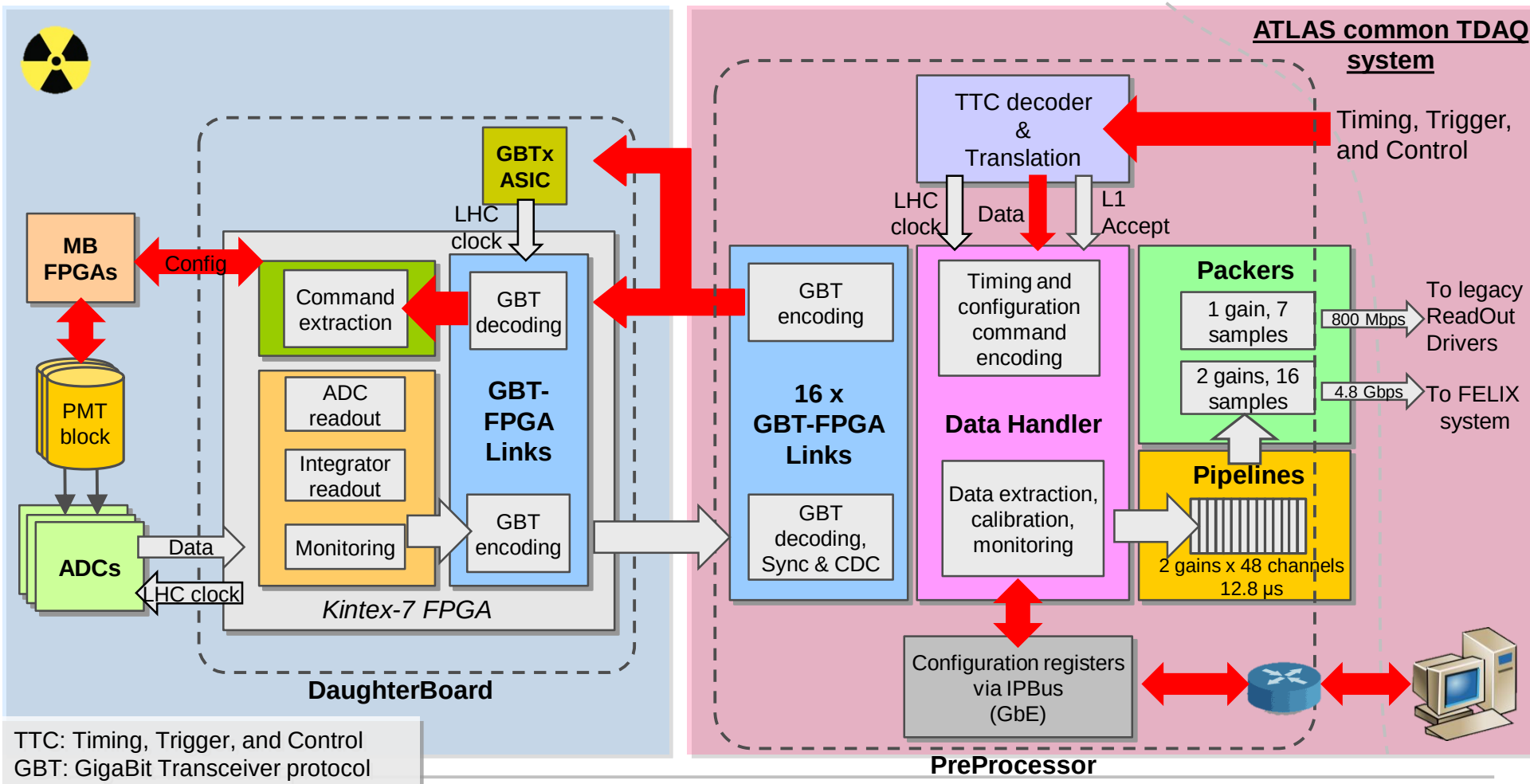
ATLAS TDAQ software





DAQ implementation: Front-end configuration

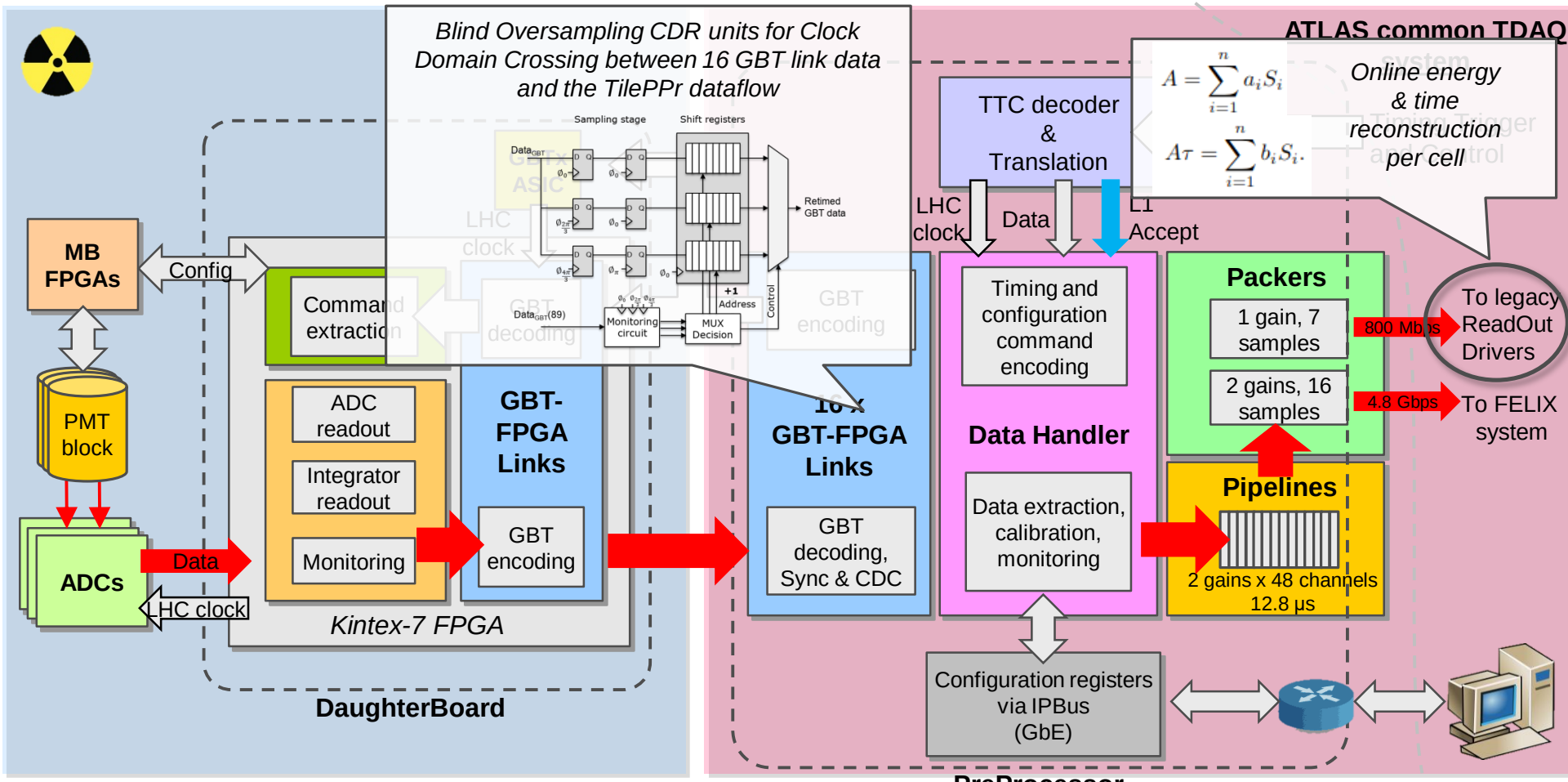
- FE configuration received from the TTC system (fibre) and from ATLAS software (GbE)
- TilePPr translates the TTC commands into “upgraded” configuration commands
- Configuration is decoded in the DaughterBoards and propagated to the rest of the electronics
  - Three GBT links at 4.8 Gbps with FEC → configured for fixed and deterministic latency



TTC: Timing, Trigger, and Control
GBT: GigaBit Transceiver protocol
FEC: Forward Error Correction

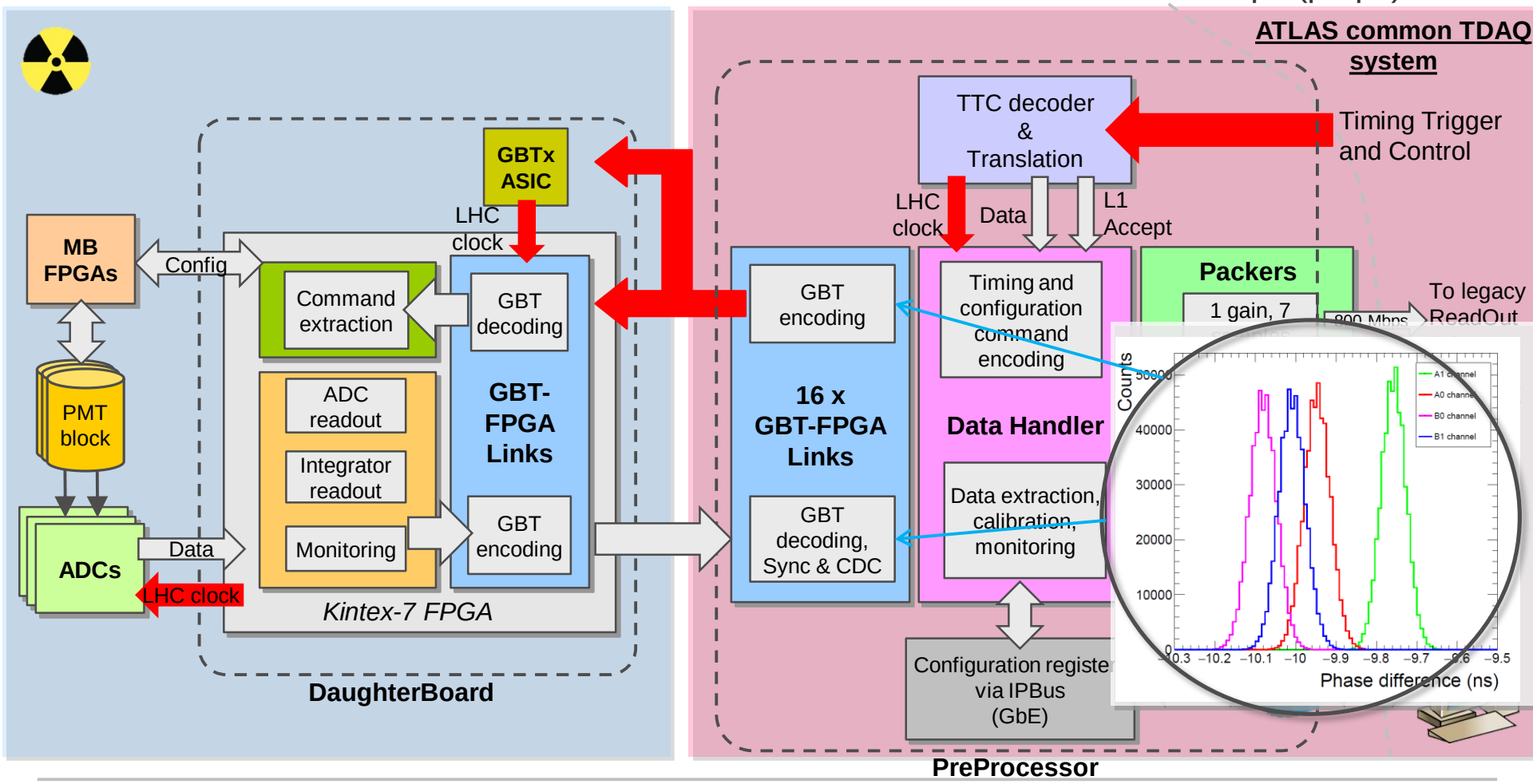
DAQ implementation: Front-end readout

- On-detector transmits digitized data for every bunch crossing (40 MHz)
- Data received through 4 GBT links@9.6 Gpbs per DaughterBoard → ~154 Gbps in total
  - Data is processed, tagged with a Bunch Crossing Identifier and stored in pipeline memories
- Selected events are transmitted to legacy RODs and FELIX after a Level-1 trigger is received



DAQ implementation: clock distribution

- Clock is recovered from TTC system and jitter cleaned on-board (Texas Ins. CDCE62005)
- Clock transmitted embedded with data through one GBT links@4.8 Gpbs
  - GBT-FPGA(PPr) → GBTx ASICs → ADCs for data sampling
- Phase variations between distributed and received LHC clock are below 100 ps (pk-pk)



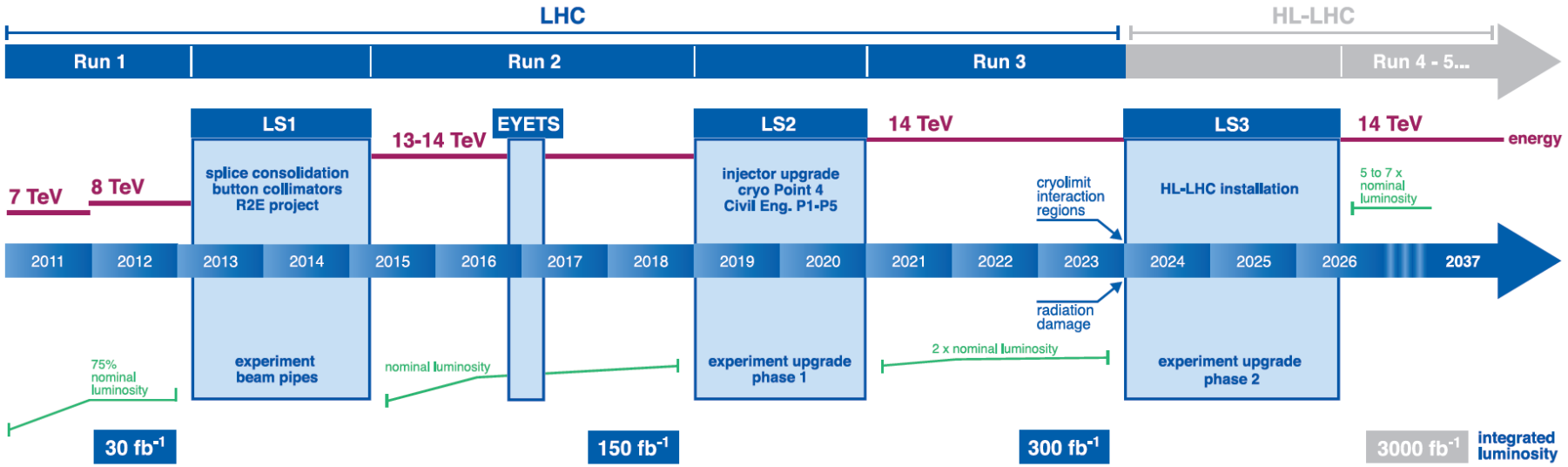
Summary

- New conditions imposed by HL-LHC requires the complete redesign of the TileCal on-detector and off-detector electronics with a new clock and data readout architecture
- Construction of a Demonstrator “hybrid” module
  - Latest versions of the on-detector electronics for the HL-LHC
  - Fully operational PreProcessor Demonstrator prototype
- Demo readout electronics implements the clock and data architecture for HL-LHC
  - Continuous sampling and transmission of data at 40 MHz to off-detector using link redundancy
  - Clock distributed via a combination of high-speed links with fixed and deterministic latency and GBTx ASICs in the on-detector
- Extensively exercised during seven test beam campaigns (2015-2018)
- Insertion of the Demonstrator module in ATLAS during Summer of 2019
  - Fully integrated in the current ATLAS DAQ system
  - Mimicking the behavior of legacy TileCal modules
- Aiming to keep the Demonstrator module inserted in ATLAS for Run-3 (2022-2024)

THANKS FOR YOUR ATTENTION

BACKUP SLIDES

High Luminosity-LHC & Tile Calorimeter



- LHC plans to increase the instantaneous luminosity by a factor 5-7 around 2027→ **High Luminosity-LHC**
  - Expected number of collision per bunch crossing will increase up to 200
  - New Trigger and Data AcQuisition architecture with full granularity and digital inputs
- TileCal: Major replacement of on-detector and off-detector readout electronics
  - Aging of electronics due to time and radiation
  - Current readout system will not be compatible with the upgraded TDAQ architecture
  - Other detector elements as scintillators or PMTs will be kept

GigaBit Transceiver Protocol

- Data protocol between the DaughterBoards and the TilePPr
- Developed by CERN for data communcation in radiation enviroments
  - GBTx, LpGBT, GBT-SCA chips
- Main features
  - 120 bit words @40 MHz → **4.8 Gbps**
  - Forward Error Correction capabilities
    - Reed Solomon encoding → up to 16 consecutive error bits

Frame	Wide-Bus
3.2 Gbps	4.48 Gbps

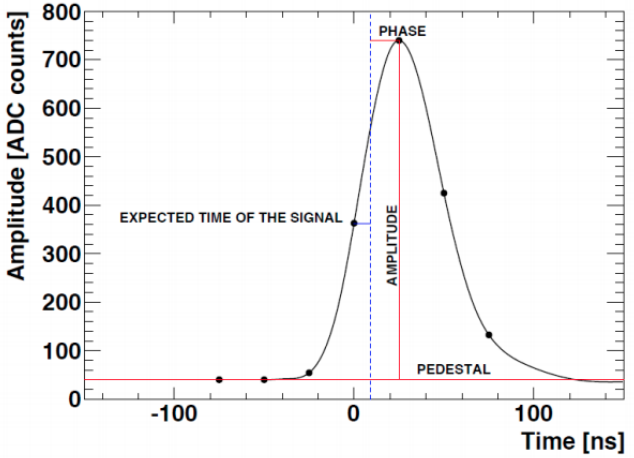
- Two possible implementations in FPGA:
  - **Standard:** easy implementation, but no fixed and determinitisc latency
  - **Latency Optimized (LO):** fixed and deterministic latency at the cost of a complex implementation

119 0

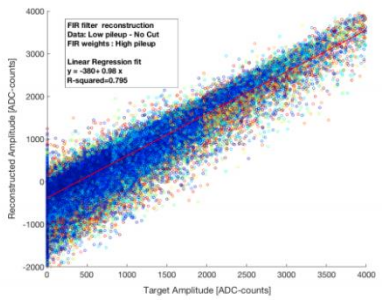
4 bits	4 bits	80 bits	32 bits
Header	Slow Control	Data	FEC

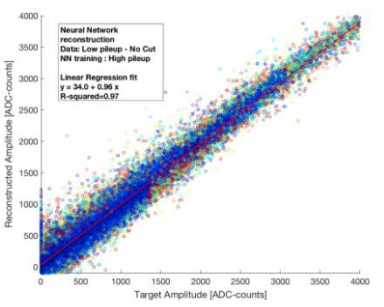
Energy Reconstruction

- Extra pile-up noise in harsh conditions with μ = 200 in HL-LHC
  - Signal alterations
- Energy reconstruction implemented in FPGA
  - Current: Optimal filtering (FIR filter)
  - Deep Learning MLP with 1 hidden layer
    - Excellent precision under mu = 80
    - More advanced studies ongoing
      - 12-bit weights
- Resources per channel
  - Latency 5 CLK cycles
  - Fullfil requirements



Resource summary	Available	Utilization		
		ANN	OF-FPGA	OF-DSP
Slice registers	607,200	695	98	-
Slice LUTs	303,600	1297	87	-
RAM blocks	1,030	4	0	-
DSPs	2,800	13	3	-
Performance summary				
Operation mode		Parallel (pipelined)	Parallel (pipelined)	Sequential
Latency	-	125 ns	25 ns	10 μs
Operation frequency	-	40 MHz	40 MHz	100 KHz

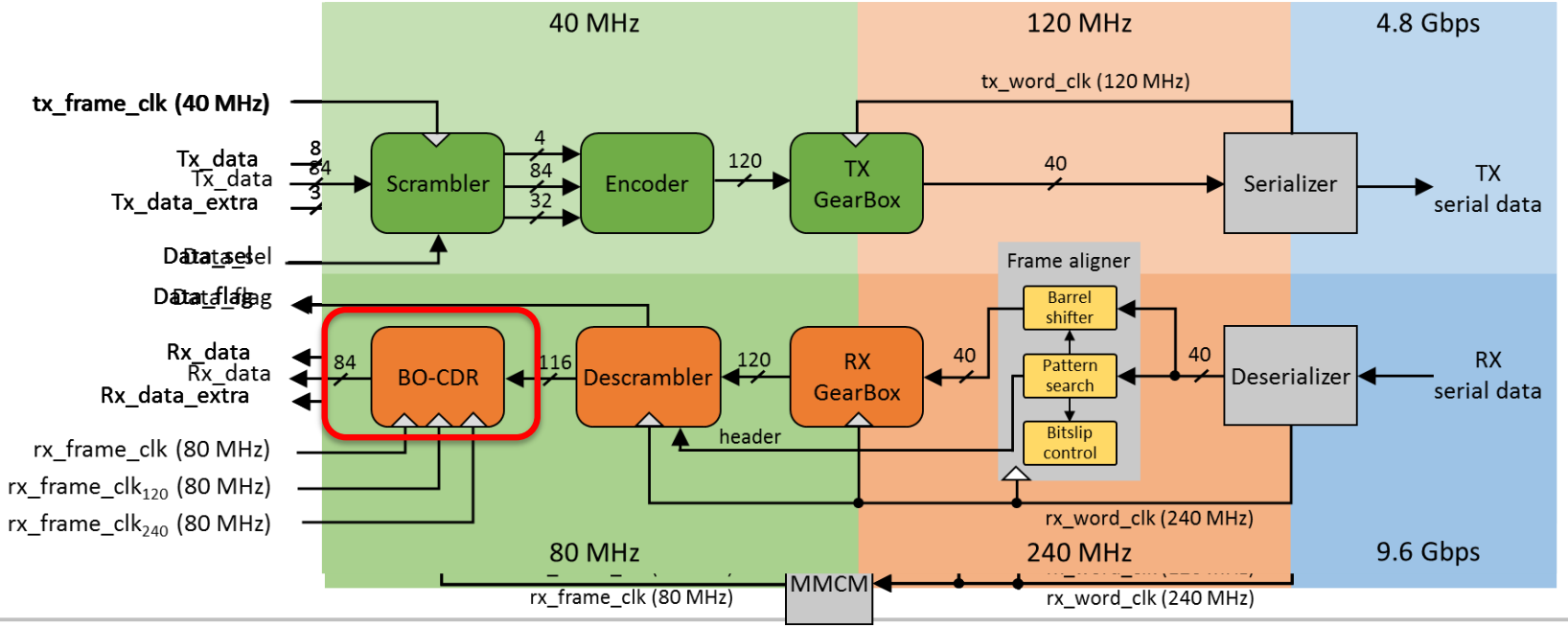




Tile GBT implementation

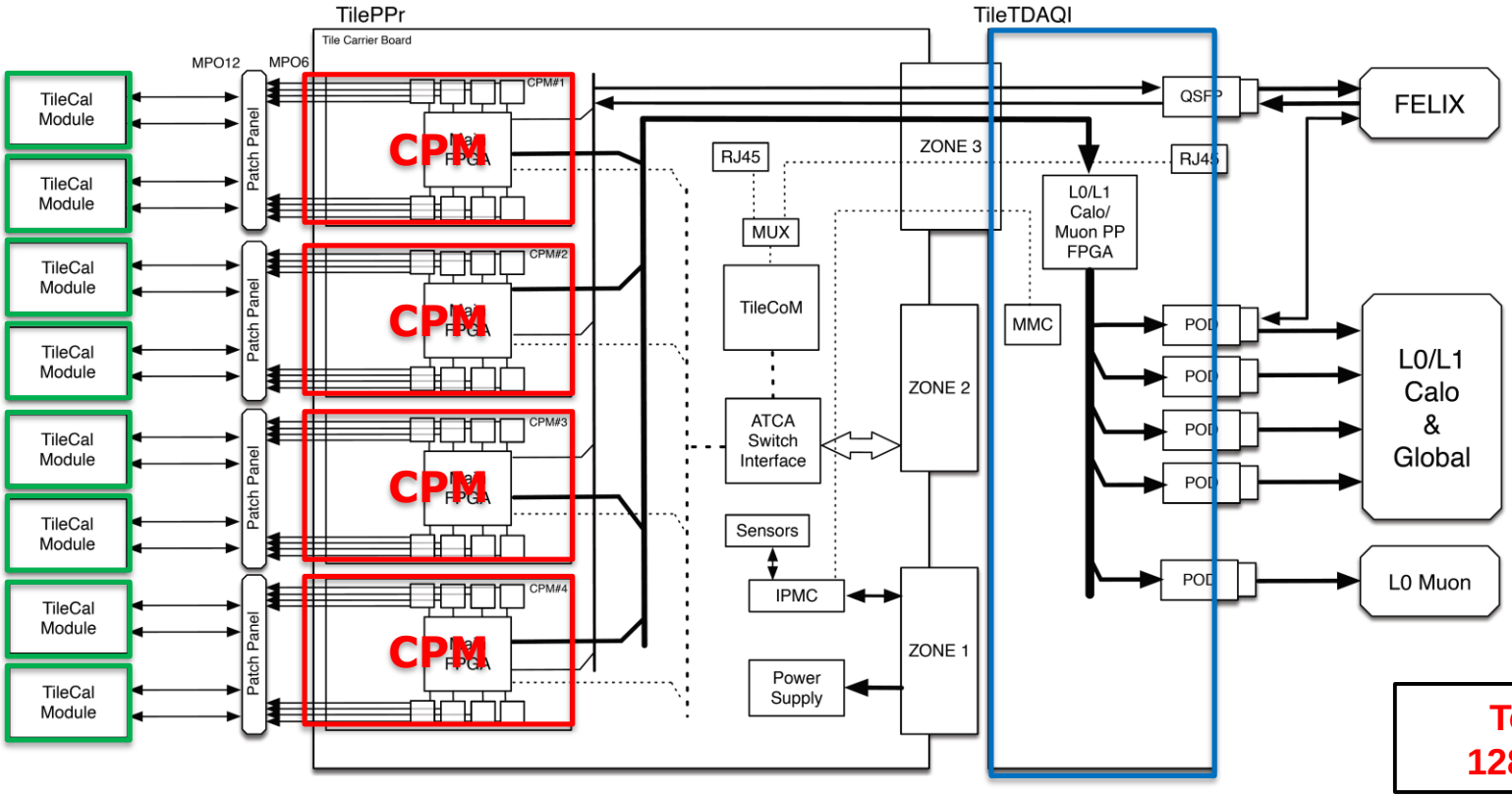
- Implementation of 16 LO GBT links in the TilePPr
  - Downlink: GBT code with minor modifications
    not enough bandwidth → **5.76 Gbps only for the PMT samples!**
  - Uplink: not enough clock resources
    time stamp the data → RX and TX clocks are not in phase

- Two important modifications on the original GBT code
  - Data rate increased by factor two: from 4.8 Gbps to 9.6 Gbps
  - BO-CDR → optimization of clocking resources and data retiming



Phase II off-detector electronics

- **The Tile PreProcessor is the core element of the off-detector electronics**
  - Data processing and handling from on-detector electronics
  - Provides clocks and configuration for the TileCal modules
  - Interface with the ATLAS trigger and readout systems (FELIX)



Total of 128 CPMs

- **32 TilePPr** boards in 4 ATCA shelves**:** ATCA carrier + **4 Compact Processing Modules**
- **32 TileTDAQ-I:** Interfaces with L0Calo, Global, L0Muon and FELIX system

Compact Processing Module - Overview

- **Single AMC board** with full-size form factor
  - **32 channels** through **8 Samtec Firefly modules** → Up to **400 Gbps** via optics
  - **14 channels** through AMC connector → Up to **175 Gbps** via electrical backplane
  - **Kintex KU085 for proto(v1), KU115 for final design**
- High bandwidth readout system