Testing of the Micromegas detector trigger electronics for the New Small Wheel Phase I upgrade of ATLAS detector

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Stamatios Tzanos [1,2] on behalf of ATLAS Muon Collaboration

1. National Technical University of Athens 2. Brookhaven National Laboratory

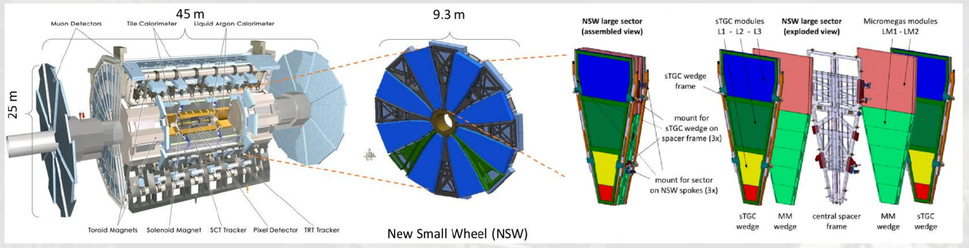
Abstract

In conjunction with the High Luminosity upgrade of the LHC, the ATLAS detector is also undergoing an upgrade to handle the significantly higher data rates. The muon end-cap system upgrade in ATLAS, will replace the Small Wheel which is the innermost muon detection section of the endcap. The New Small Wheel (NSW) is expected to combine tracking and triggering information for the Level-1 trigger. To accomplish this, small Thin Gap Chamber (sTGC) and MicroMegas (MicroMesh Gaseous Structure) detector technologies are being deployed.

The Micromegas detector technology is equipped with three types of electronic boards to provide the triggering and tracking information. These boards are the Micromegas Front End with 8 VMM chips (MMFE8), the Level 1 Data Driver Card (L1DDC) and the ART Data Driver Card (ADDC). The Address in Real Time (ART) signals produced by the VMMs are propagated through the ADDC and sent to the Micromegas Trigger Processor for the decision of the Level 1 Accept (L1A) trigger signal.

In order to test the functionality and efficiency of the trigger electronics, various tests are being conducted at the dedicated integration site at CERN. During the "Micromegas ART connectivity test", testing pulses generated internally on the VMMs are sent through the trigger electronics to simulate ART hits from the MMFE8s to the Trigger Processor. This test is performed to validate every New Small Wheel Micromegas double wedge and is essential to identify ADDC boards or fibers that must be replaced, tested or repaired. MMFE8 and L1DDC issues can also be identified. Finally, the trigger processor's data acquisition, firmware and trigger logic are being tested with cosmics data. In this poster, the various tests and results from cosmics data are presented.

New Small Wheel of ATLAS detector

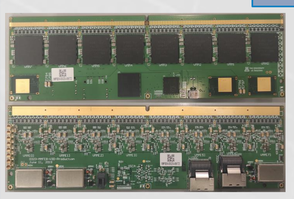


HL-LHC is expected to reach luminosity levels of $7.5 \times 10^{34}\ \mathbf{cm^{-2}s^{-1}}$. Thus, NSW specifications are expected to include:

- Angular coverage of $1.3 < |\eta| < 2.7$
- Angular resolution of **1 mrad** at the Level-1 Trigger
- Track reconstruction resolution of **50 μm**
- Track reconstruction **efficiency** ≥ **97**% for energies over 10 GeV

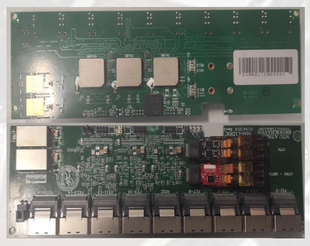
NSW is expected to replace the Small Wheel in ATLAS during 2021.

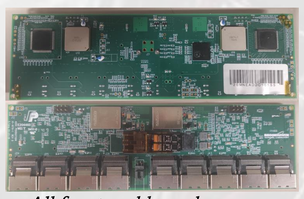
Front End Electronics



The **MMFE8** 64-channel **VMM** ASICs, the Read-Out Controller (**ROC**) and the Slow Control Adapter (**SCA**). Each VMM channel is connected to a detector read-out strip and transmits the signal received to the L1DDC through the ROC. At the same time, the **ART** data is transmitted (which is the fastest 'OR' of the 64-channels) to the ADDC for the trigger decision.

The **L1DDC** consists of 3 GigaBit Trasceivers (**GBTx**) ASICs capable of receiving front-end data from 8 MMFE8s. The L1DDC forwards the data through an optical link with a speed of 4.8 Gbps. Communication with the front-ends is achieved with differential pairs combined in groups called e-links. The L1DDC's purpose is to configure the MMFE8s, ADDCs, receive L1 data (time, charge, strip address), forward it to the network interface (FELIX).

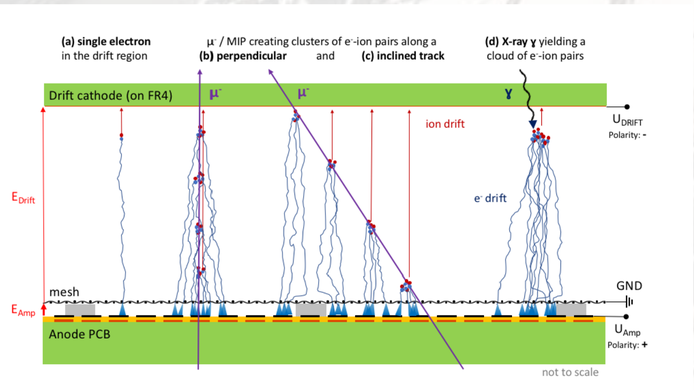




The **ADDC** consists of two GBTx that receive ART data from 8 MMFE8s (1 GBTx per 4 MMFE8s). The ART Data is then sent through optical links to the Trigger Processor (**TP**) for the trigger decision.

*All front end boards are powered by the Low Voltage Distribution Board (**LVDB**). For NSW, all chips on every front end board is custom-designed to be radiation tolerant. Each Micromegas double wedge is equipped 128 MMFE8s, 16 ADDCs, 16 L1DDCs and 16 LVDBs.*

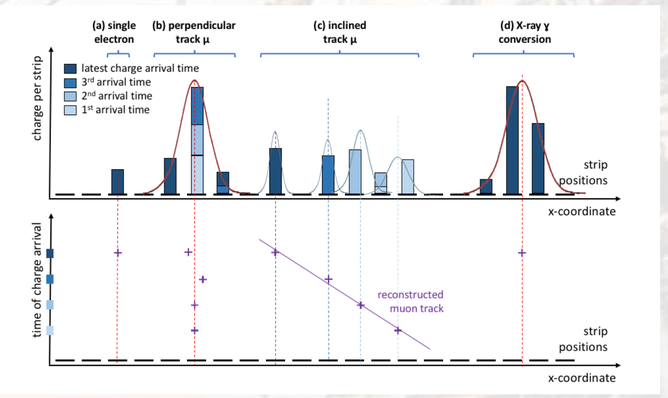
The Micromegas detector



- Micromegas is a gaseous detector divided into two regions, *drift* and *amplification*.
- Muons pass through the detector ionizing the gas
- Ionized electrons drift through a micromesh into the amplification region
- The signal induced through the avalanche is read out by the electronics attached on the strips

- Ability to reconstruct the **time** of the electron cluster
- Known **x-coordinate** of the readout strip where signal was induced
- Electron **drift velocity** from simulation
- Reconstruction techniques used: **charge centroid**, **μTPC**

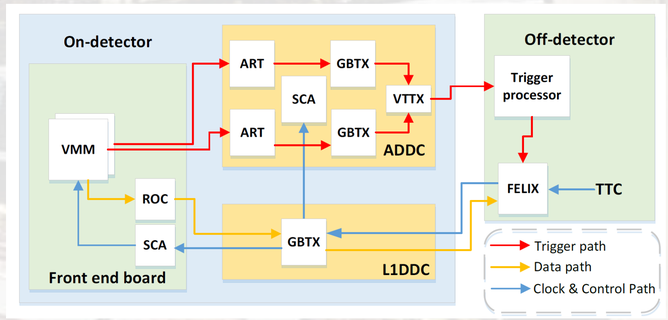
*2 × 4-layer detectors with this design compose a **Micromegas Double Wedge***

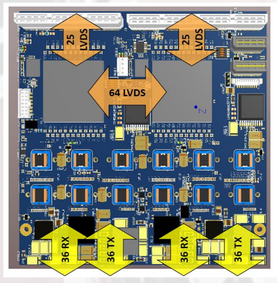


The Triggering scheme

Inside the trigger path:

- ADDC **deserializes the ART stream** from the VMMs and phase-aligns the hits to the bunch crossing (BC) clock provided through the L1DDC
- Identifies which **strip is hit** from a 6-bit geographical VMM ASIC address
- Sends the **ART data** and **BCID** (time) of the hit to the trigger processor
- Off-detector, the TP makes a **trigger decision** based on the strips that had a hit





Trigger Processor hardware platform High Density Optical Mezzanine (**HORX**):

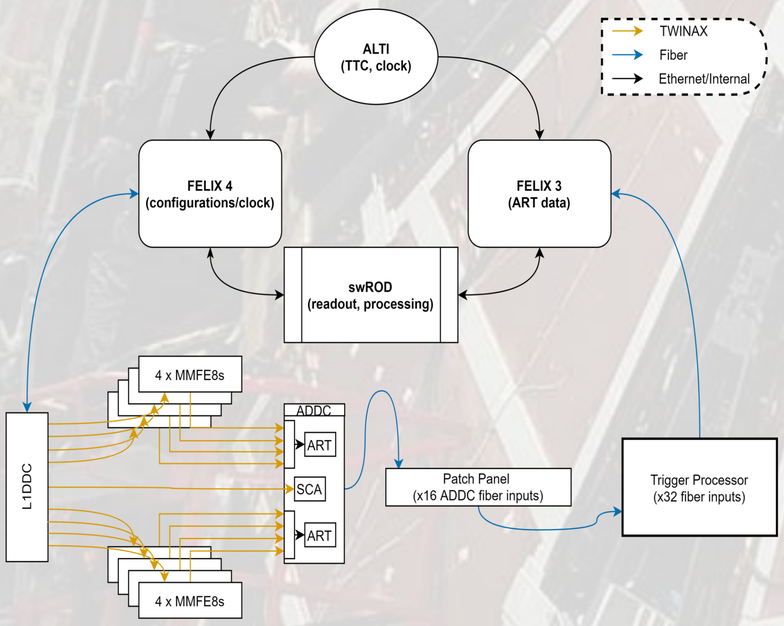
- ❑ **ATCA mezzanine** with NSW specifications
- ❑ 2 × Virtex7 690 **FPGAs**
- ❑ **36 Optical Transceivers** per FPGA

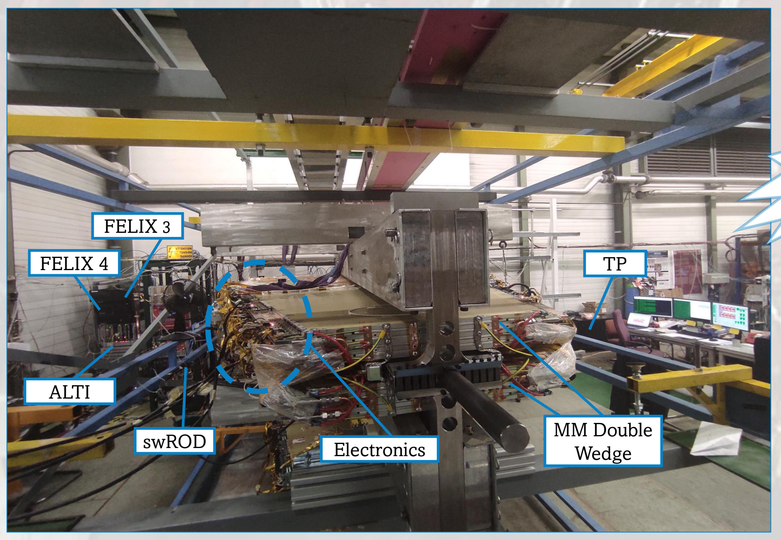
The trigger processor will:

I. Receive ART data with optical links from the front ends
II. Look for track coincidence using the trigger algorithm
III. Send L1A signal to FELIX/Trigger Logic

Testing of the electronics

Testing setup for the electronics at Building 899 (BB5)

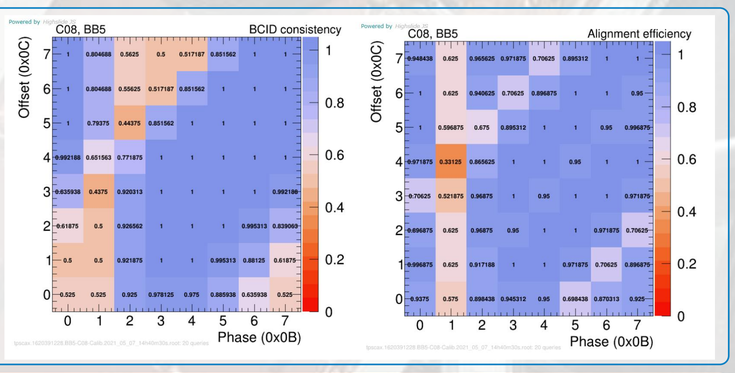


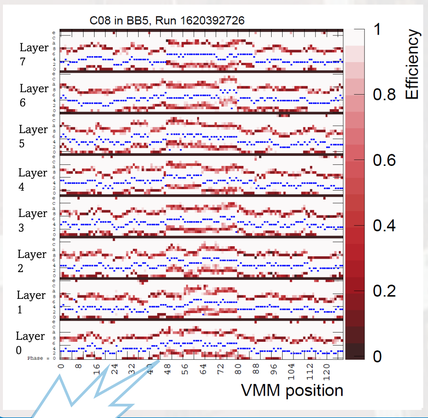


Picture of BB5's cosmic stand with all components shown. Patch panels for L1DDCs and ADDC lay behind the detector

Trigger Processor Input Phase:

- ❖ ADDCs from different positions have **different fiber lengths**
- ❖ Align the fibers using two 40 MHz stages, phase locked with the BC clock
  - First stage of alignment is to delay the short fibers and latch the data within an aligned window
  - Second stage provides alignment and fixed latency
- ❖ Plot on the right gives us a map of all phases and offsets.
- ❖ Select the best pair of (Phase, Offset) for the best **BCID Consistency and Alignment Efficiency**



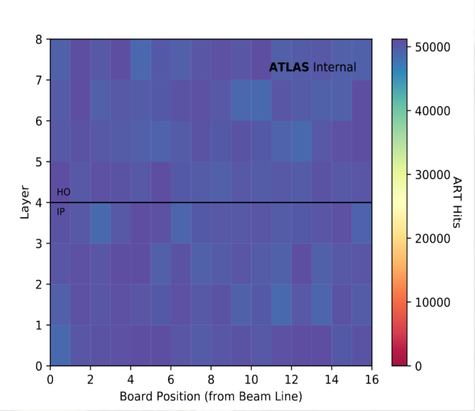


ART Input Phase Calibration:

- ❖ Aligning the **ART clock** with the VMM **ART Phase**
- ❖ Use **delays** of the ART signal on VMM to find an efficient phase

$$eff = \frac{hits\ observed\ with\ expected\ channel}{hits\ observed}$$

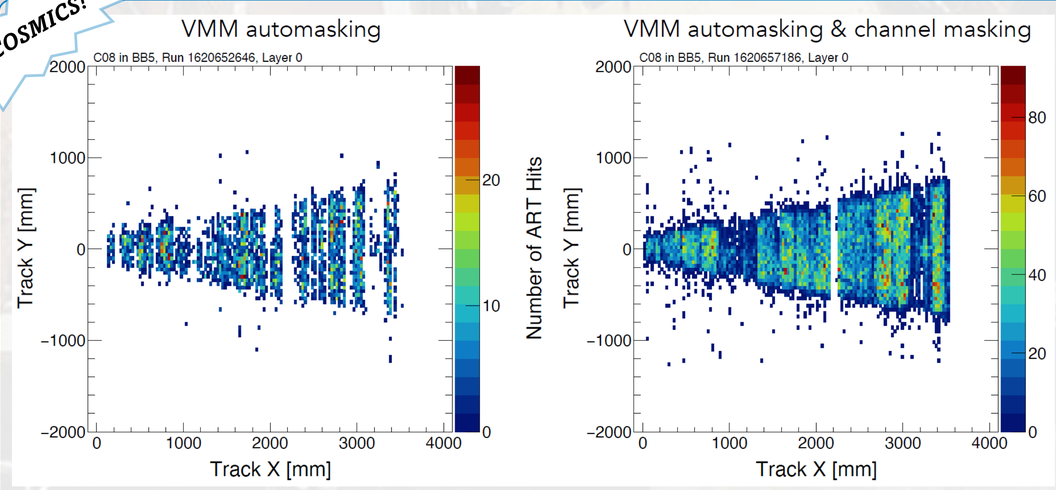
- ❖ Choose the phase in the **middle of the first plateau** of efficient phases
- ❖ Repeat for all VMMs of all Layers



ART Connectivity Test:

- ❖ Using the VMM **Internal Pulser**, produce 100 artificial ART hits per VMM channel
- ❖ Total: $100 \times 8\ (VMM) \times 64\ (ch) = 51200$ ART hits **per MMFE8**
- ❖ Propagate the signals through the trigger scheme
- ❖ **Create an L1A** that matches the ART Timing
- ❖ Readout the ART hits through FELIX
- ❖ Repeat for all MMFE8s of all Layers

COSMICS!



Cosmics data after testing the electronics:

- ➢ Enable the MMFE8s ROC e-links to receive real ART Data
- ➢ Program the TP with a firmware that uses the Trigger Algorithm to self-generate L1As
- ➢ Use the detector geometry to visualize ART Hits

Feedback with cosmic data is crucial to our engineer for debugging and optimization of the TP

Noise Tackling:

- ➢ Noisy VMMs can be masked by the TP
- ➢ Channel masking cannot be implemented by the TP
- ➢ Channel masking at the VMM directly, significantly improves data acquisition (right plot)
- ➢ Efforts to recognize noisy channels before attempting cosmics

Ongoing commissioning effort to test new TP firmwares, noise tackling techniques, data acquisition and analysis techniques.