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RD Collaboration Proposal: Extension of RD53 for 3 years to finalize pixel chips for the ATLAS and CMS pixel detector upgrades

RD53 collaboration

ABSTRACT: The RD53 collaboration was established in 2013 to develop next generation radiation hard pixel readout chips for the High Luminosity LHC detector upgrades. It has been agreed with the ATLAS and CMS experiments that RD53 will deliver final production version chips to the two experiments. Final pixel chips will be optimized for each experiment, having minor differences: chip size and analogue front-end, but will otherwise have identical functions and be based on a common design and verification framework developed in RD53. Full sized pixel chip prototypes have recently been made for each experiment. The ATLAS chip is currently under exhaustive testing at chip, module and system level. The CMS chip is in final sign-off verification and prototyping in the 65nm foundry. This proposal is to extend the RD53 collaboration for further 3 years to submit final production version chips during 2022 and assure required exhaustive testing and radiation qualification and necessary support to the experiments for their final integration into the pixel detectors of both experiments during 2023-2024. The current status of RD53 pixel chips are shortly summarized and a proposed work plan to make final chips are outlined.

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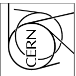

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1. Introduction and summary of current status

The RD53 Collaboration was established in 2013 to develop next generation of pixel readout chips for the High Luminosity LHC detector upgrades [1]. The collaboration has been fully focused on building the technology and design foundation needed to produce large format pixel readout chips for the challenging requirements from the two experiments. The first years R&D were dedicated to radiation tolerance studies of the chosen technology to determine how sufficiently radiation hard circuits can be implemented in the chosen 65nm CMOS technology. Critical building blocks (DAC, ADC, Analogue front-end, Serial power regulator, PLL, high speed serializer, cable driver, Bandgaps, etc.) were developed, prototyped and tested for functional performance and radiation tolerance to the 1Grad level. An appropriate digital readout architecture was developed and simulated to cope with the high hit rates of 3-4GHz/cm^2, extended trigger latency of 12.8us, trigger rates of 1MHz and the required readout bandwidth of 5Gbits/s per chip. A half sized (to allow mask sharing with other HEP chips) fully functional pixel readout chip, RD53A, was designed and submitted in 2017. The RD53A contained all necessary building blocks and 3 different analogue front-ends to enable their extended testing and qualification in a large complex mixed signal pixel chip. 100 wafers of the RD53A chip have successfully been produced for the two experiments and have been the foundation for testing and qualification of the developed pixel chip, 50 μmx50 μm and 25 μmx100 μm pixel sensors and also pixel modules and pixel detector system based on the novel serial powering concept, critical for low mass power distribution.

Following the successful development, and extensive use of the RD53A demonstrator chip, ATLAS and CMS have formally mandated the RD53 Collaboration to design final pixel chips for their phase 2 pixel upgrades. It was proposed to develop a common chip for use in the two experiments. Different geometric layout constrains and different emphasis on specific performance of the analogue front-end implied that the experiments requested to get pixel chips optimized for their particular use. Two slightly different full sized pixel chips have been been developed and submitted. The RD53B-ATLAS chip was submitted in March 2020 and the RD53B-CMS chip is

in final sign-off check and prototype production in the foundry (expected delivery end August). The two chips are based on a common design and verification framework developed in RD53, based on experience from the RD53A demonstrator chip.

The RD53B-ATLAS chip has been under extensive testing and qualification within the RD53 and ATLAS (and CMS) pixel detector communities during the last 9 months. An unfortunate design bug in a custom high density 4 bit TOT latch implied that a re-spin of the design, with two minor mask changes, has been required to get chips working with acceptable power consumption in binary pixel hit detection mode. The lack of TOT charge measurement per pixel in this chip is being alleviated by using a high precision timing and TOT feature in the chip, at low hit rates, to perform detailed characterization of the analogue front-end and use it for detailed pixel sensor and pixel module testing and characterization. Otherwise the chip is fully functional with a much improved on-chip serial power regulator and many new configurable features made for flexible use in final pixel detectors. A RD53B-ATLAS chip testing community has been organized with weekly meetings where test results are presented and discussed among chip designers and pixel detector experts from RD53, ATLAS and CMS pixel detectors. A few minor bugs have been identified, that have been corrected in the RD53B-CMS chip submission. Extensive TID and SEU tests have a been made at different radiation facilities (CERN, Louvain-la-Neuve, GANIL, TRIUMF, Oxford). TID tolerance have been confirmed up to 1Grad at high dose rate and low dose rate tests have been made to evaluate the magnitude of low dose rate effects (500Mrad OK, 1Grad to be verified with extended low dose rate TID testing). SEU and SET testing with heavy ions and protons have been made to confirm acceptable behaviour in its extremely hostile radiation environment (up to 100 memory elements per chip will be corrupted each second from radiation induced SEUs). Efficient SEU protection has been confirmed using Triple Modular Redundancy (TMR) in critical parts of the design. Hit storage in latency buffer and readout buffers are not SEU protected, as can simply not fit in the extremely dense digital logic required to handle the high hit rates and long trigger latency. Needed incremental improvements for Control and readout links have been identified.

The RD53B-CMS chip is in final design verification and sign-off for submission before end of May and 20 wafers are expected to be delivered end of August. The CMS specific analogue front-end have been integrated, identified bugs in the RD53B-ATLAS chip corrected, and a set of minor optional additional features have been added (BX-ID, L0ID, CRC check sum in readout. Improved features for SEU/SET verification. Two alternative sampling modes of hits, etc.). The CMS chip submission has effectively been delayed 6 months because of the required design fix and re-spin of the TOT memories in the RD53B-ATLAS chip, and unfortunate loss of critical and experienced designer and verification collaborators at a very unfortunate moment (replacements found and now engaged in RD53 project). Extensive testing of this chip will start after the summer to verify integration of CMS front-end (was already in RD53A chip), corrected TOT latches, added features and minor bug fixes. A RD53B-CMS chip testing coordinator has been assigned, being an active member of both RD53 and the CMS pixel project. Testing will be closely coordinated with on-going testing activities of the RD53B-ATLAS chip and be reported/discussed in common weekly testing meetings, co-convened by the two assigned testing coordinators.

Required test and DAQ systems for RD53B and RD53C generation chips are made to be compatible. Test cards (single chip card, wafer probe card) have been designed and produced in common as the IO pad frame of the RD53B and RD53C generation chips will be identical. RD53

test systems, with FPGA firmware and software, have been extensively used by the RD53 and pixel detector communities and debugged during testing of the RD53A demonstrator and RD53B chips. Experiment specific DAQ systems have also been trained and debugged with the RD53A and RD53B chips. Simulations are performed of pixel chip (at RTL level) together with test system firmware to assure that test and DAQ systems are appropriately updated for changes made in new chip versions. This assure that test and DAQ systems are immediately working when new chip versions arrive from prototype production.

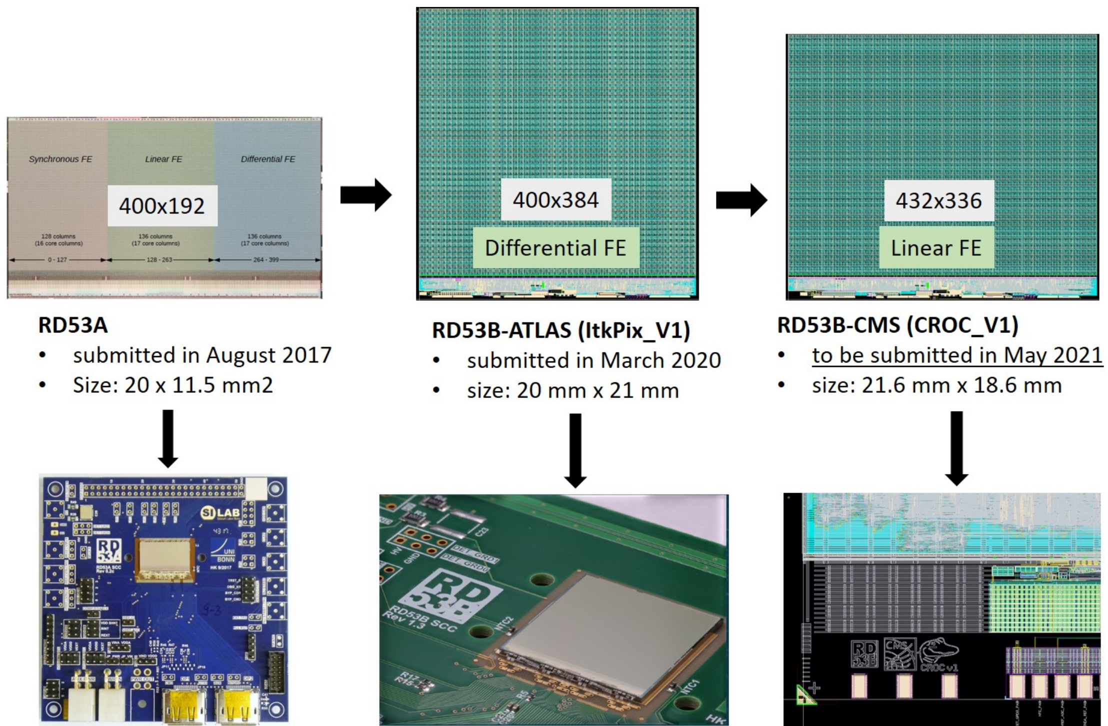

Figure 1. RD53 chips: RD53A demonstrator and the two experiment specific RD53B chips.

2. Design and submission of final RD53C production chips

Final production chips for the two experiments, named RD53C-ATLAS and RD53C-CMS, must be submitted in the first half of 2022 to be compatible with installation schedules of the ATLAS and CMS pixel detectors. The ATLAS version will be submitted first as the larger ATLAS pixel detector needs longer time for construction and installation than the CMS pixel detector (which is fully extractable/insertable). The CMS version can be submitted shortly (3months) after the ATLAS version, but it is highly advisable to delay this until the RD53C-ATLAS chip has been verified to be functional. This implies submitting the CMS chip 4-6 months after the ATLAS chip.

No major functional additions/changes are required for final production chips. Only minor bug fixes and possible improvements will be implemented in final production version chips, to minimize risks for new issues in final chips. IP blocks have been extensively tested in RD53A and RD53B generation chips and will not require modifications. The finalization and submission of production version chips depends critically on exhaustive testing of the RD53B generation chips,

so all possible bugs and issues have been identified at both chip and system level. Exhaustive testing of RD53B generation chips relies on testing on pixel modules, with pixel sensors, and system tests with serial powering that must be done in the pixel detector projects in the experiments. It has been seen that the critical path for this is to have wafer probing tests ready, preparing chips for bump-bonding (under bump metallization and bump deposition), flip-chipping to pixel sensors, mounting and testing of pixel modules in test beams (both non irradiated and irradiated) and system level verification with serial power chains and near final readout configuration (cables, LPGBT, etc.).

The RD53C generation chip submissions will be prepared in parallel with on-going testing and qualification of RD53B generation chips, being done in RD53 and in the ATLAS and CMS pixel projects. The RD53 pixel chip verification framework will be extended and improved to have significantly increased verification coverage at simulation level, based on an industrial standardized methodology: UVM (Universal Verification Methodology). The existing RD53 verification framework is already based on UVM, but needs to be extended/improved during 2021 to assure that no design issues or bugs can be overlooked in final chips. Simulation based verification is in many respects more thorough than what can in practice be obtained in practical chip testing (process corners, radiation corners, SEU and SET verifications, exhaustive and extreme case verifications, etc.).

A major challenge (and cause of submission delays) in submitting RD53B generation chips has been the complex and delicate timing closure of the large complex digital part after place and route. The encountered issues are specifically caused by the extreme conservative timing models required to assure radiation tolerance to the Grad level (gate delays seriously affected by TID above 100Mrad), in combination with the complexity of having TMR, with triplicated clocking, on SEU critical parts of the design . Such issues are not encountered in normal industrial designs and are therefore particularly challenging to resolve with available commercial ASIC design tools. Improved and alternative digital design flows will be evaluated, to assure that the time needed for this final delicate design step can be done with less iterations and manual interventions. As only very minor bug fixes will be applied to final chips, this can be verified well in advance of final chip submissions.

Based on extensive SEU/SET tests of RD53B generation chips during 2021, it will be investigated with detailed analogue simulations, and extended digital SEU/SET injection simulations, if the SEU/SET sensitivity of final chips can be further improved. SEU testing of RD53B generation chips have shown a SEU sensitivity improvement of a factor 400, compared to a non protected design. It has also been verified that if the chip gets affected by SEUs, it normally self recovers quickly without required interventions from the DAQ system. The design and architecture has been specifically made to enable the DAQ system to be capable to recover quickly normal chip functionality individually per chip if needed (control links and readout links organized specifically for this in the pixel detectors). During extensive SEU testing with ions and protons (same flux as in inner level pixel detectors) the RD53B generation chip has not required such fast chip recovery to be applied. An identified issue with occasional very short (microseconds) readout link dropouts is under investigation and is expected to require only simple improvements to the control link differential receiver and possibly the on-chip PLL.

3. Organization and manpower for final chip submissions and testing

RD53 has a well defined project structure in place for the chip submissions, based on specific contributions from different groups (e.g. IP blocks) and experience from previous submissions, as indicated in Figure 2. Manpower issues encountered during the RD53B submissions, with loss of key digital designer and verification expert, have been been resolved with new collaborators that have actively contributed to the RD53B-CMS chip and will remain engaged for final chip submissions.

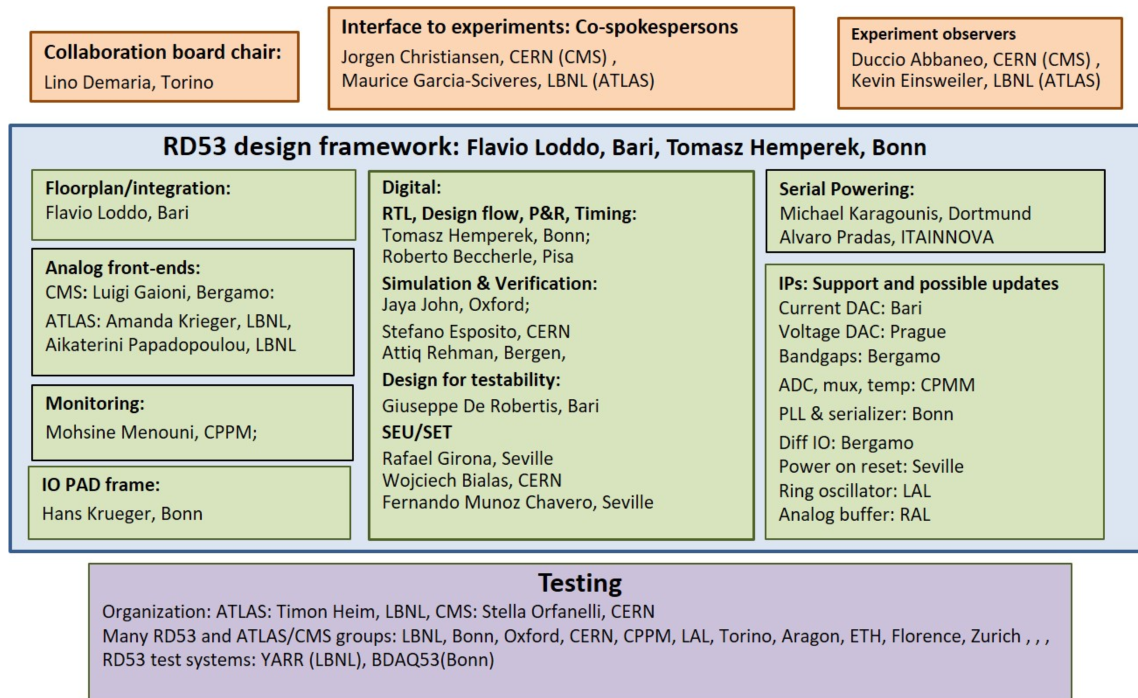

Figure 2. RD53 chip design, verification and testing organization

Testing and qualification of the pixel chips for the two experiments are organized with specific testing coordinators for each experiment. These coordinators are full, and long time, members of the RD53 collaboration (and management board) and co-nominated by RD53 and the experiments. This assures good and efficient organization and verification of the two chip versions in close collaboration between the RD53 design team and the chip/system testing teams in the two experiments. Tests and test results are organized and presented in a weekly common chip testing meeting, assuring the best possible synergy for the critical test and qualification.

4. Studies for future pixel upgrades with 28nm CMOS technology

It is known that both the CMS and ATLAS experiments will have to replace their inner-most pixel detector layers after 5years running at full HL-LHC luminosity, because of expected radiation damage to pixel chips and sensors. This replacement of a small number (less than 10%) of pixel modules is currently assumed done with pixel modules based on RD53C generation chips. This

is though a possible occasion to replace inner pixel layer modules with higher performance (e.g. better track resolution, high time resolution, two level trigger) pixel detector modules, based on a potential new pixel chip in a 28nm CMOS technology, that have shown indications of excellent radiation tolerance. Initial discussions have started on this within the RD53 collaboration and with the experiments. The extensive experience accumulated in RD53 on collaborative development of complex pixel chips for extreme rates and radiation will be a major advantage for developing such a new pixel chip. This will be evaluated over the coming 1-2years, to determine if a focussed R&D on this should be started in RD53. This will obviously not be allowed to interfere with the finalization of the RD53C chips, and can possibly help to keep certain groups and people engaged in this absolute highest priority task.

5. CERN Resources

The majority of the work takes place at the collaborators' respective institutes. In the past a significant productivity gain was obtained getting the core design team together at CERN in the last months before submissions. This has unfortunately been impossible in the last 2 years because of the exceptional COVID19 situation. Two key designers have been hosted at CERN to assure their effective contributions and access to IC design tools. We will possible again (if allowed according to COVID regulations) get the core design team together for a limited time at CERN for the submission of final RD53C chips and temporary office space in building 14 (or nearby) may be needed.

The design work is enabled by the CERN frame contract with TSMC already in place and the corresponding 65 nm design kit, managed by the CERN IC group, including legal authorizations though letters of compliance. As CERN makes all formal orders via the frame contract, produced wafers are delivered to CERN. Appropriate handling and logistics of the experiment specific chips and wafers will be organized by the experiments.

CERN computing resources are used to host the design repository, digital code, and verification environment. Access and use of CERN IC design tools are required for collaborators located at CERN for extended periods. This is not anticipated to increase for making final production chips.

CERN testing labs, Irradiation facilities and test beams will be used for chip testing and characterization. Many facilities outside CERN are also used for irradiation, SEU tests and beam tests.

CERN manpower (Co-spokesperson, ASIC verification expert, fellow for chip testing and logistics, administration support) is assumed to be kept at same level as now, until finalization of the project (or specific tasks). Financial resources at the level of 50-100K per year is assumed to be made available for chip testing infrastructure, travelling, meetings and general logistics for the collaboration.

References

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