The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

10 October 2020 (v7, 14 February 2021)

Status of the Phase-2 Tracker Upgrade of the CMS experiment at the HL-LHC

Luigi Calligaris for the CMS Collaboration

Abstract

The Phase-2 Upgrade of the CMS experiment is designed to prepare its detectors for operations at the High Luminosity Large Hadron Collider (HL-LHC). The upgraded collider, scheduled to start operations in 2027, will lead to challenging conditions in terms of data throughput, pile-up and radiation. For these reasons the tracker detector will be entirely replaced by a new detector, the Phase-2 tracker. We present the status of the design, test and validation of the components of the Phase-2 tracker, and its read-out, calibration, control, and data processing chains [1].

Presented at *ICPPA-2020 5th International Conference on Particle Physics and Astrophysics*

PAPER • OPEN ACCESS

Status of the Phase-2 Tracker Upgrade of the CMS experiment at the HL-LHC

To cite this article: Luigi Calligaris and on behalf of the CMS collaboration 2020 *J. Phys.: Conf. Ser.* **1690** 012039

View the article online for updates and enhancements.

Status of the Phase-2 Tracker Upgrade of the CMS experiment at the HL-LHC

Luigi Calligaris *on behalf of the CMS collaboration*

Universidade Estadual Paulista "Júlio de Mesquita Filho", Rua Dr. Bento Teobaldo Ferraz, 271, Bloco II - Térreo, 01140-070 São Paulo, Brazil

E-mail: `luigi.calligaris@cern.ch`

Abstract. The Phase-2 Upgrade of the CMS experiment is designed to prepare its detectors for operations at the High Luminosity Large Hadron Collider (HL-LHC). The upgraded collider, scheduled to start operations in 2027, will lead to challenging conditions in terms of data throughput, pile-up and radiation. For these reasons the tracker detector will be entirely replaced by a new detector, the Phase-2 tracker. We present the status of the design, test and validation of the components of the Phase-2 tracker, and its read-out, calibration, control, and data processing chains.

1. Introduction

The High-Luminosity LHC upgrade program [1], planned to be complete by 2027, aims to increase the instantaneous luminosity of the LHC machine from the current values of the order of 1.5-1.9 $\cdot$ 10^{34}cm$^{-2}s^{-1}$ to a nominal value of $5 \cdot 10^{34}$cm$^{-2}s^{-1}$, with provisions to eventually reach a luminosity of up to around $7.5 \cdot 10^{34}$cm$^{-2}s^{-1}$. These values correspond to a number of pile-up interactions of 140 and 200, respectively, and such conditions pose a serious challenge for the consistent and effective operation of the existing detectors. As a consequence, a number of important upgrades to the experiments are in commissioning or under development.

The CMS [2] detector at the LHC will replace or upgrade most of its detectors under a program named "Phase-2 Upgrade", in preparation for its operations at the HL-LHC. In this publication we focus on the upgrade of the tracker detector [3], which is currently subject to an intense research and development effort, prior to the beginning of the manufacturing phase for its various components.

2. The CMS Phase-2 Tracker

During the Phase-2 upgrade the existing tracker detector will be completely replaced by a new one, composed of two main parts: an *Inner Tracker* (IT) and an *Outer Tracker* (OT). The structure of the new tracker, along with the positioning of the different kinds of sensor modules, is shown in figure 1.

The IT detector design aims to resolve the origin of the observed charged particle tracks, for example a primary proton-proton collision vertex or a secondary vertex from the decay of a long-lived particle, and to provide good quality seeds to be used for the offline reconstruction of tracks. These tasks need to be performed in an environment characterized by the most intense

particle fluxes in the detector, with significant ionizing radiation doses and with important constraints on the detector's material budget.

At each collision event the IT detector modules store the detected hits in a local buffer, part of the read-out chips, and these hits are later read out of the detector to the back-end electronics if the event is accepted by the level-1 trigger. Similarly to the IT, the OT stores detected hits locally, and reads them out for those collision events that have passed the level-1 trigger selection. The sets of hits from the IT and the OT constitute the *DAQ stream*, and are used to reconstruct tracks in the HLT and in offline event reconstruction.

A distinguishing aspect of the OT is that, for all collision events, it provides to the level-1 trigger a set of high transverse momentum tracks, reconstructed by powerful online track-finding processors, to aid the trigger in the L1 accept decision. This latter function drives the design of the OT detector and the design of its back-end.
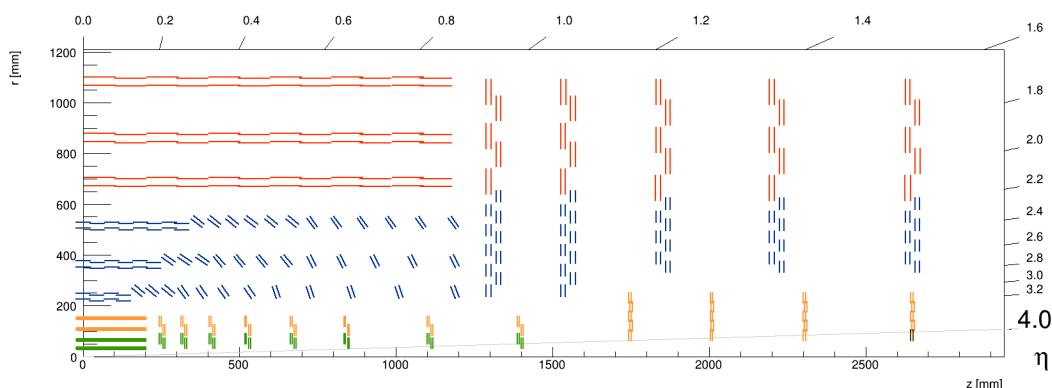

Figure 1. Layout of the CMS Phase-2 Tracker, showing Inner Tracker 2x1 (green) and 2x2 (orange) modules, and Outer Tracker PS (blue) and 2S modules (red).

3. Inner Tracker

The IT [4] is composed of four barrel layers, eight endcap disks and four endcap extension disks on each side along the beam axis, which allow it to will cover a range of pseudorapidities up to $|\eta| = 4.0$ using two types of pixel detector modules: a two-chip design (2x1 module) with high read-out rate capability to be used in the regions closest to the beam pipe, and a four-chip, lower rate design (2x2 module) to be used in the other regions of the detector. The use of just two types of modules makes the manufacturing process easier, and allows for a simpler servicing of the detector over the years of operations.

In order to cope with the increase in the flux of charged particles expected after the HL-LHC upgrade, the pixels used in IT sensors will have an area of 2500 μm^2, which is 1/6 the area of the current CMS pixel detector. Currently, different kinds of sensors are being evaluated for use, some of which are shown in figure 2. The sensors will employ either planar or 3-dimensional pixel detector technology, with the latter one of particular interest for use in the inner layers, thanks to their shorter charge drift length and therefore better radiation resistance properties.

The IT sensors will be read out by ASICs bump-bonded to the sensors in a flip-chip configuration. These "CMS Read Out Chips" (CROC) are based on the RD53 project [5, 6], a common ATLAS-CMS effort designing highly integrated pixel detectors in which the analog front-end circuitry, corresponding to each read-out pad, is embedded in a "sea" of digital logic tasked with the digitization of the signal and its read-out. CROC will also enable the serial powering of the sensor modules by including among its peripherals a shunt-LDO regulator, able to tap from the serial power chain the current required for its operation.
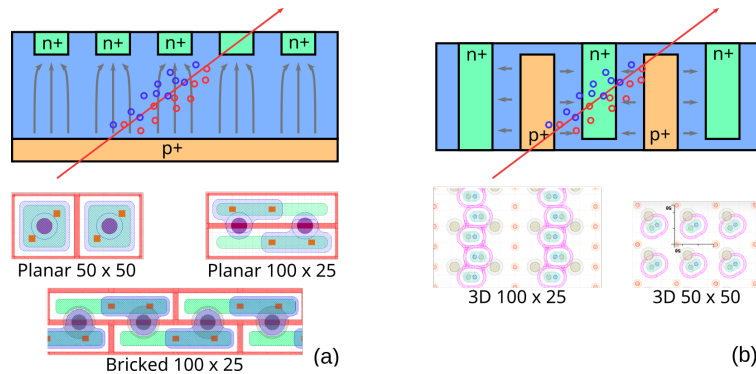
Figure 2. Top: schematic of a planar (a) and one type of 3D (b) pixel sensor. Bottom: top view of some types of planar (a) and 3D (b) pixel configurations under study for the IT, all of which are further described in the text. All dimensions are in μm.

The serial powering scheme plans to power up to 12 modules with a single circuit, leading to a significant saving in the number of low-voltage power cables that need to be run into the detector. This reduction in the amount of cables, and therefore the overall material budget of the IT, improves the measurements performed by the other detectors of the experiment, since particles have to pass through less material to reach them. Following promising tests on RD53 prototypes, the design of CROC is now underway and a prototype for the final chip is expected soon.

4. Outer Tracker

The OT is composed of six barrel layers and five endcap disks on each of its sides, with a coverage in pseudorapidity of up to $|\eta| = 2.4$. The detector is composed of dual-sensor detector modules, known as "p_T-modules" [7], where the two parallel sensors are separated by a gap of a few mm. This geometrical arrangement allows to correlate hits from the two sensors using dedicated logic contained in the read-out ASICs, and select pairs of hits (known as "stubs") compatible with tracks having a transverse momentum higher than a set treshold, which is a function of the configurable width of the correlation window (figure 3).
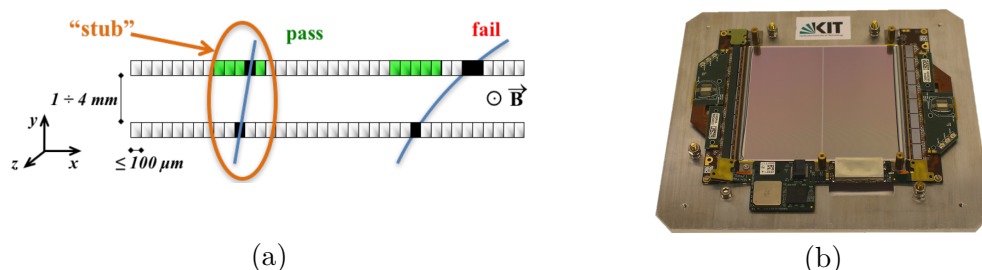

Figure 3. (a) Schematic showing the functioning of a p_T module: the high-p_T track on the left hits the module with a steep angle, falling into the green correlation window and producing a stub, while the low-p_T track on the right impacts the module with a shallow angle due to the magnetic field bending its trajectory, such that it falls out of the correlation window and doesn't generate a stub. (b) A fully assembled prototype Outer Tracker 2S module. The sensors at the center are read out on each side by 8 CBC ASICs hosted on a PCB hybrid, which contains the CIC chip. The CICs send stubs and hits to the service hybrid containing the optoelectronic link, in the foreground.

The correlation window is chosen such that only those stubs which will lead to the reconstruction of interesting tracks for the level-1 trigger (around 2.4% of all tracks if the cut-off is set at 2 GeV) are read out of the detector modules, greatly reducing the amount of bandwidth needed and bringing it into a range that is practical for current technology.

Two types of detector modules are employed in the OT. The *PS modules* use a pixel sensor and a microstrip sensor to detect particles. The pixel sensor is composed of long pixels with a pitch of 100 μm in the $r\phi$ plane and a length of 1.5 mm. The microstrip sensor has a pitch of 100 μm in the $r\phi$ plane and a strip length of 5 cm. Both sensors have a length of 10 cm in the $r\phi$ plane and a width of 5 cm. The modules are tilted in the forward regions of the barrel, such that they are oriented normally to the average trajectory of the particles coming from the collisions. The PS modules are used in the three innermost barrel layers and the endcap disk regions closest to the beam pipe. The *2S modules* use two microstrip sensors to detect particles. The sensors have a length and width of 10 cm, a pitch of 90 μm in the $r\phi$ plane and a strip length of 5 cm along the z axis. The 2S modules are used in the rest of the OT.

In each PS module the microstrip sensor is read by 16 Short Strip ASICs (SSA)[8], eight per side with 120 channels each, which are mounted on a flexible PCB resting on a support structure and connected through wire-bonds to the sensor pads. The pixel sensor is read by 16 Macro Pixel ASICs (MPA)[9], each having 1888 channels, arranged in a 2 x 8 matrix and bump-bonded to the sensors. Each MPA is connected to a corresponding SSA via wire bonds and the aforementioned flexible PCB, such that the SSAs can send hits to the MPAs and the latter can identify stubs using its internal hit correlation logic.

In the 2S modules the strips are read out by 16 CMS Binary Chips (CBCs)[10], eight on each side with 127 channels each, which contain the stub correlation logic.

Both PS and 2S modules host a pair of Concentrator ICs (CICs)[11], which have the task of multiplexing stubs and hits sent by the individual read-out chips into a set of common serial electrical connections (e-links), prioritizing stubs that match higher transverse impulse tracks. The e-links lead to the PCB hybrid holding the optical read-out electronics. In the case of the 2S modules, the DC-DC converters used to power the on-module chips are located on the same PCB hybrid as the optical read-out electronics, called *Service Hybrid*, while in the case of the PS modules two PCBs, the *Power Hybrid* and the *Read-Out Hybrid* lie in opposite positions of the module.

The preliminary production series for the PS and 2S sensors and front-end read-out chips has shown excellent results, and mass production for most of the components is expected to begin in the second half of 2020, such that assembly of modules could start he following year.

5. Back-end systems

Both the IT and OT modules communicate optically with the back-end electronics through low power GigaBit Transceiver (lpGBT) links [12], which run at speeds of either 5 or 10 Gbps in uplink (from front-end to DAQ) and 2.56 Gbps in downlink. In the case of the OT, the lpGBT ASICs, lasers and photodiodes are hosted directly on the detector modules, while in the case of the IT they are hosted on separate portcards, located at a larger distance from the beam and connected to the module via e-links running over differential pairs.

In the service cavern, Data Trigger and Control (DTC) cards hosted in dedicated racks sit at the opposite end of the lpGBT optical links coming from the IT and OT modules. The DTCs are high bandwidth processors, tasked with receiving hits pertaining to triggered events from up to 72 detector modules and sending them to the DAQ system (which forwards them to the High Level Trigger), controlling, monitoring the health of and calibrating the detector modules, sending to the modules timing and synchronization information and, in the case of the OT, forwarding the stubs to the Track Finder Processors (TFPs) after converting the stub coordinates from the module-local to the global reference frame. Prototypes of the DTCs

have been produced: the Serenity board [13] targeting the role of DTC for the OT, while the Apollo board [14] targeting the role of DTC for the IT and of TFP. To meet the elevated processing and bandwidth requirements (up to 720 Gbps per card) DTCs use high performance Xilinx Ultrascale+ Virtex FPGAs and 12-channel, 25 Gbps-per-channel optical transceivers to implement their functions.
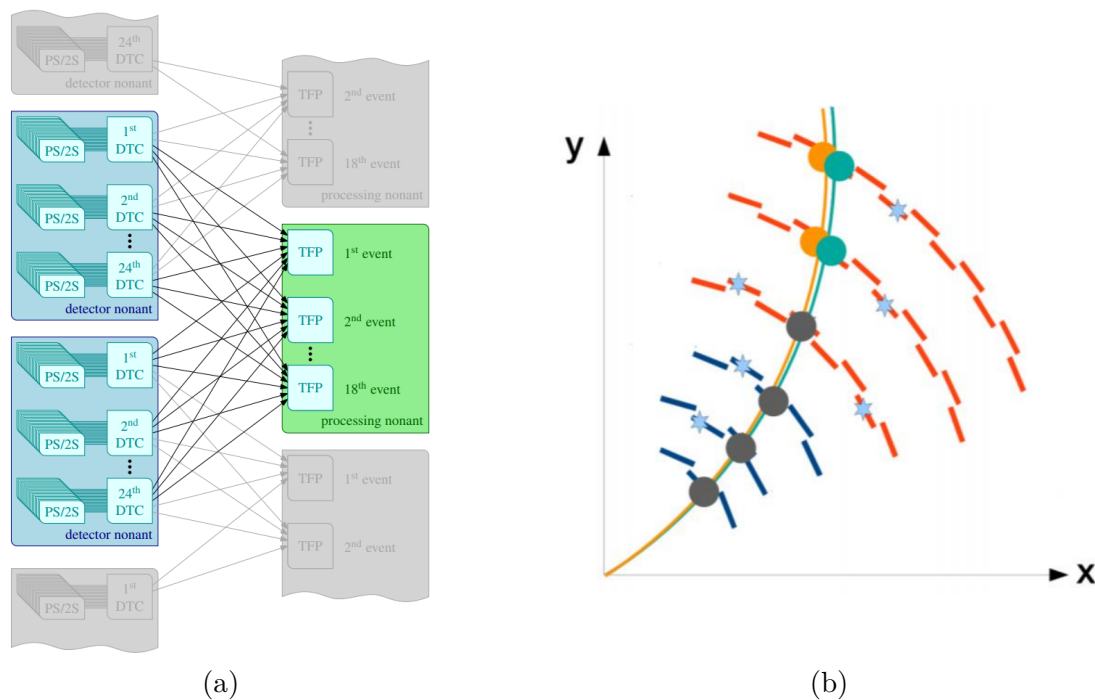

(a) (b)

Figure 4. (a) Interconnection of the DTCs with the TFPs as part of the time-multiplex arrangement. (b) Illustration of the road search algorithm used in track finding.

For all the events, the OT back-end system needs to find tracks with a latency short enough to leave the L1 trigger enough time to process the event and take the L1 accept decision. Overall, the total latency cannot exceed 12.5 μs, as this is the length of the event buffers across the various detectors of the experiment. This brings a number of challenging requirements for the back-end system (4 μs maximum latency to process an event, 40 MHz event rate, order of 20000 stubs per event), which requires a massive amount of computing power. This is accomplished through a *divide and conquer* strategy where the detector is divided in nine azimuthal *nonants*, each served by a group of DTCs and TFPs. Futhermore, in each nonant, 18 identical instances of the track finding system run in parallel, taking turns in the analysis of events in round-robin. This technique, called *time-multiplex* allows further parallelization of the track reconstruction task.

A TFP uses one or two high performance Xilinx virtex Ultrascale+ FPGAs to reconstruct tracks from the stubs received from 18 DTCs, as shown in figure 4. It is planned that the TPFs will run a *hybrid algorithm*, which merges the benefits of two previously demonstrated algorithms, the TMTT [15] and Tracklet [16]: pairs of stubs in different layers act as seeds for an iterative algorithm, which matches stubs to computed trajectory estimations and updates the latter with the new matches. Subsequently, the track candidates are processed by a Kálmán algorithm, which fits their track parameters. Finally the tracks are sent to the L1 trigger system. Overall, the OT tracker back-end system is expected to be able to reconstruct 300 tracks per event, equivalent to 12 billion tracks per second. The development of the hybrid algorithm is

currently in progress.

6. Conclusion

The Phase-2 upgrade of the CMS tracker is a significant effort involving the participation of many different groups working on different aspects of the inner and outer tracker detectors, from the development of the sensors, to the read-out ASICs, to the sensor modules, to the back-end systems. An important number of R&D activities will come to an end soon with the finalization of the designs and the beginning of the manufacturing phase for the various components.

Acknowledgments

References

[1] Apollinari G *et al.* 2017 URL `http://cds.cern.ch/record/2284929`
[2] Chatrchyan S *et al.* (CMS Collaboration) 2008 *J. Instrum.* **3** S08004
[3] CMS Collaboration 2017 The Phase-2 Upgrade of the CMS Tracker Tech. Rep. CERN-LHCC-2017-009. CMS-TDR-014 URL `https://cds.cern.ch/record/2272264`
[4] Orfanelli S (CMS Collaboration) 2020 *Nucl. Instrum. Meth.* A **980** 164396
[5] Gaioni L *et al.* (RD53 Collaboration) 2019 *Nucl. Instrum. Meth.* A **936** 282–285
[6] Demaria N *et al.* 2016 *J. Instrum.* **11** C12058
[7] Pesaresi M and Hall G 2010 *J. Instrum.* **5** C08003
[8] Caratelli A, Ceresa D, Kaplon J, Kloukinas K, Leblebici Y, Murdzek J and Scarfi S 2018 *PoS Proc. Sci.* **TWEPP2017** 031
[9] Ceresa D, Marchioro A, Kloukinas K, Kaplon J, Bialas W, Re V, Traversi G, Gaioni L and Ratti L 2014 *J. Instrum.* **9** C11012
[10] Prydderch M L *et al.* 2018 *PoS Proc. Sci.* **TWEPP2017** 001
[11] Nodari B, Caponetto L, Galbit G C, Viret S and Scarfi S 2019 *PoS Proc. Sci.* **TWEPP2018** 099
[12] Mendez J M, Baron S, Kulis S and Fonseca J 2019 *PoS Proc. Sci.* **TWEPP2018** 059
[13] Rose A *et al.* 2019 *PoS Proc. Sci.* **TWEPP2018** 115
[14] Albert A *et al.* 2020 **TWEPP2019** 120 (*Preprint* `1911.06452`)
[15] Tomalin I *et al.* 2017 *J. Instrum.* **12** P12019
[16] Bartz E *et al.* 2020 *J. Instrum.* **15** P06024 (*Preprint* `1910.09970`)