ATLAS muon gaseous chamber technologies for a detector at the ILC

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International Workshop on Future Linear Colliders (LCWS2021)

18 March 2021

Introduction

A sequence of LHC upgrades are scheduled during Long Shutdown (LS) periods.

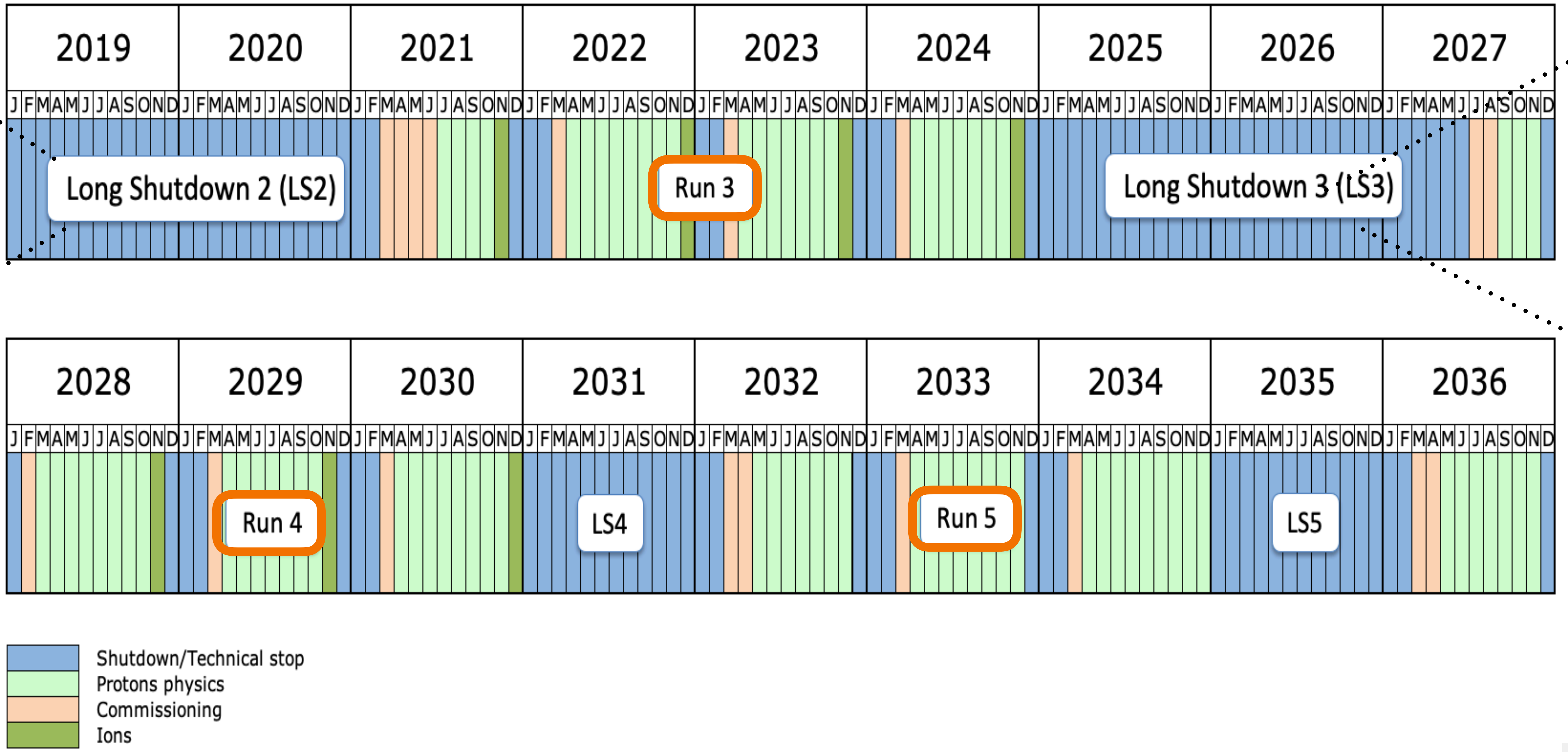
- Instantaneous luminosity expected to increase up to 5 to 7 times higher than nominal following **LS3** in **2027**.
- After the LS2 (2019-2020), LHC will reach design energy 14 TeV and collision intensity L=2x10^{34}cm^{-2}s^{-1}.
- Expect to collect approximately **3000 fb^{-1}** of data by the end of LHC operations in **2037**.

ATLAS Upgrade projects(LS2)

New Small Wheel

LAr calorimeter

Fast tracker



ATLAS Upgrade projects(LS3)

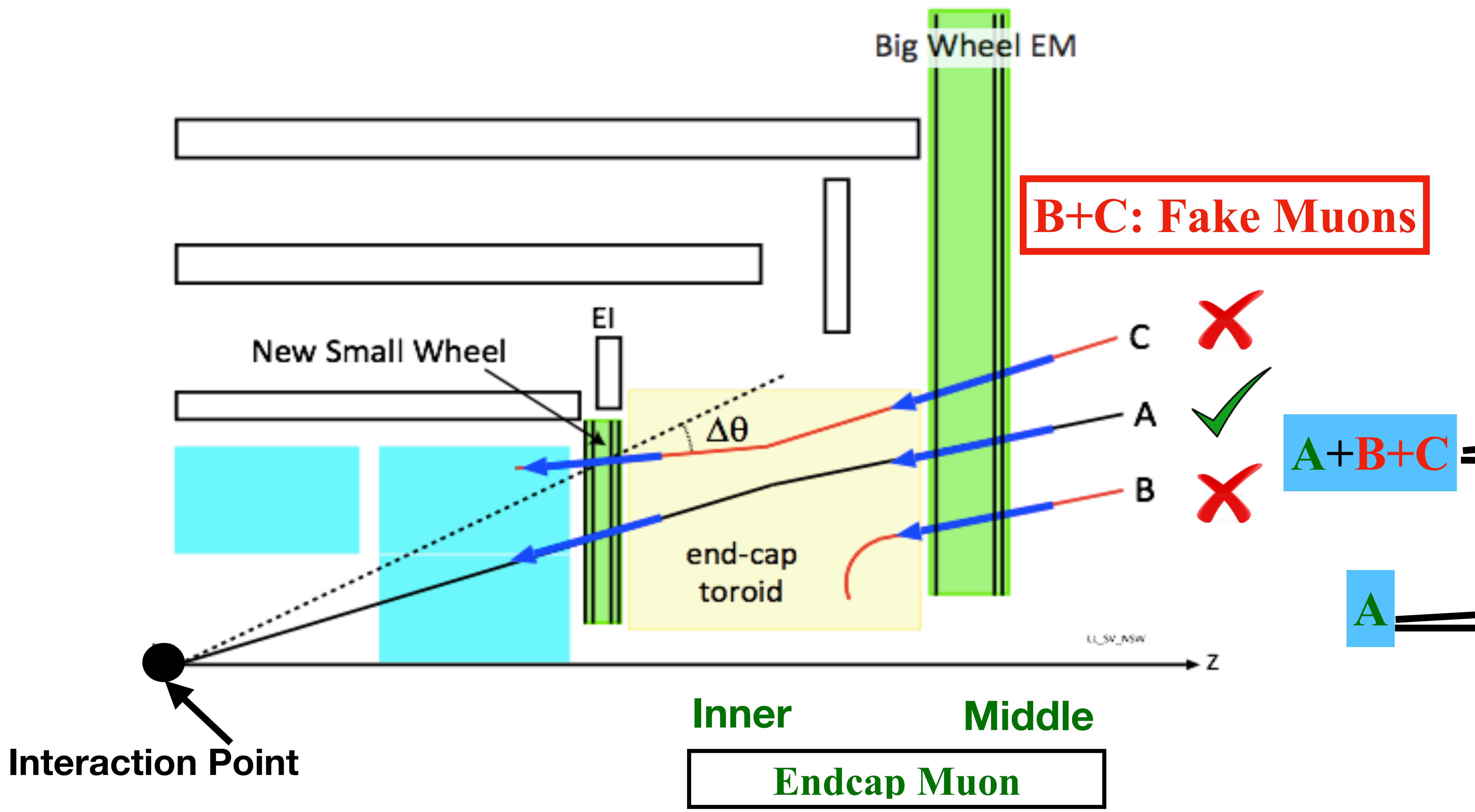
Muon System

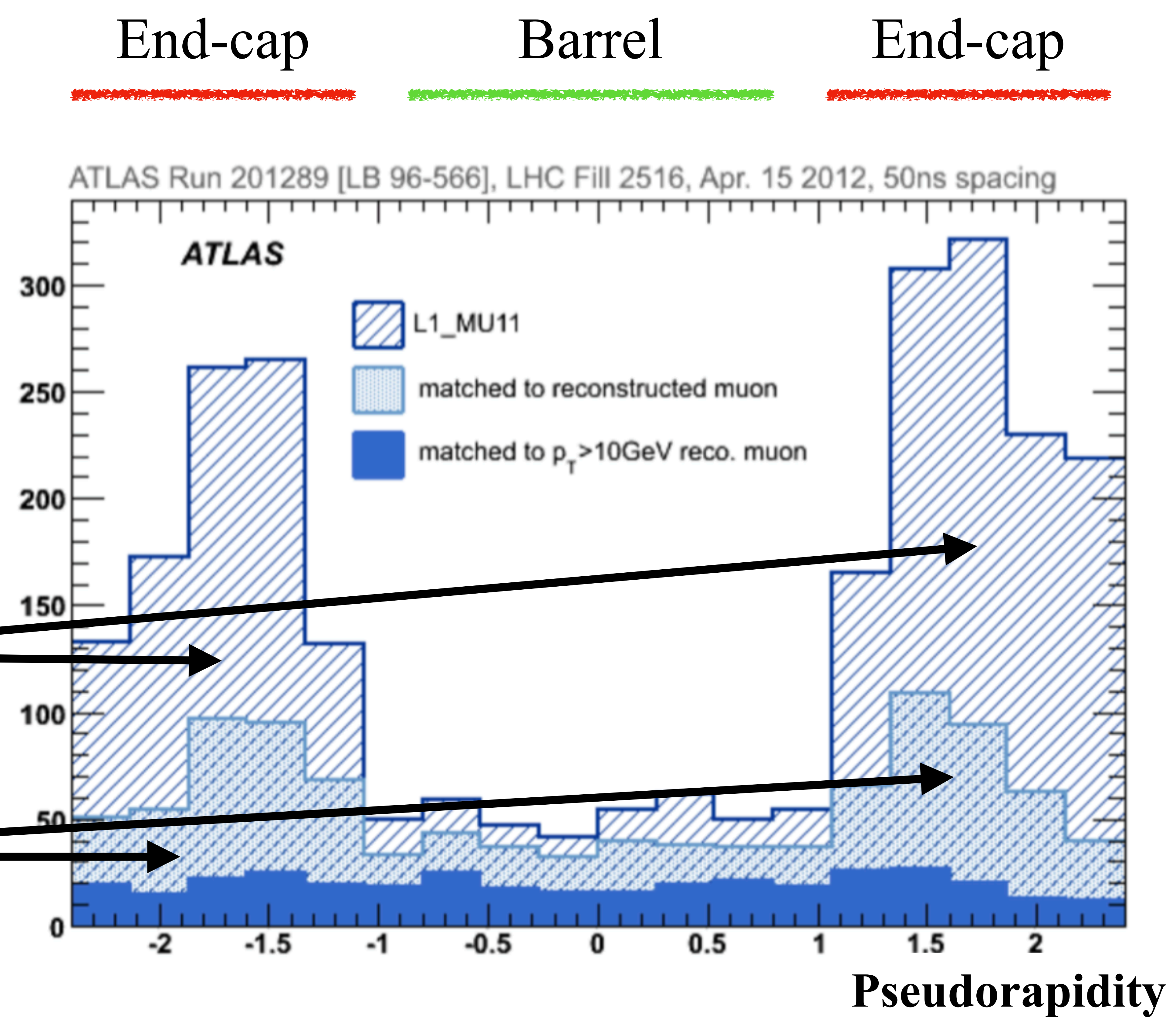
Inner tracker

LAr and Tile calorimeters

DAQ and trigger systems

Trigger Rate & Identification Limitations





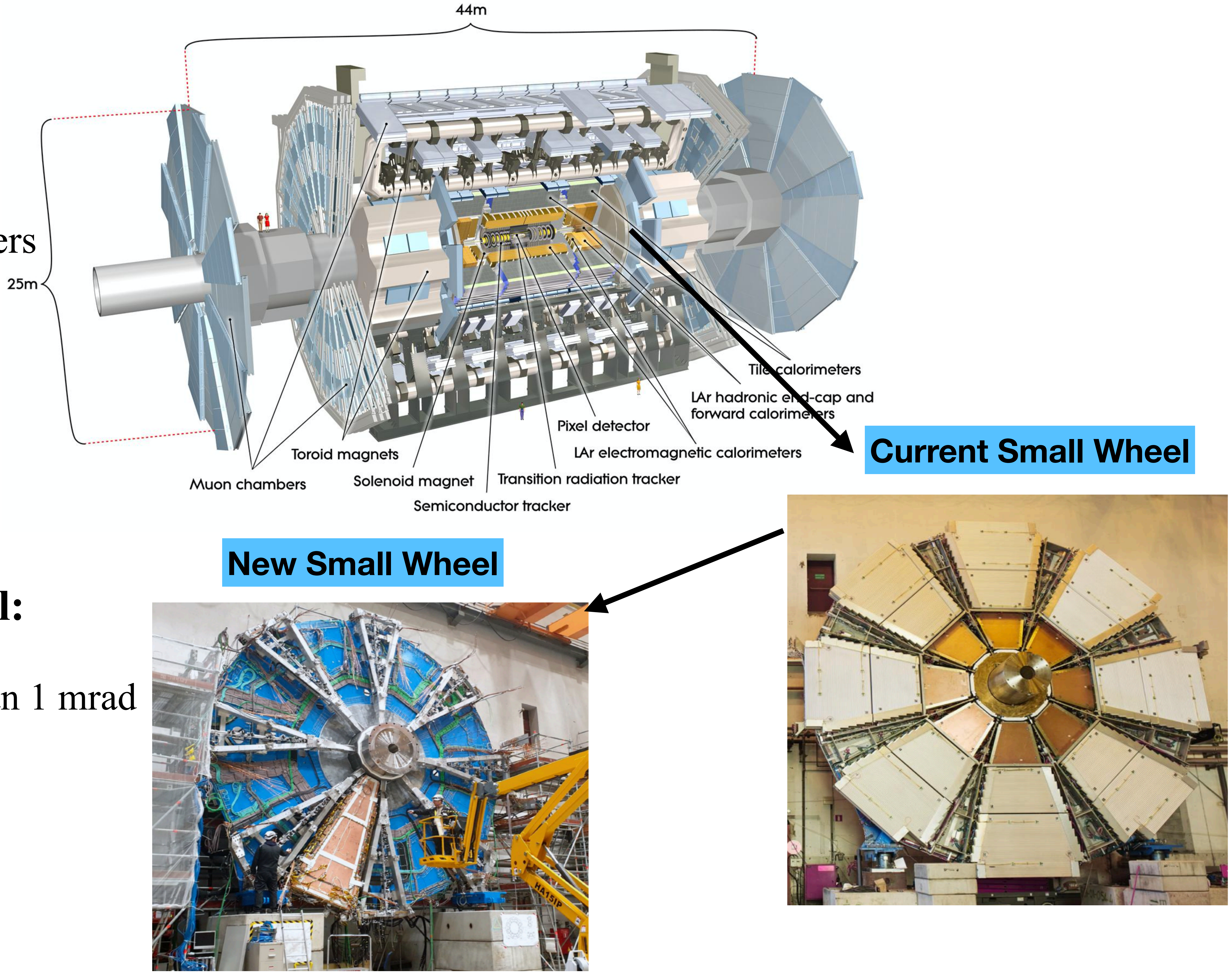
Online Muon Identification: Current Wheel Chambers will lose efficiency at high hit rates due to higher instantaneous luminosity.

- Current Muon system only uses middle wheel for triggering; it would not be able to hold such rate.

Trigger limitations: Lowest unprescaled muon trigger is dominated by fake muons (90%) in the endcap region which waste the bandwidth of the HLT.

ATLAS-Muon Spectrometer Upgrade

Solution: The New Small Wheel(NSW) upgrade will replace the current Small Wheel of the ATLAS Muon Spectrometer to handle tracking and triggering problems.



It is designed to:

- Significantly reduce the fake Level-1 muon triggers
- Precisely reconstruct muon tracks
  - 95% on-line track reconstruction efficiency

Strict Requirements for the new small wheel:

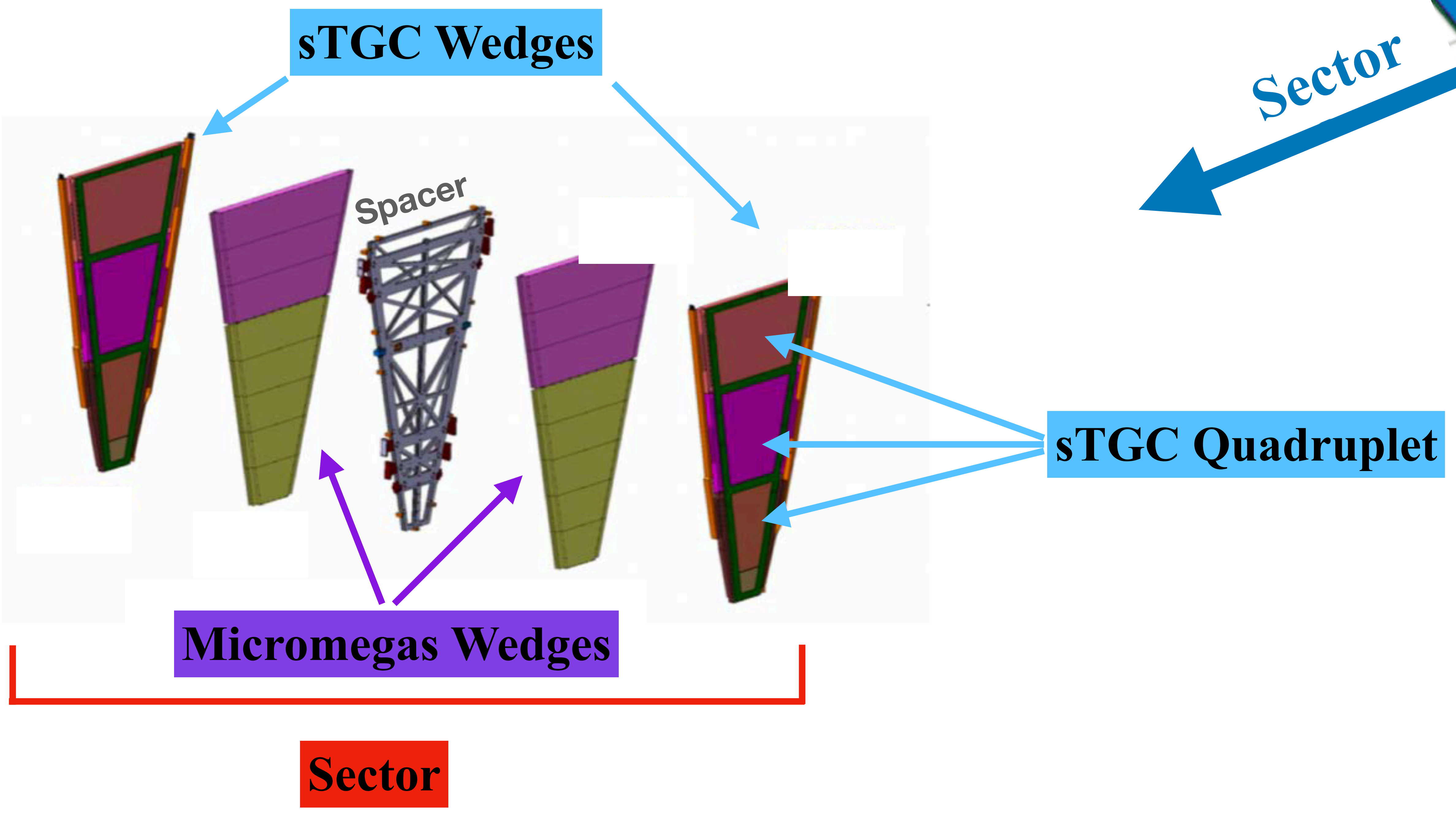
- Excellent online angular spatial resolution; less than 1 mrad
- Operate efficiently at Run-3 and beyond it

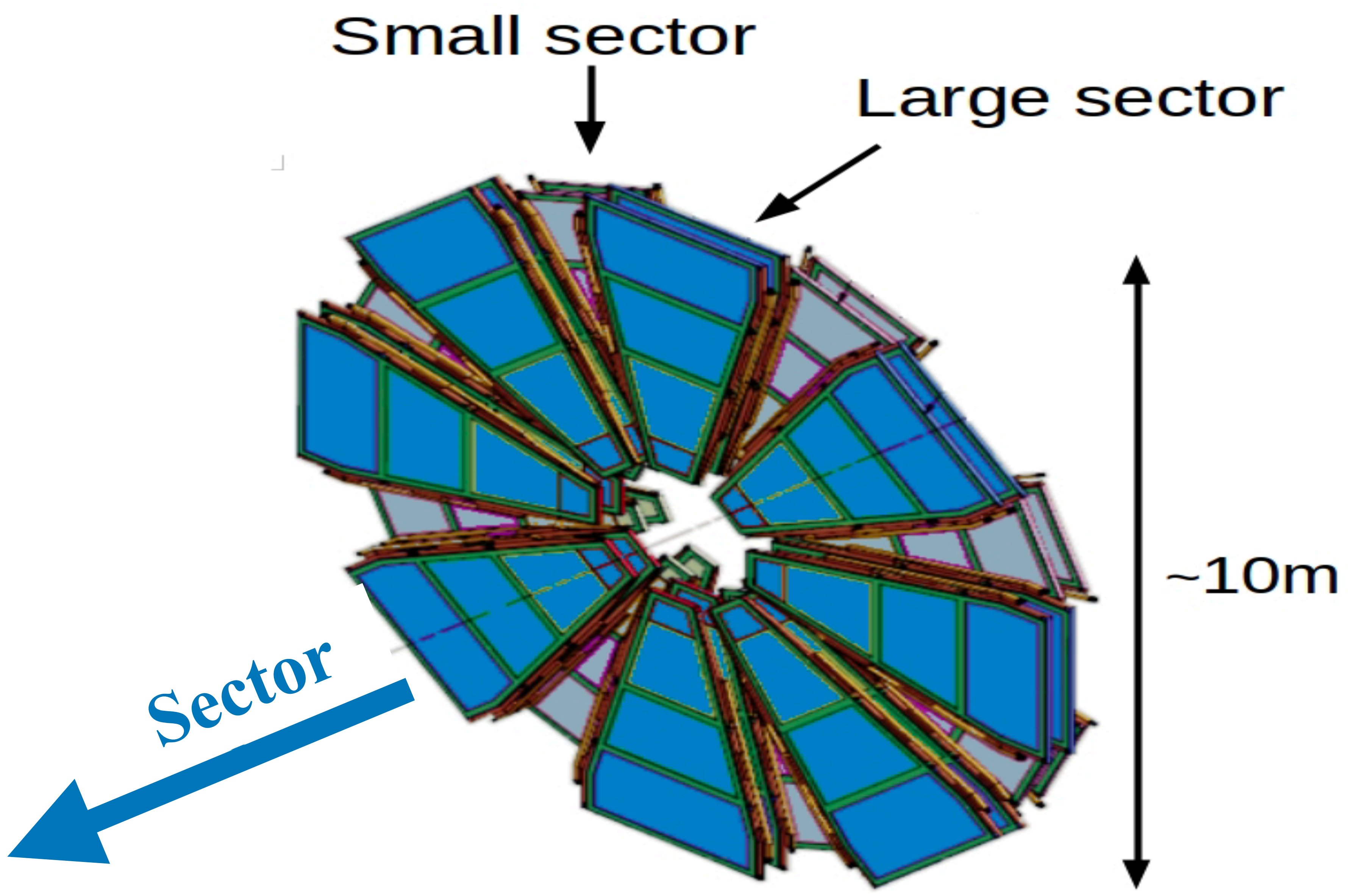
The NSW is composed of 16 trapezoid sectors, each sector being made of two detector technologies:

- The Micromegas (MM) designed for precision tracking
- The small-strip Thin Gap Chambers (sTGC) optimized for triggering

Each sector is made of 2 sTGC wedges and 2 MM wedges.

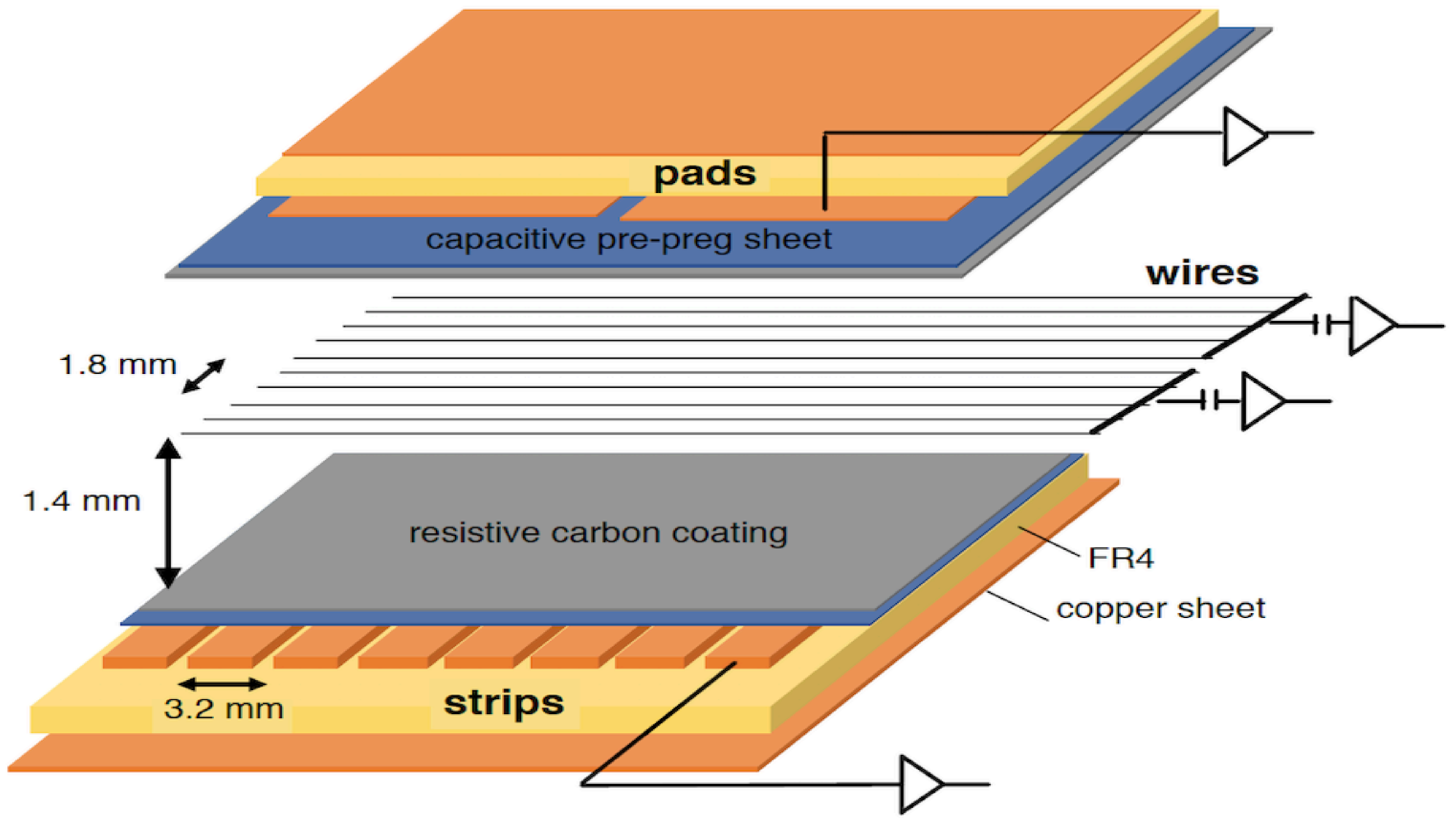
- The sTGC wedges are made up of 3 quadruplets modules
- Each quadruplet is a multiplet with 4 sTGC layers



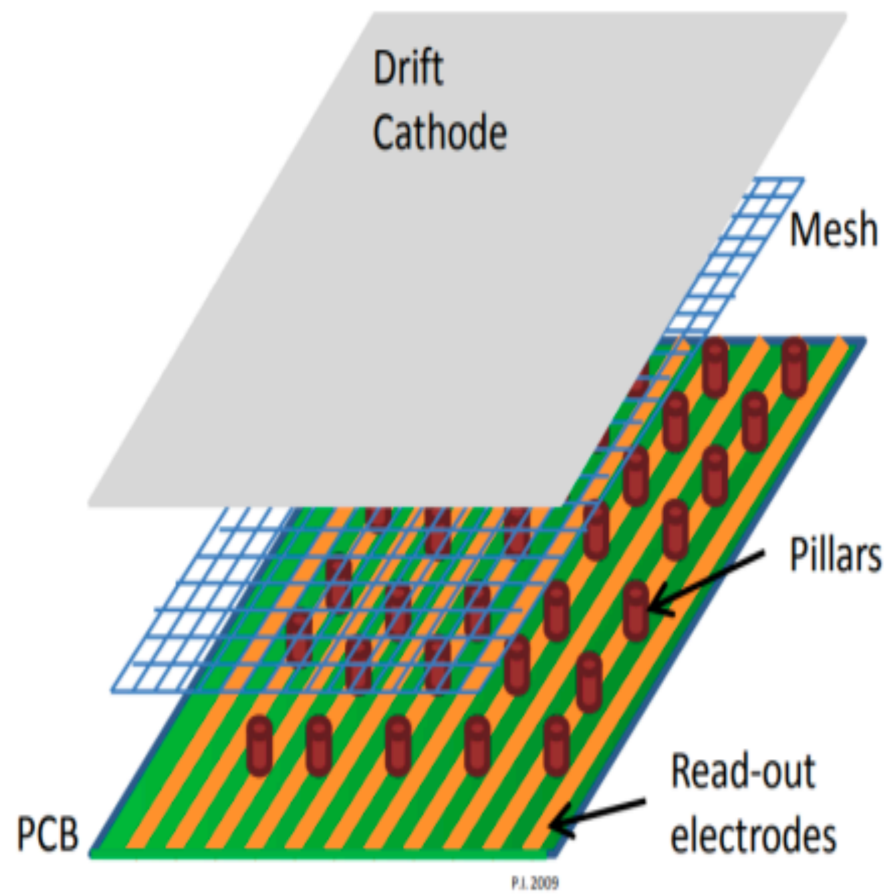


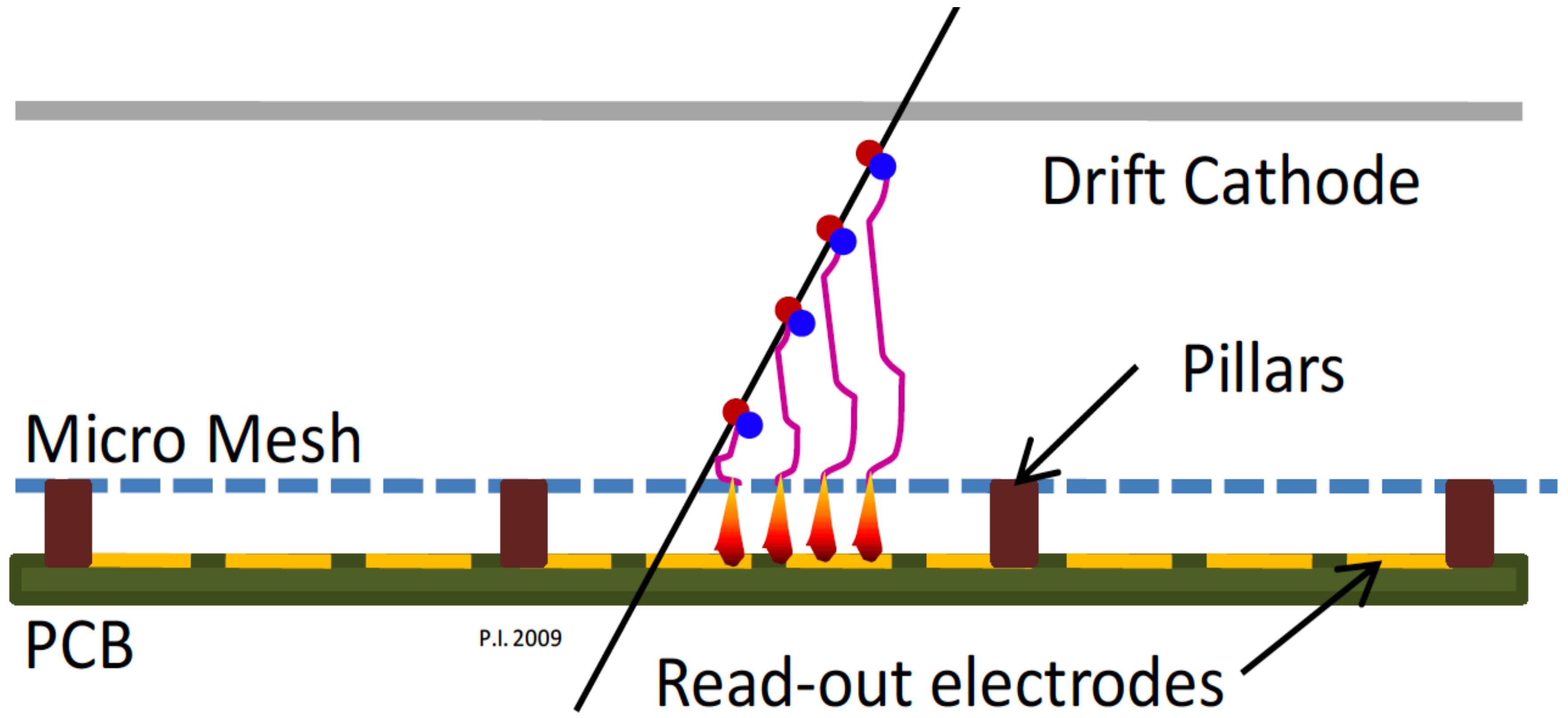
New Small Wheel

sTGC detector



Micromegas detector





<u>Mainly for triggering, also for good tracking</u>

- Good timing resolution with short drift time for electrons
- Small strip pitch (3.2 mm)
  - less than 1 mrad trigger track resolution

It will provide a ~ 7 fold increase in rejection rate for fake muon triggers.

<u>Mainly for precise tracking, also for triggering</u>

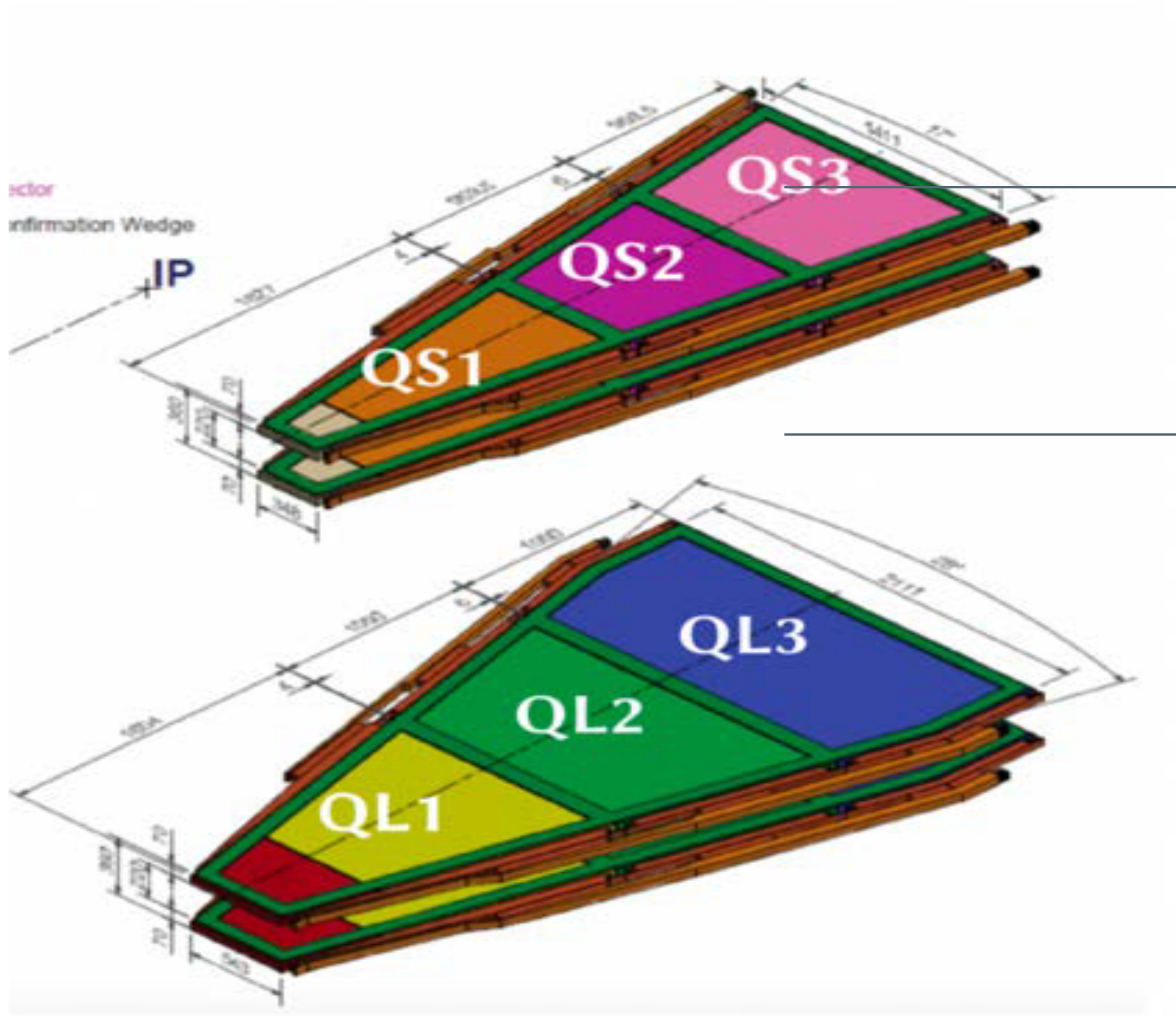
- Small strip pitch (~0.4 mm)
- Fast drift time (~100 ns)

It will reach space resolution < 100 μm independent of track incidence angle.

sTGC Construction Sites

sTGC quadruplets (each with 4 layers) are assembled at independent construction sites located in 5 countries.

sTGC Production Sites		
Canada	TRIUMF, Carleton University, McGill University	1/2QS3 QL2
China	Shandong University	QS2
Chile	Pontifical Catholic University of Chile, Federico Santa Maria Technical University	QS1
Israel	Weizmann Institute of Science, Tel Aviv University	1/2QS3 QL1
Russia	NRC Kurchatov Institute PNPI, Petersburg Nuclear Physics Institute	QL3



sTGC Modules

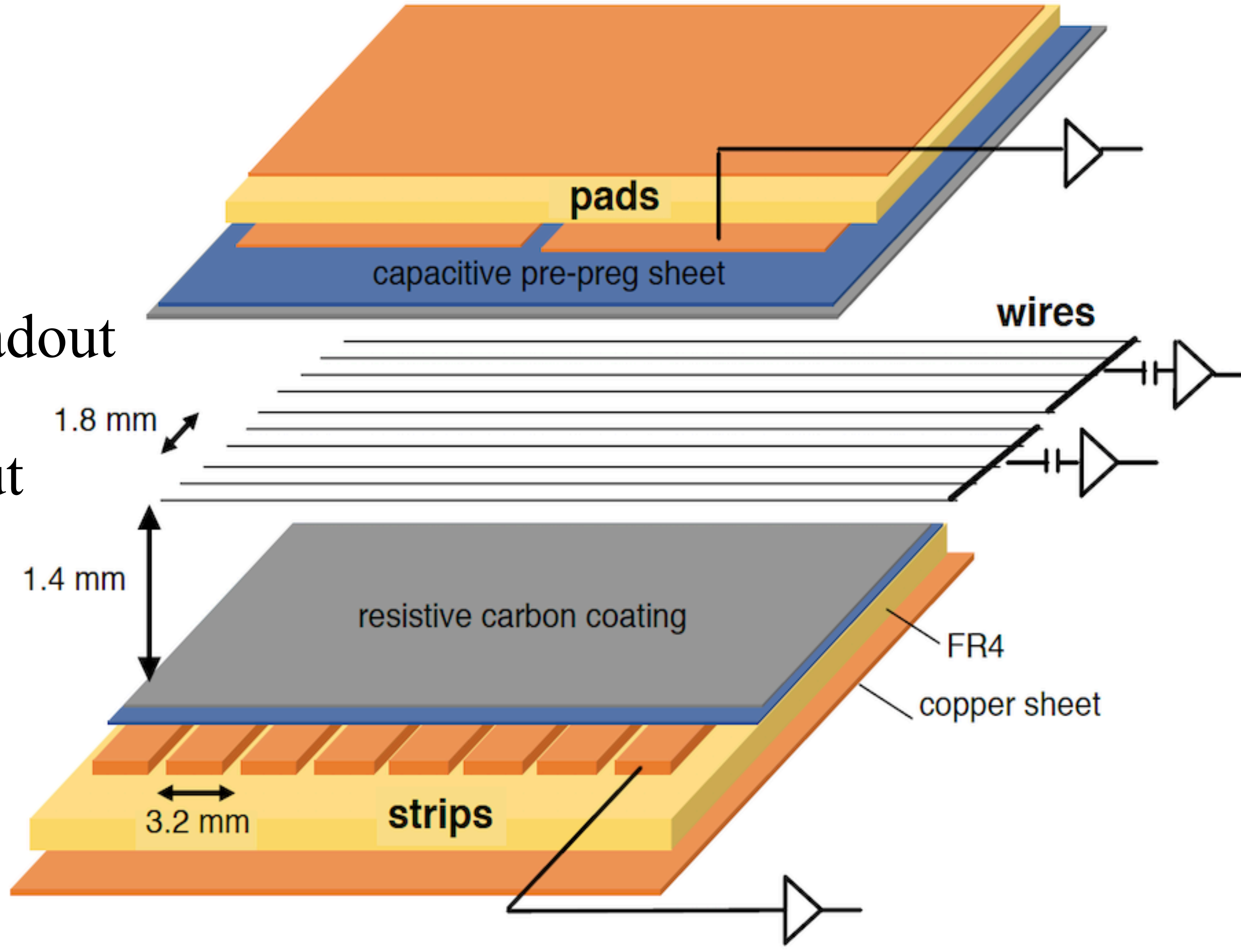
A Small-Strip Thin Gap Chamber (sTGC) is a multiwire proportional chamber operated in quasi-saturated mode. It is made up of 2 segmented cathodes and one plane of anode wires.

The sTGC chambers are operated with a gas mixture of CO_2 and npentane vapour and at a voltage of 2.8 kV. Ionization products induce current on wires, pads and strips as **three readout channels:**

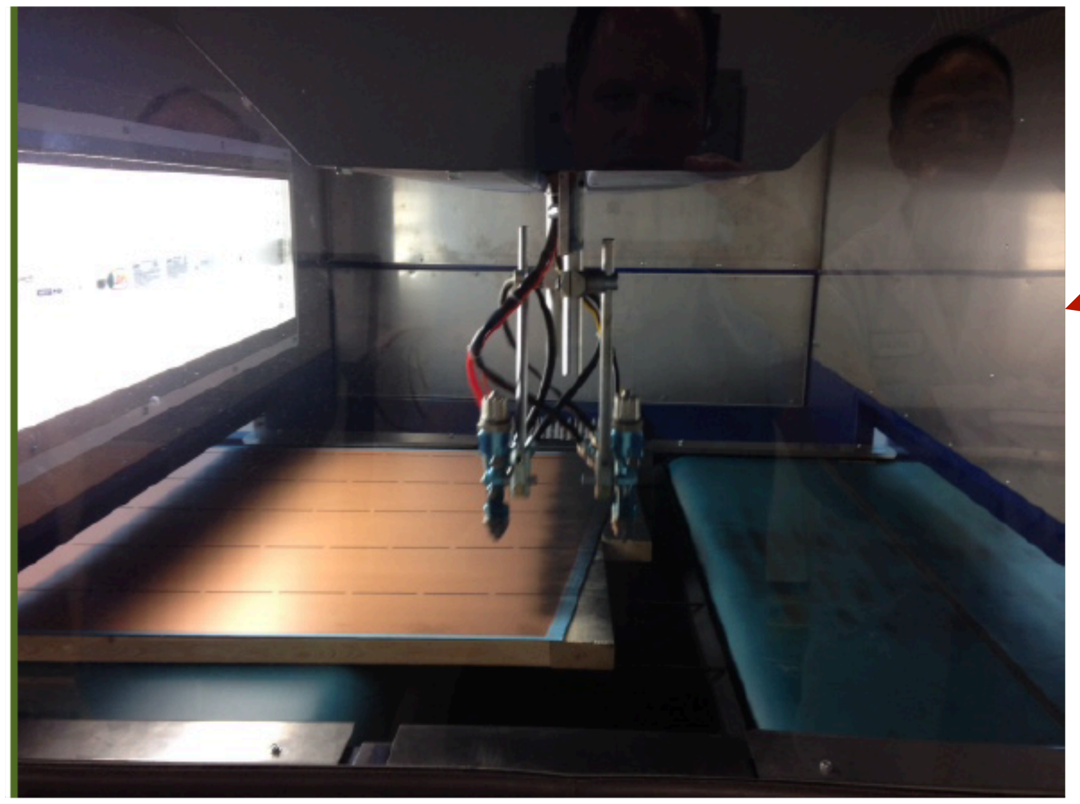
Wires: Coarse azimuthal muon coordinate

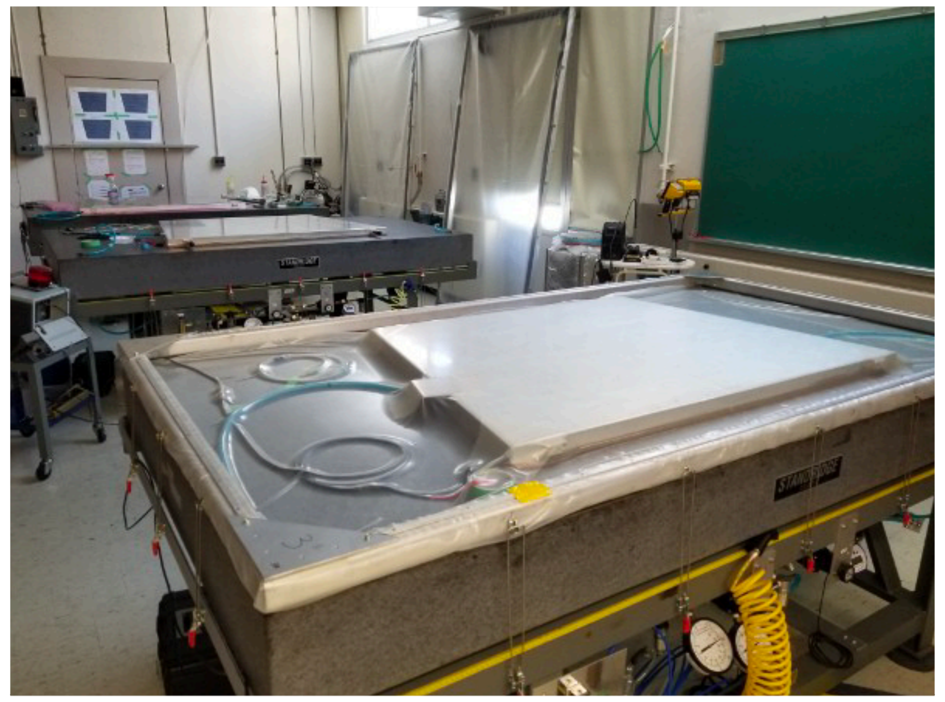
Strips: Precision muon track reconstruction and 1mrad angular resolution; analog readout

Pads: Define NSW trigger region of interest(ROI) and coarse tracking; digital readout



sTGC Construction





Graphite spraying

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Half-gap production

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Wire winding of cathode boards

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Gap closing and testing

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Doublet assembling and testing

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Quadruplet assembling

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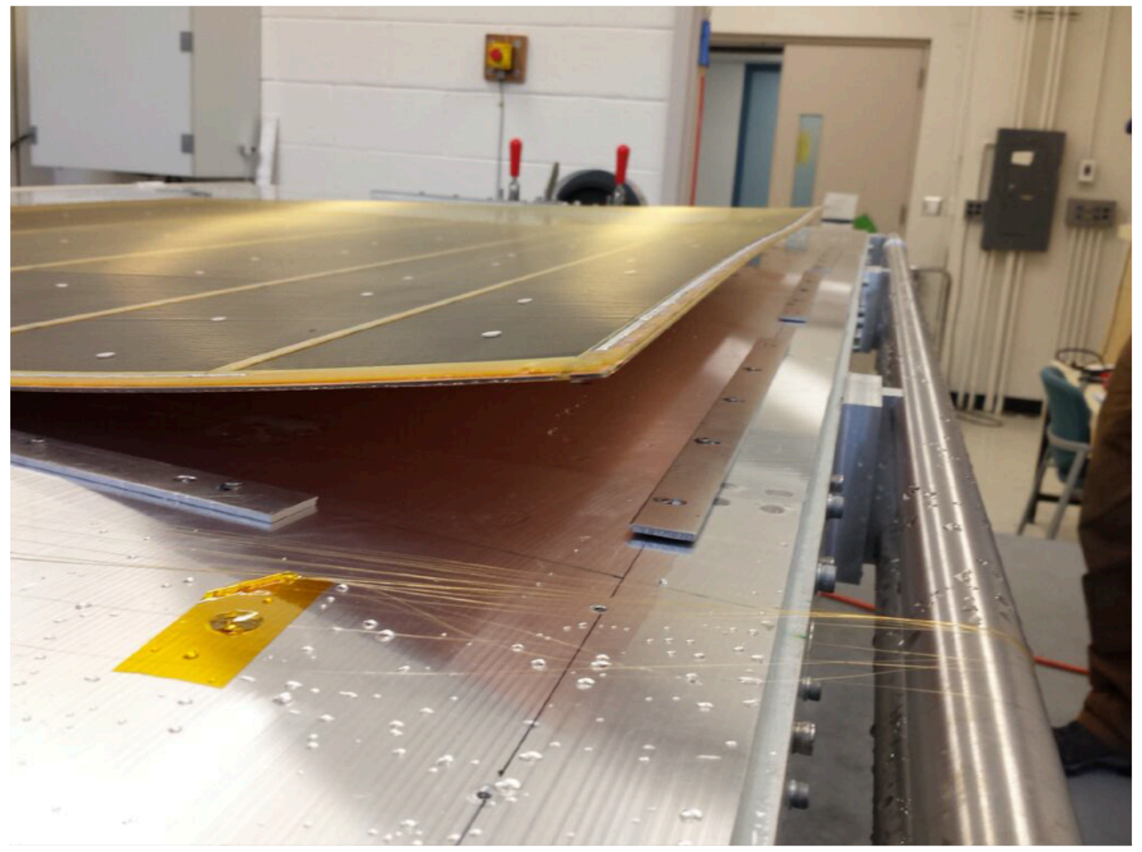
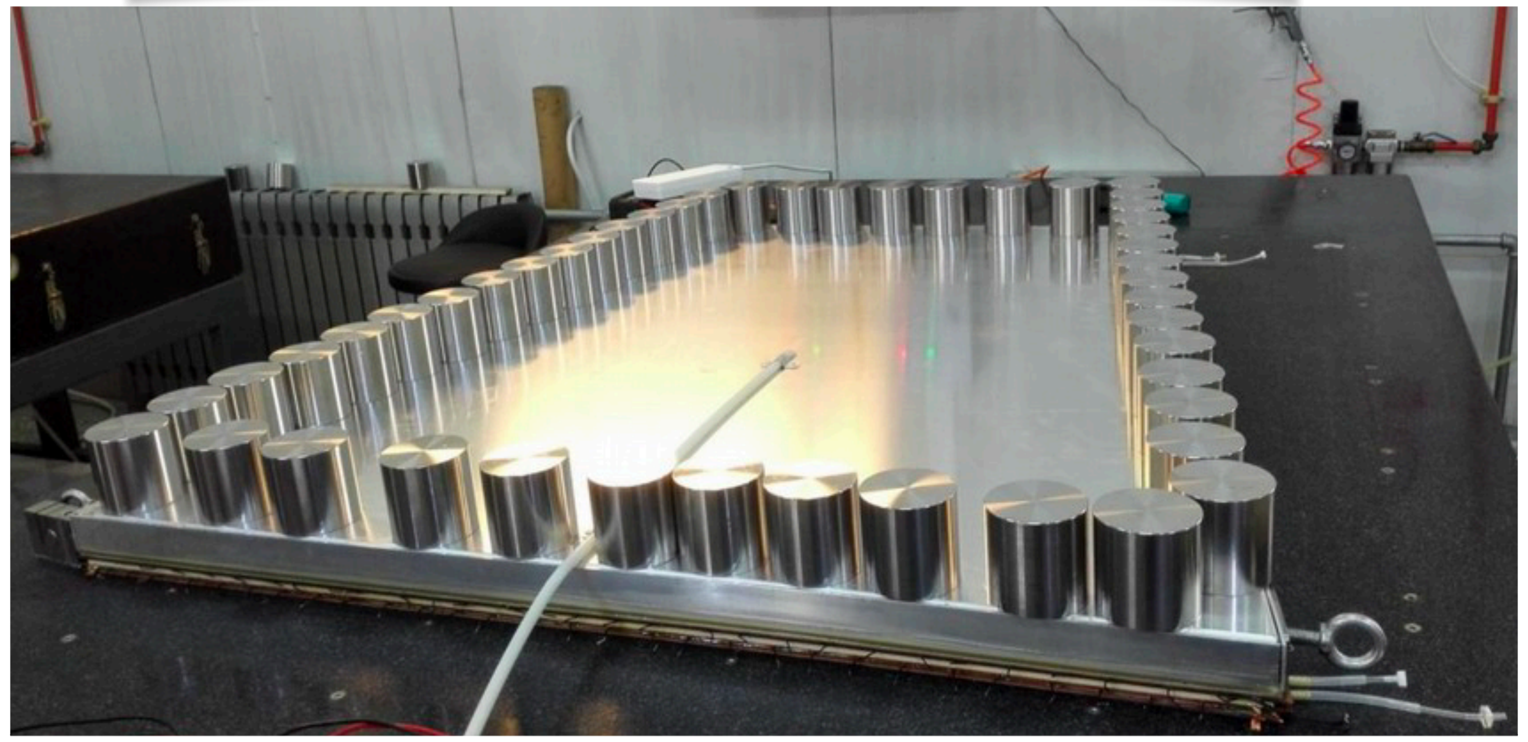
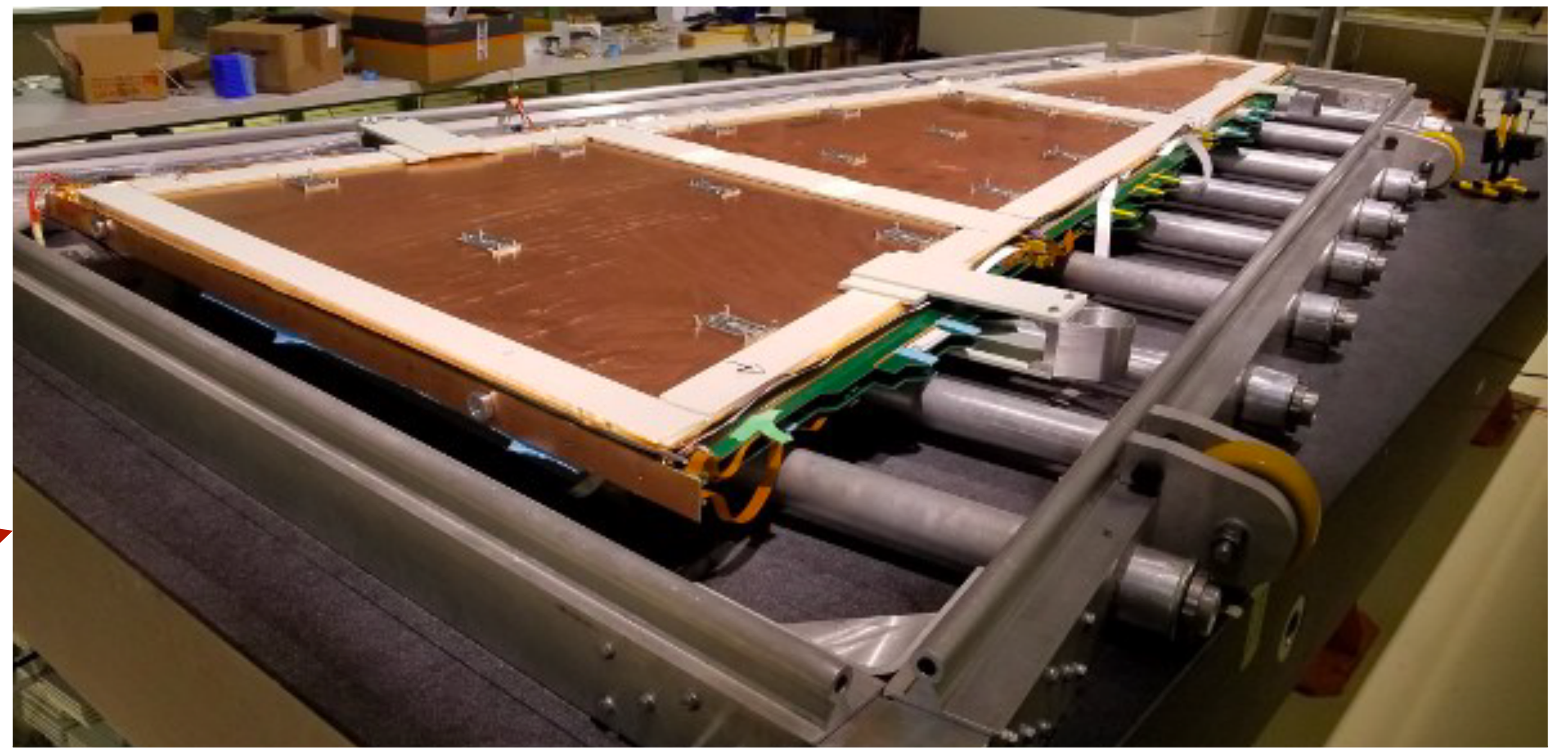
Cosmic-ray testing

↓

Wedge assembly

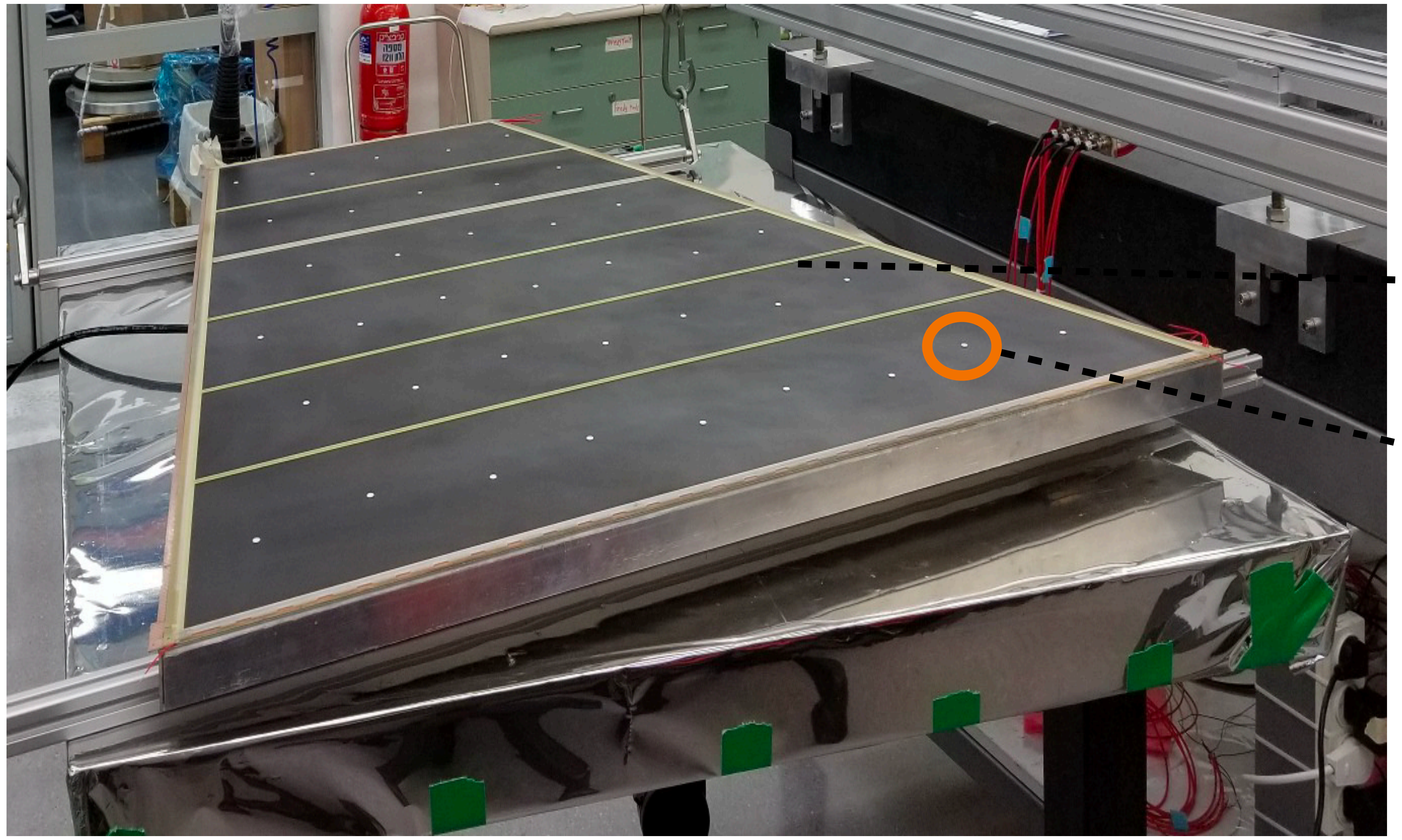


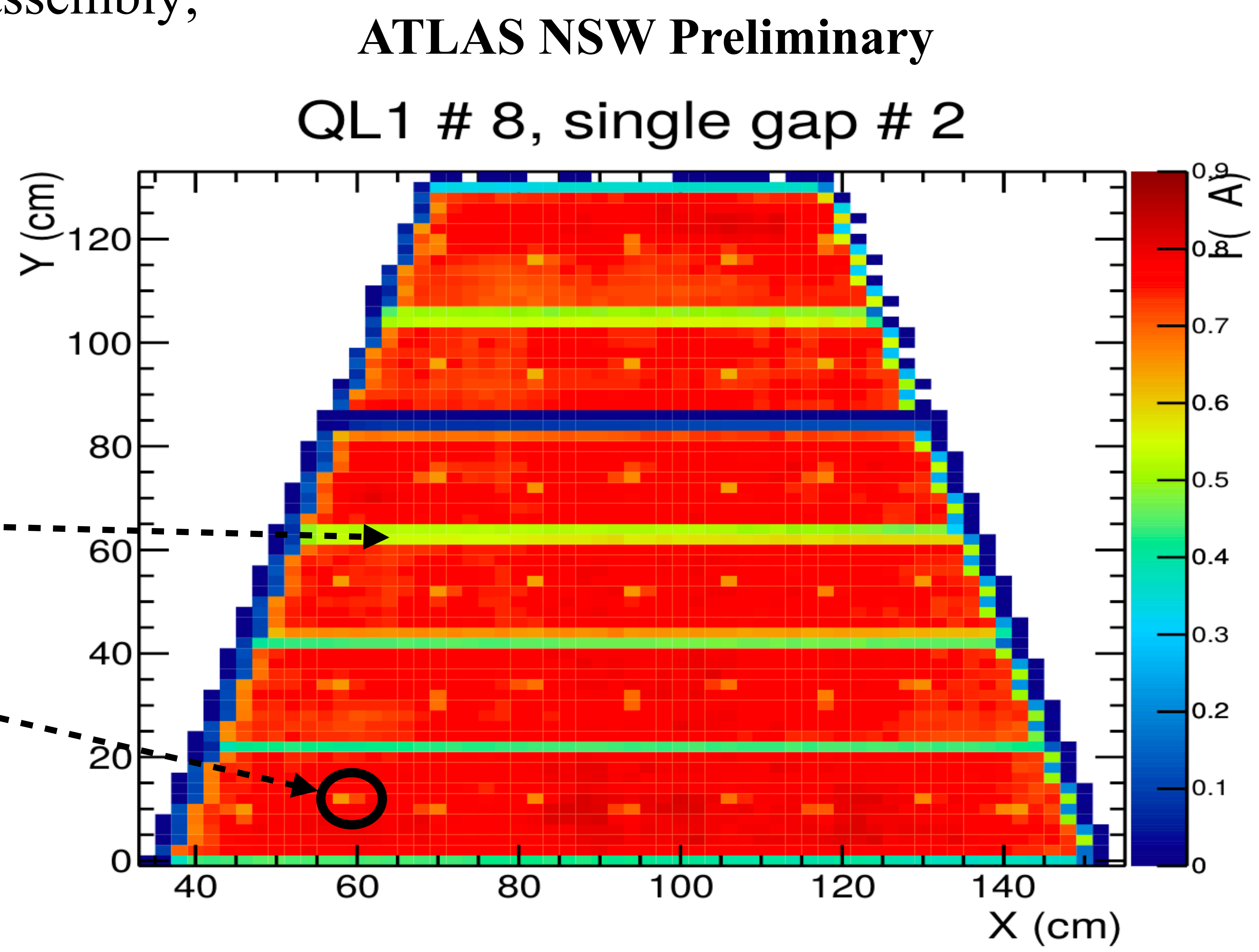




sTGC Quality Tests @ Construction Sites

- HV tests at different stages (single gap, doublet, quad) to identify leakage currents, shorts, sparks;
- X-Ray scan of single gap to measure gain uniformity and probe internal structure of gaps;
- Electrical connectivity test of readout channels after adapter board assembly;

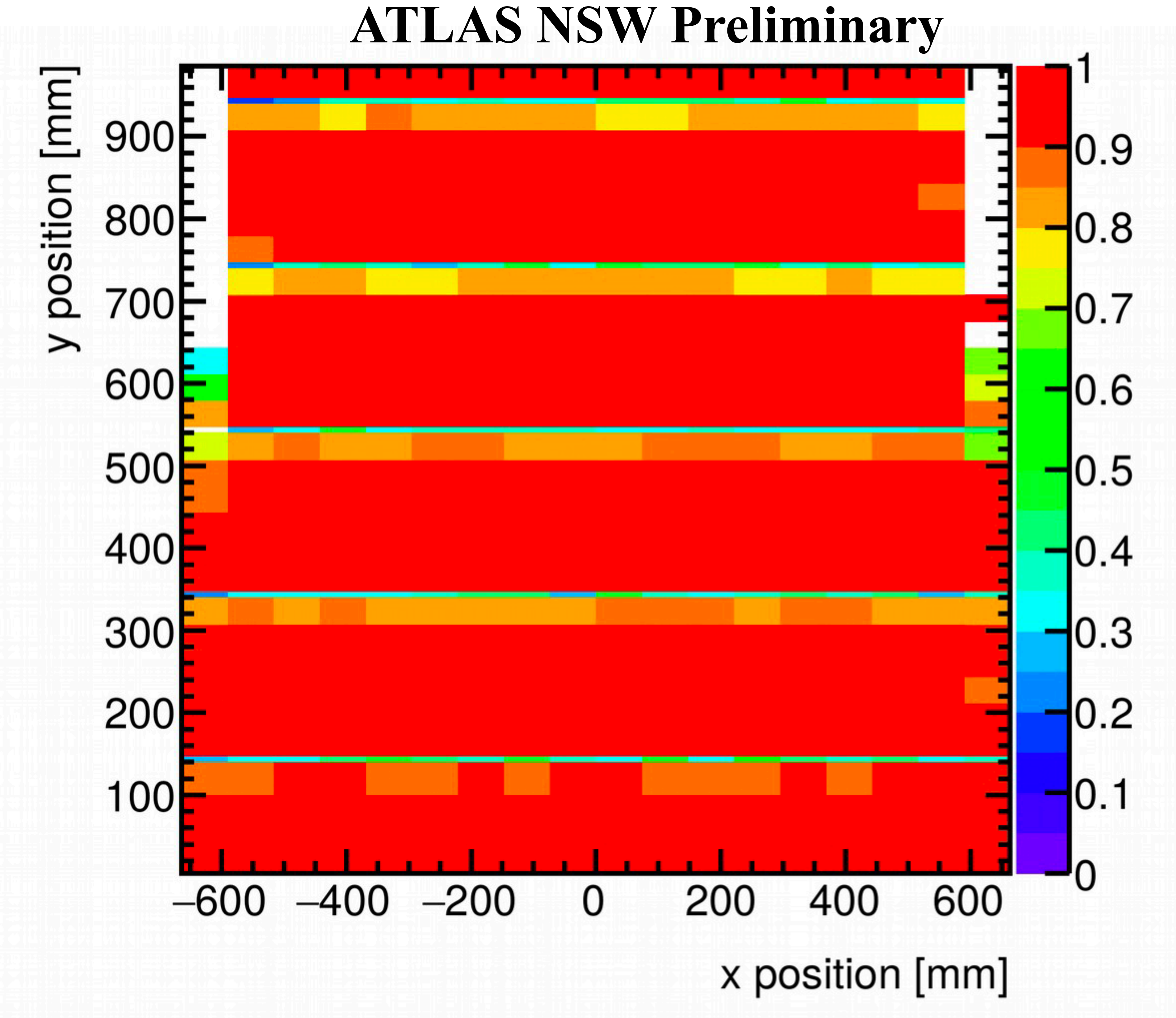




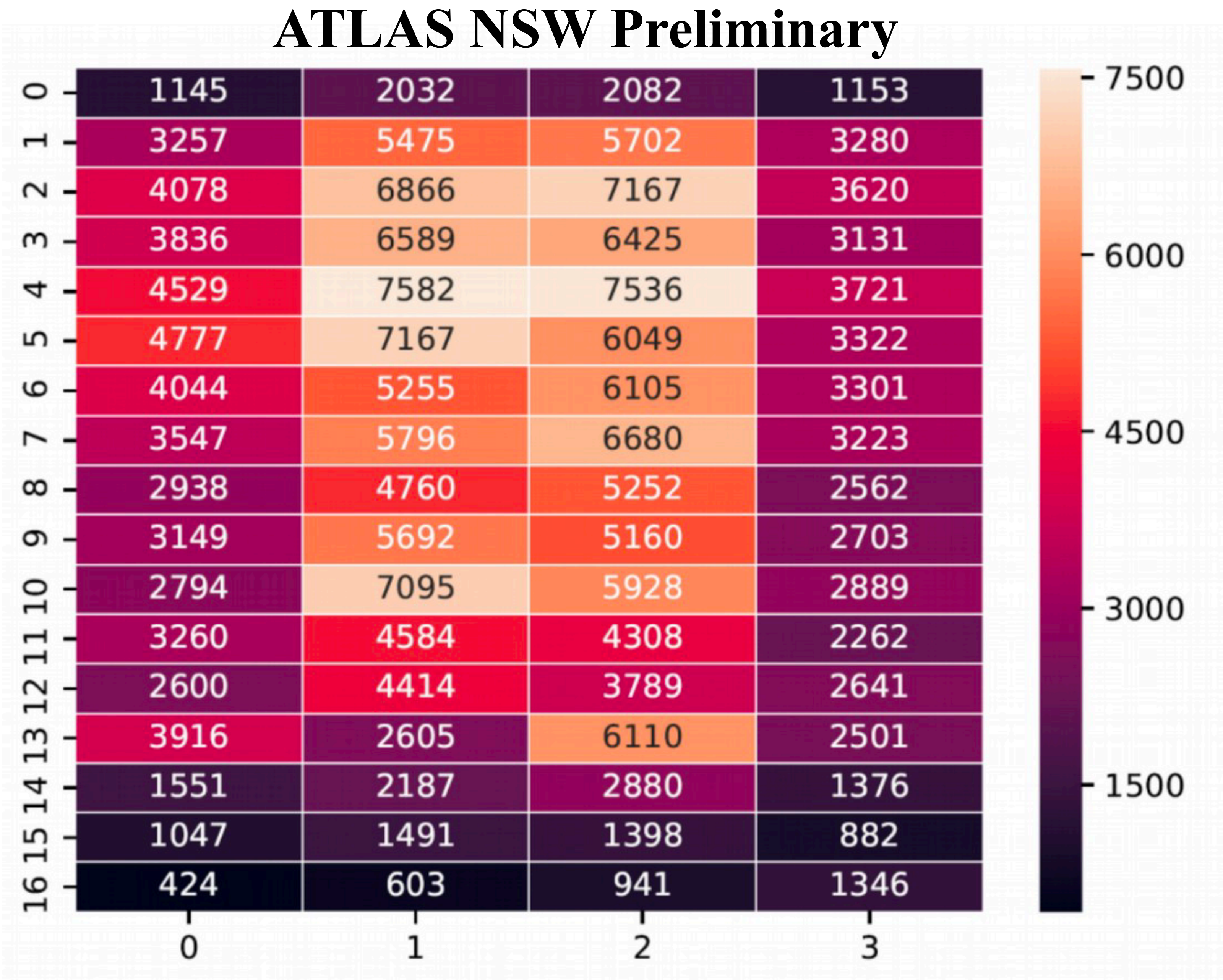
sTGC Cosmic Tests

Tests are conducted to check:

- Hit maps
- 2D efficiency maps
- Resolution and misalignment corrections
- Noise measurement



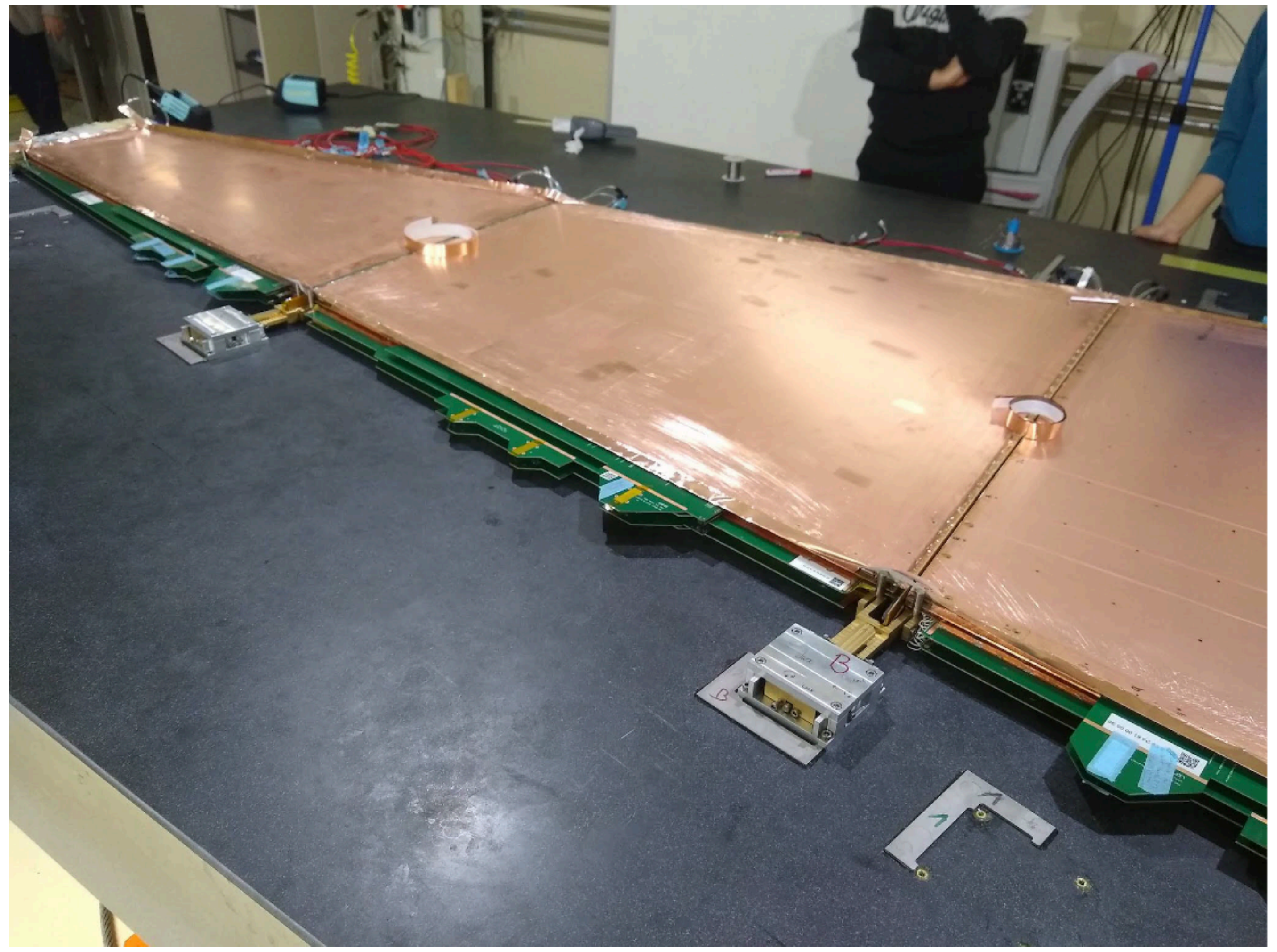
Preliminary 2D efficiency of strip channels of a QS3 gap



Number of cosmic muons counted in a QS1 gap during a period of approximately 13 hours.

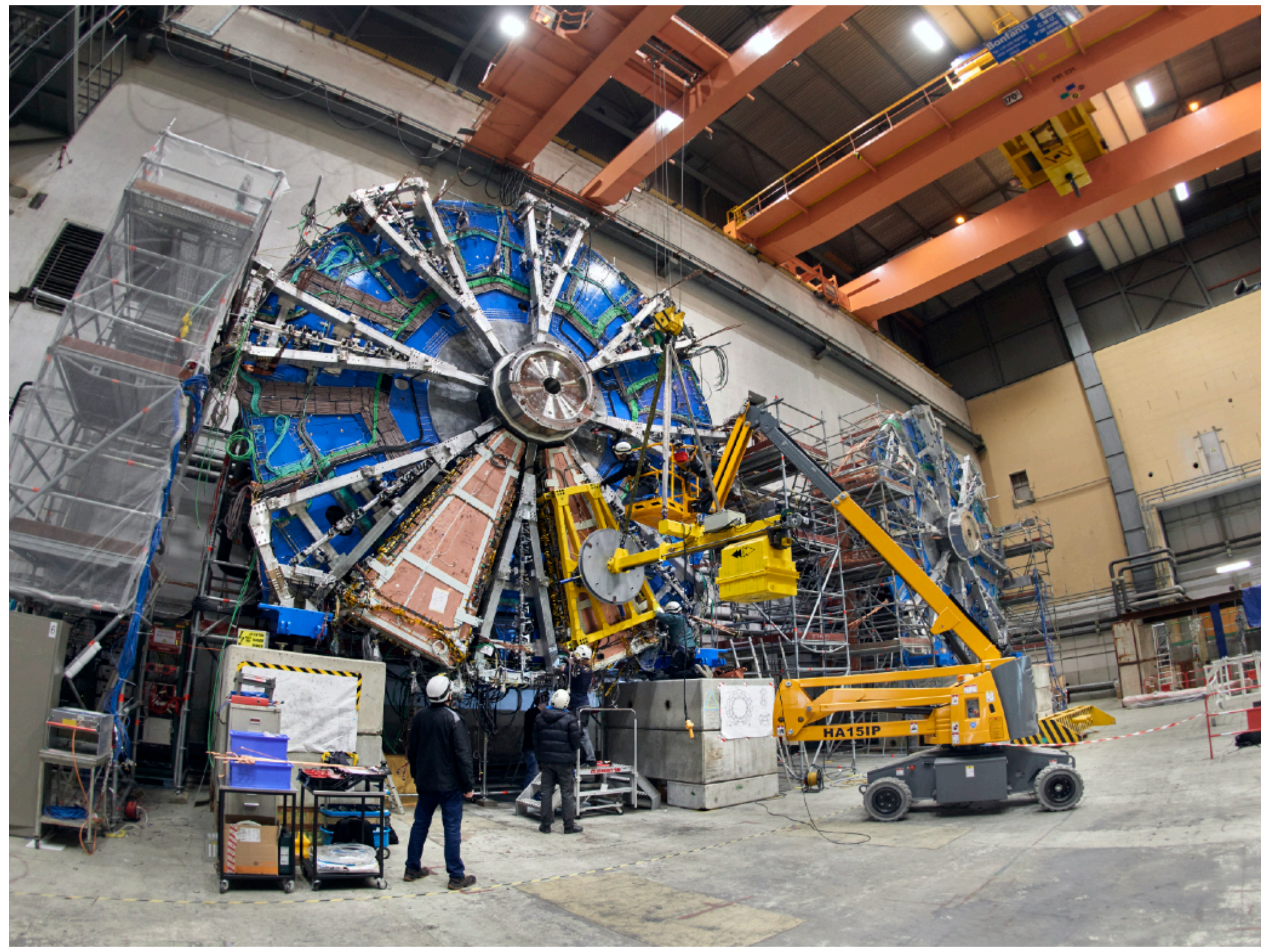
Wedge Assembly and Integration @ CERN

Gluing: 3 quads are assembled into wedges



Faraday cage assembly

Install the electronics and sector integration(sTGC and MM)



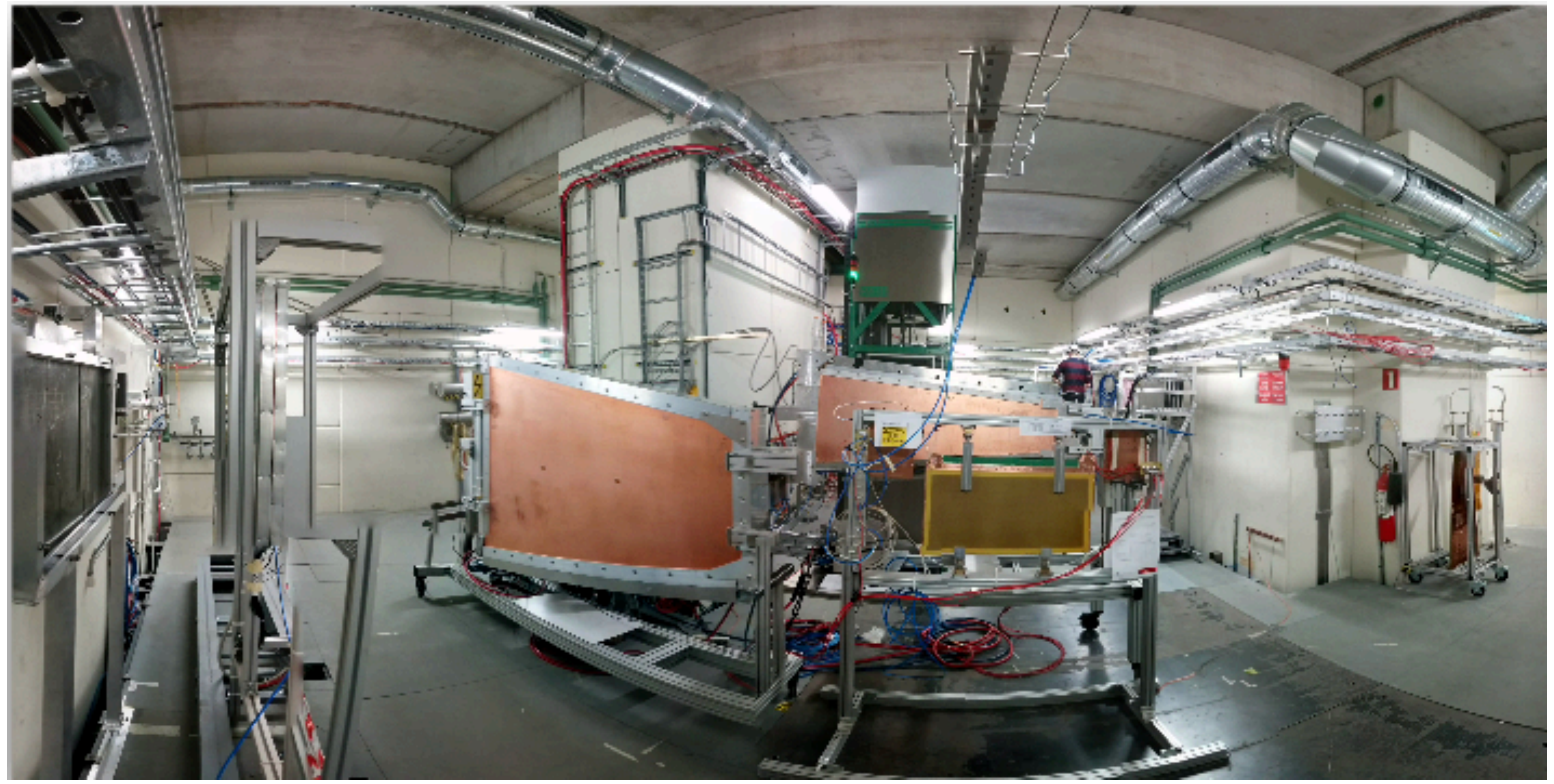
Integrate sTGC and MM into sectors and wheel assembly

Quality Controls @ CERN

Quality control carried out at every step of assembly:

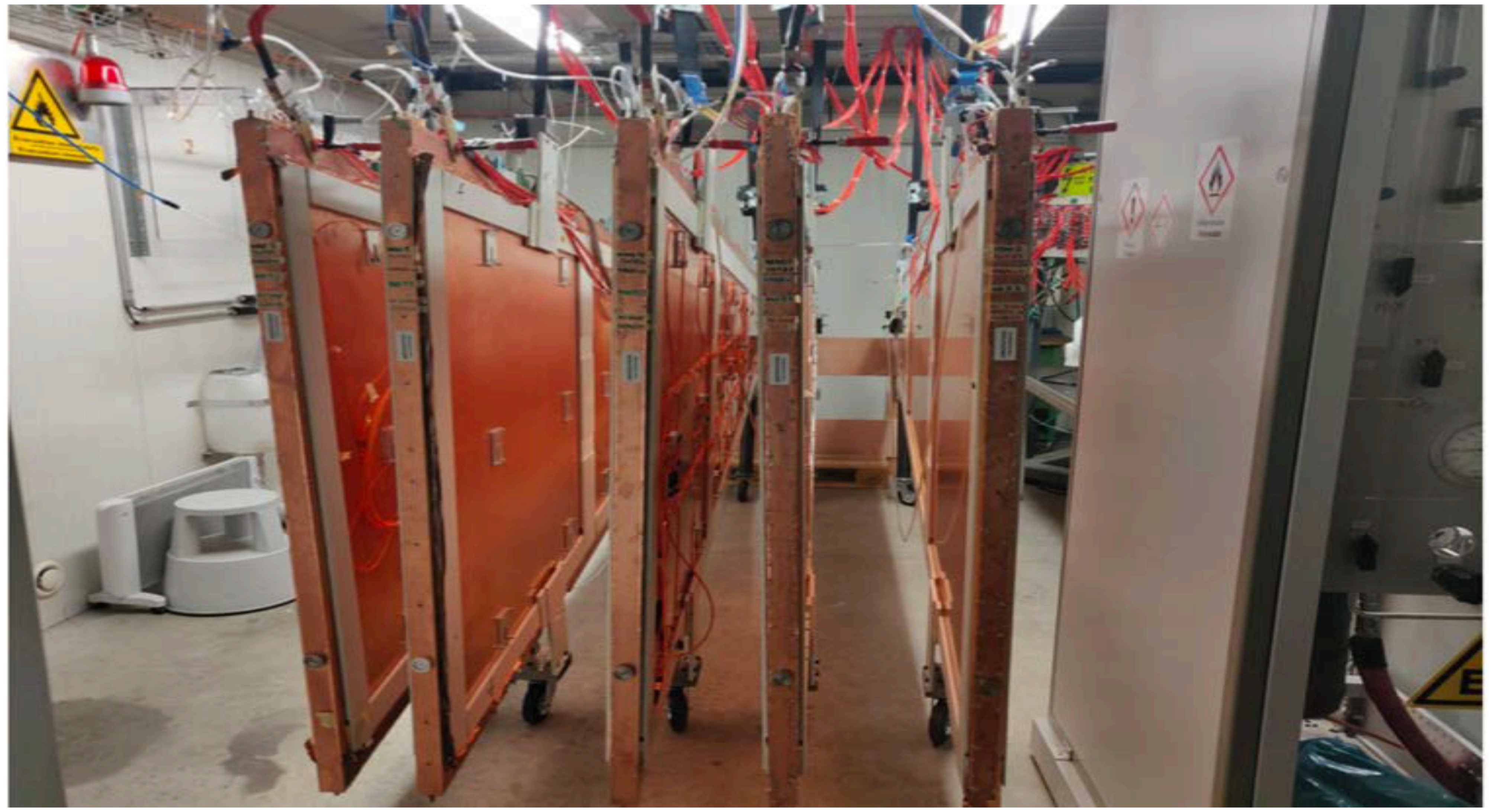
- Ensure no damage during shipment
- Readout connectivity test
- Stability test under high radiation with 20 kHz/cm² (at CERN; GIF++ facility)
- Noise measurements with integrated electronics(wedges)
- Long-term HV test(wedges)
- Measurement of misalignment using x-rays (wedges)

CERN GIF++ facility



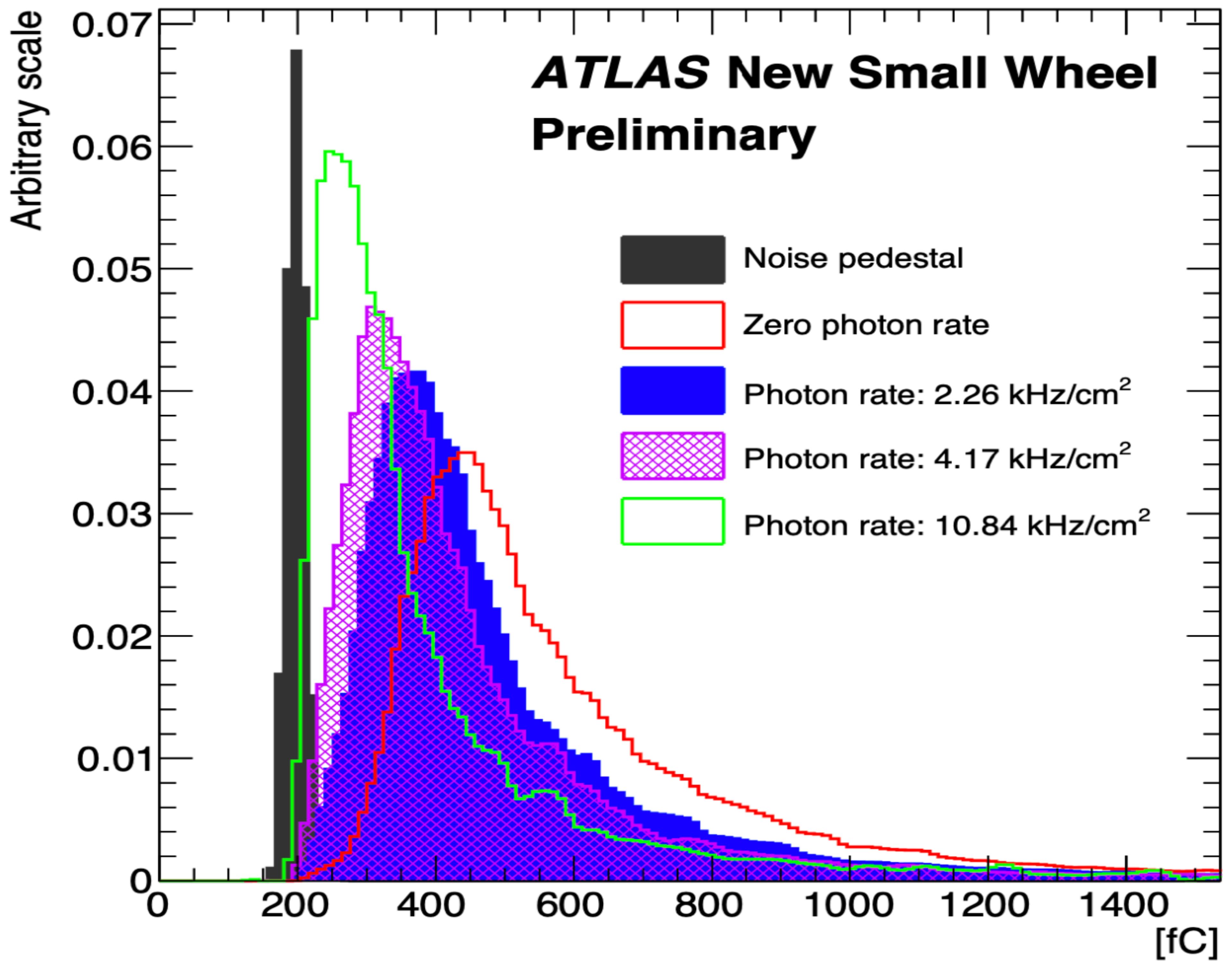
GIF++ operates with 137Cs source of 14 TBq that radiates gamma rays.

HV test @ CERN

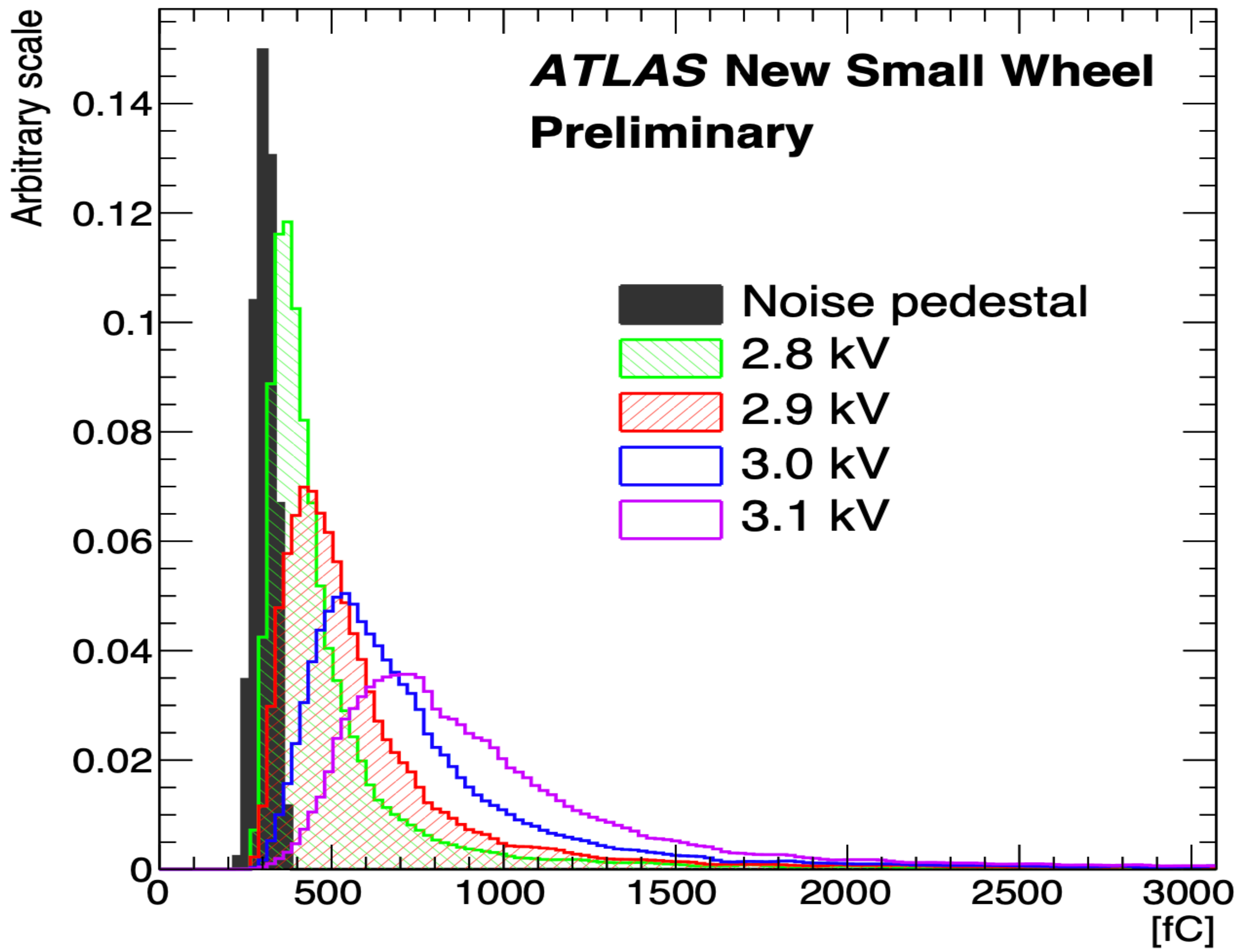


sTGC Performance in Muon Test Beam at CERN

Test with muon beam in the presence of high rate photon background;
CERN GIF++ facility with QL1



Test with muon beam
CERN H8 beam line with QS3

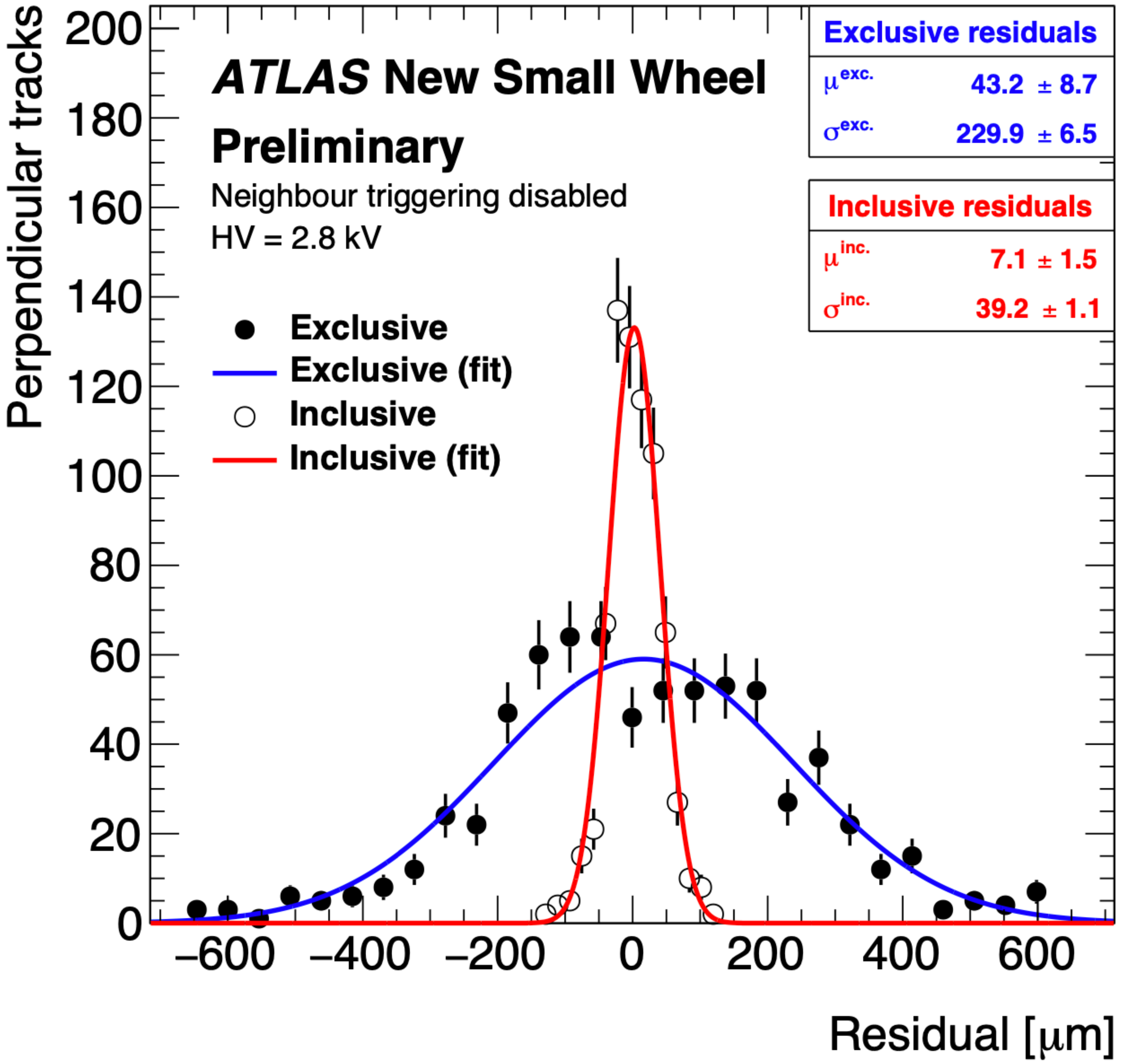


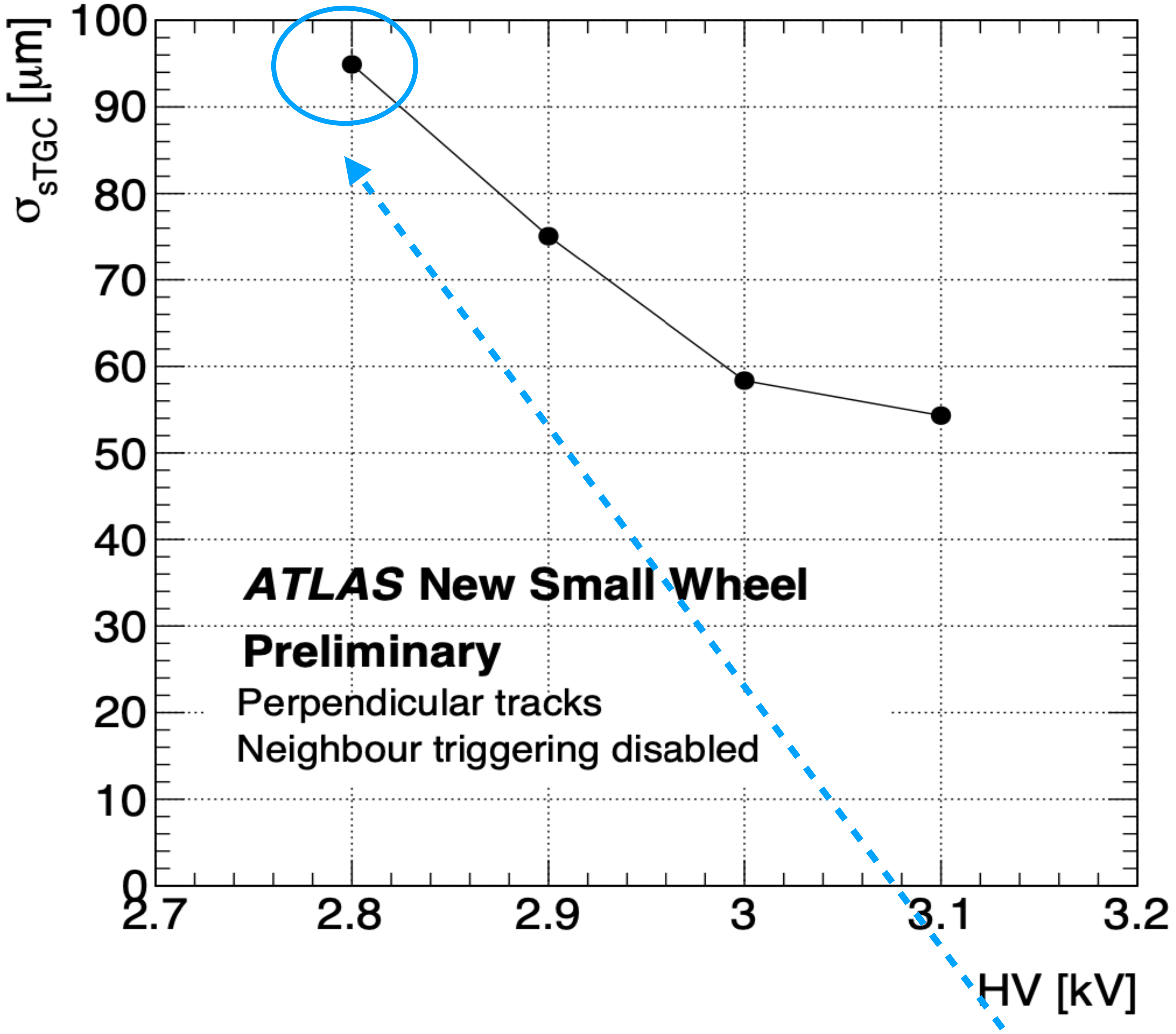
- NSW detectors read out using the VMM amplifier-shaper-discriminator ASIC
- VMM on custom front-end-boards (FEB) designed for sTGC readout

sTGC Spatial Resolution, Test Beam at CERN

Carleton UNIVERSITY | ATLAS EXPERIMENT

sTGC strip spatial resolution as a function of the applied high voltage; measured with final VMM prototype.





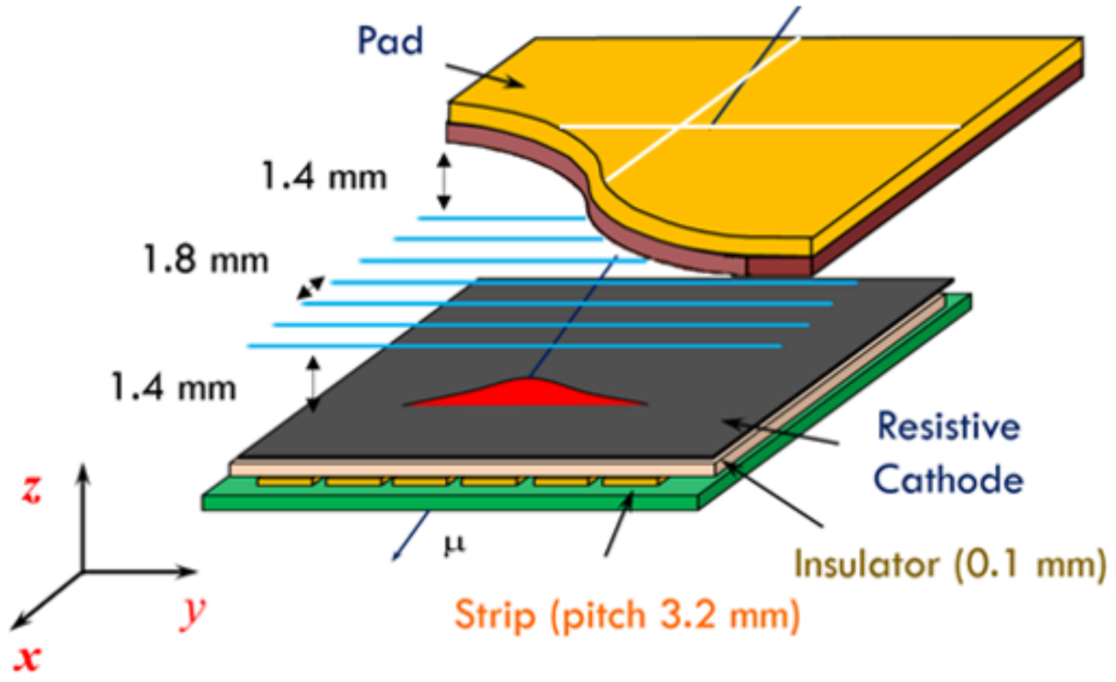
The strip spatial resolution is obtained from the distributions of the exclusive and inclusive residuals of the reconstructed tracks.

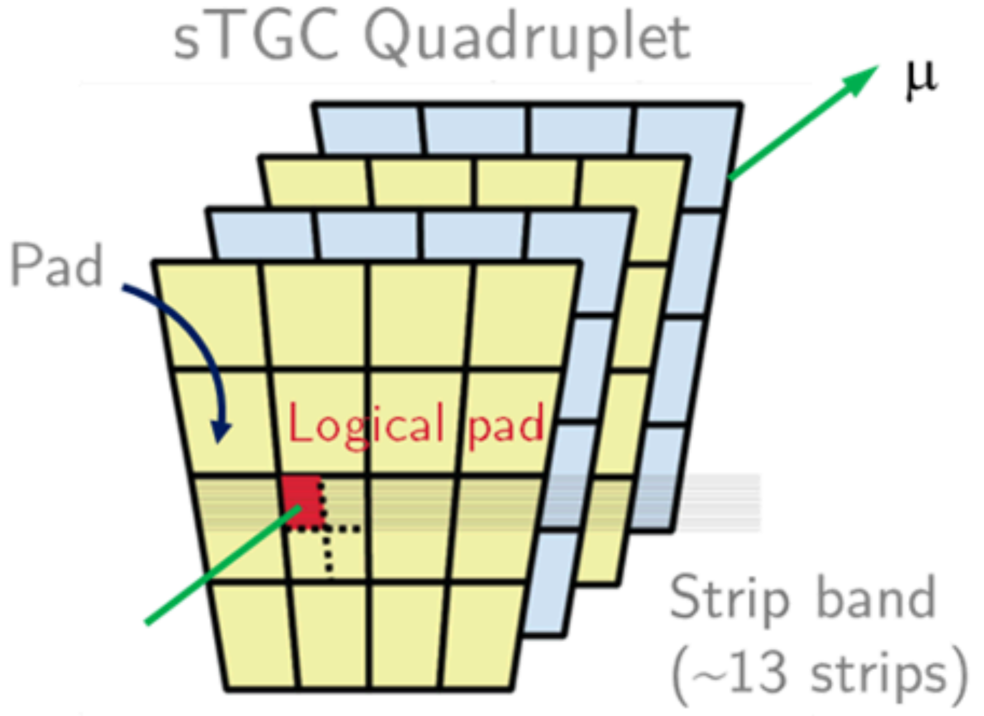
$$\sigma_{sTGC} = \sqrt{\sigma^{inc.} \times \sigma^{exc.}} = 95\mu m$$

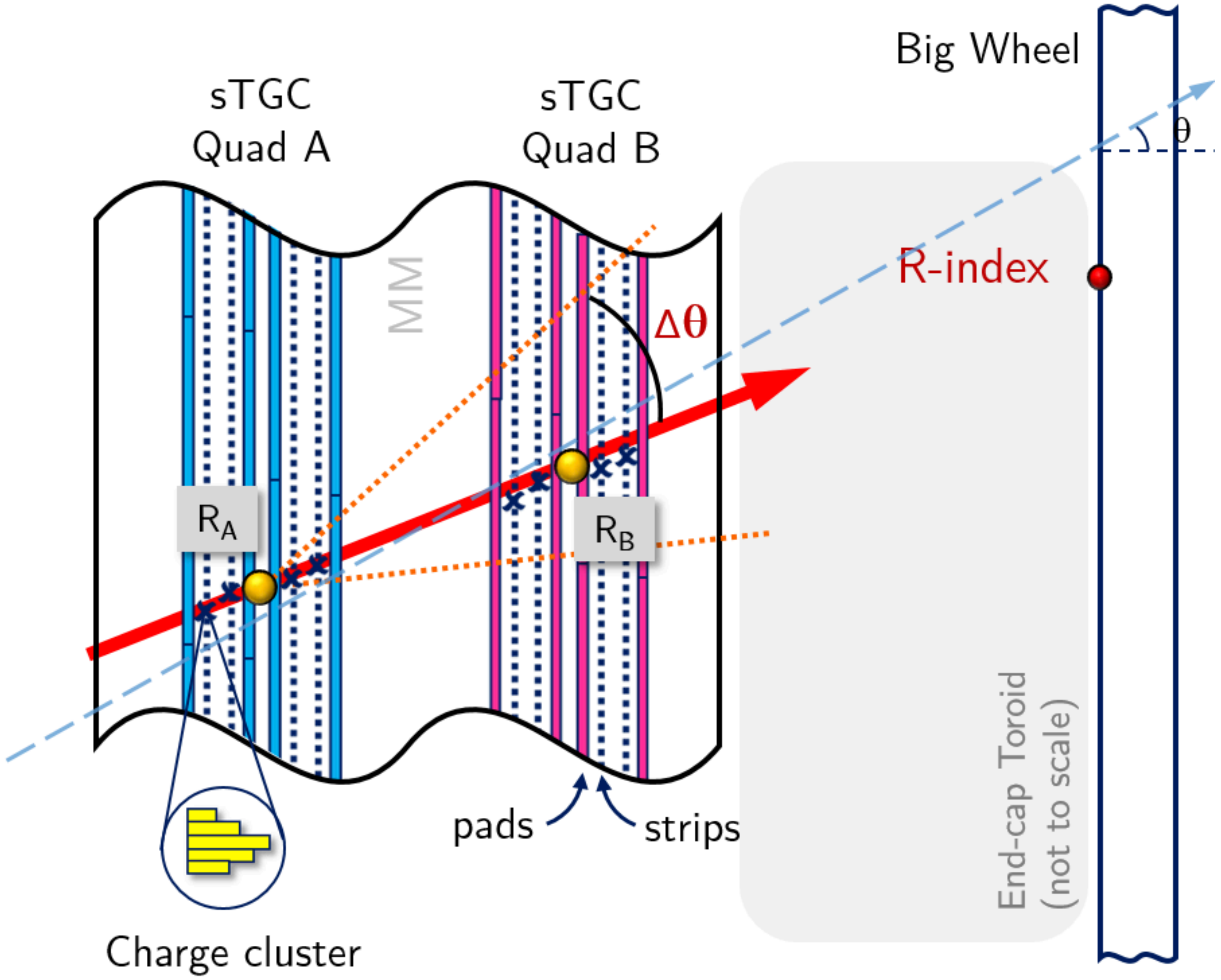
Inclusive residuals for a layer of interest are defined as the position difference between the layer space point and the position of a track reconstructed using the space points of all 3 layers. The **exclusive residuals** are obtained the same way but reconstructing the track without the space point of the layer of interest.

sTGC Trigger

- Pad layers staggered to make "logical' pad towers
- Muon trajectories define pad trigger towers
- 3 out of 4 layers with a hit required for single wedge trigger
- Final decision based on geometrical matching between the two wedge triggers
- Strips from both sTGC wedges and MM hits used for online track angle measurement





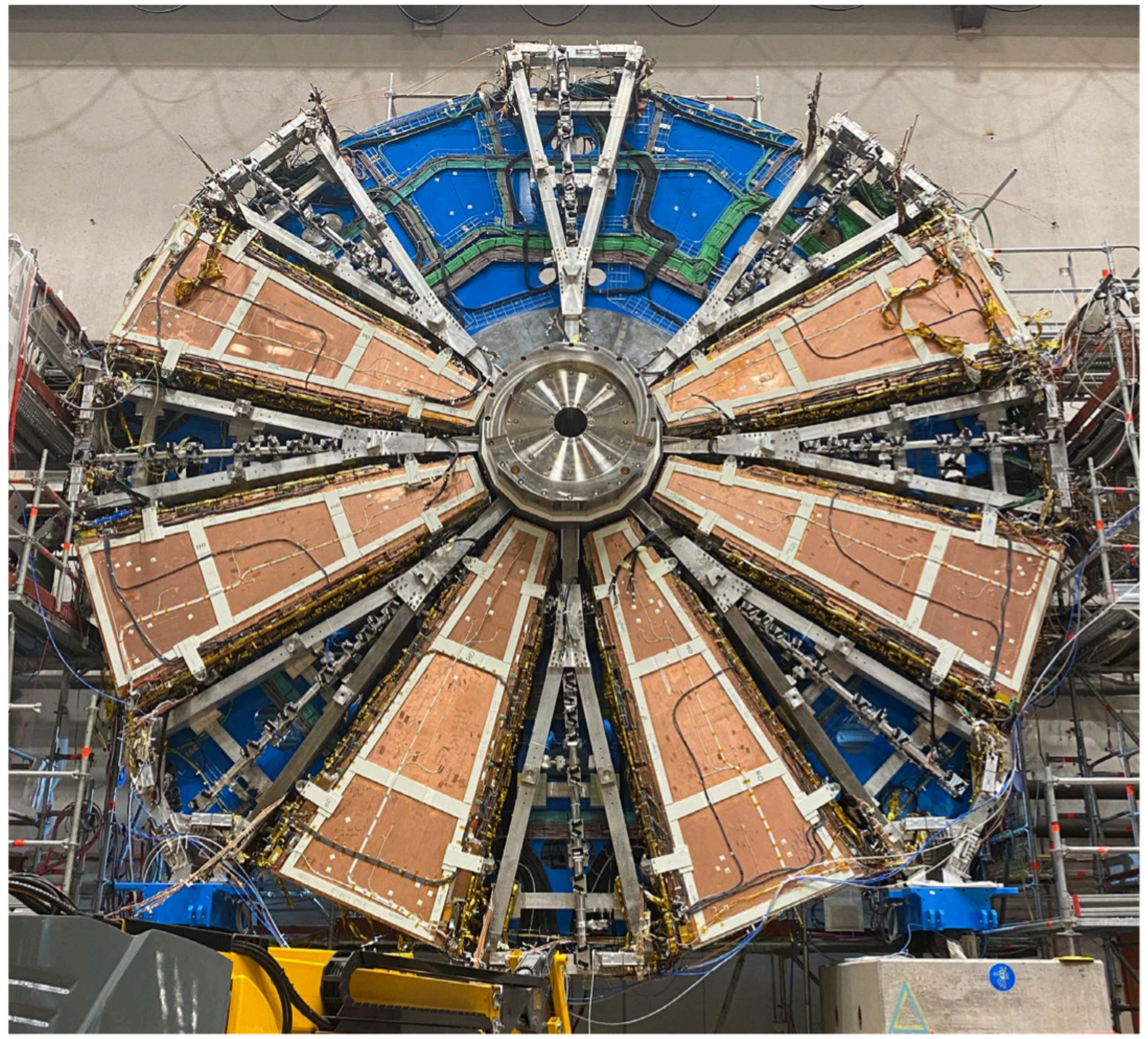


ILC SLIDES

Summary

- The NSW is essential for ATLAS to maintain high trigger efficiency and momentum resolution in the high pile-up and high radiation environment expected during high luminosity phase of the HL-LHC.
- The installation of front-end electronics on the wedges is going well.
- Test beam and irradiation tests are done for the NSW electronics.
- Electronics performance is in really good shape.
- sTGC quadruplet production is underway at all construction sites.
  - It is complete for side A and well under way for side C.
- Integration at CERN is progressing with chambers and electronics

THANKS FOR THE ATTENTION



NSW-A with 6 small sectors installed

ILC:

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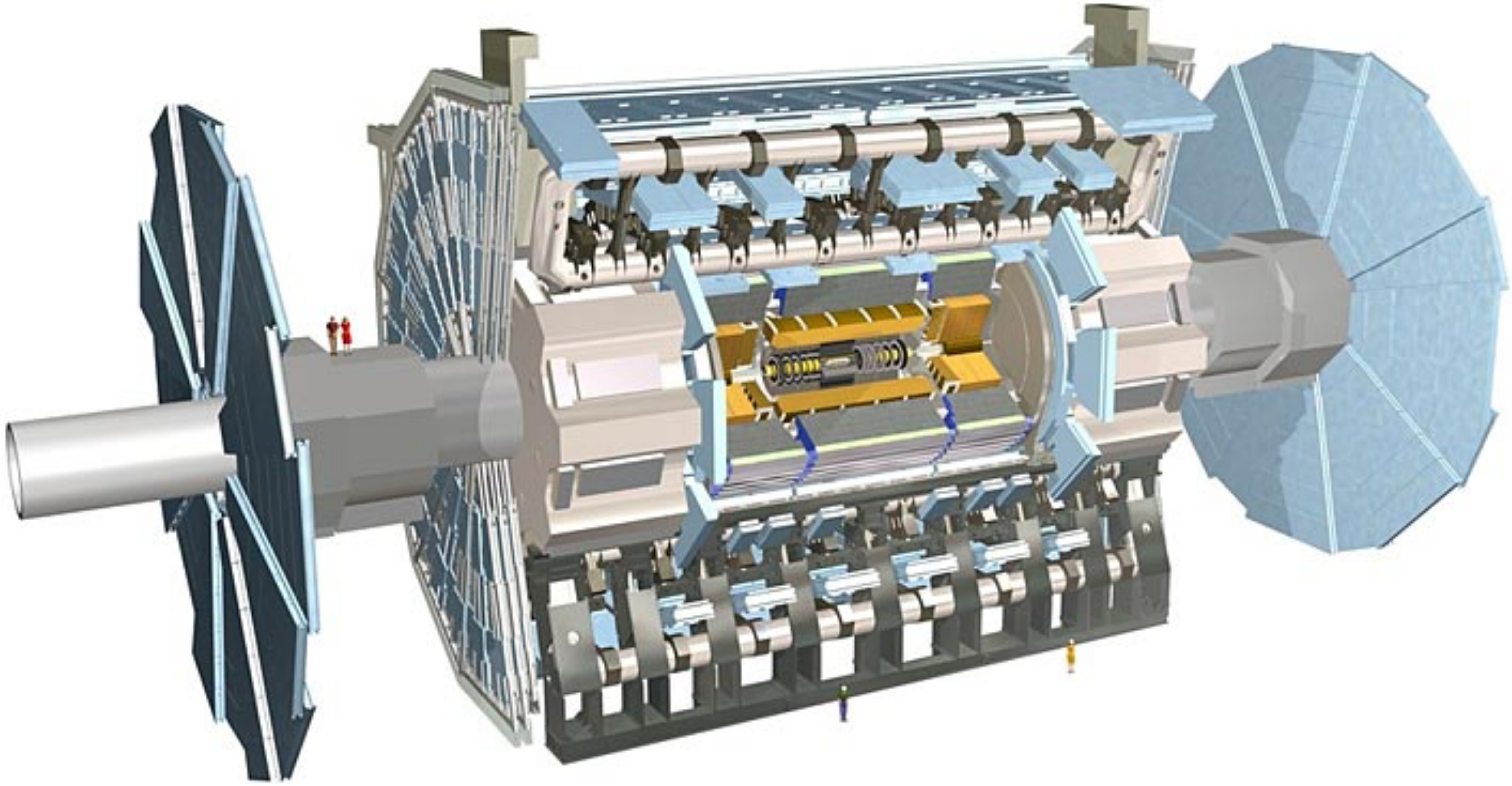
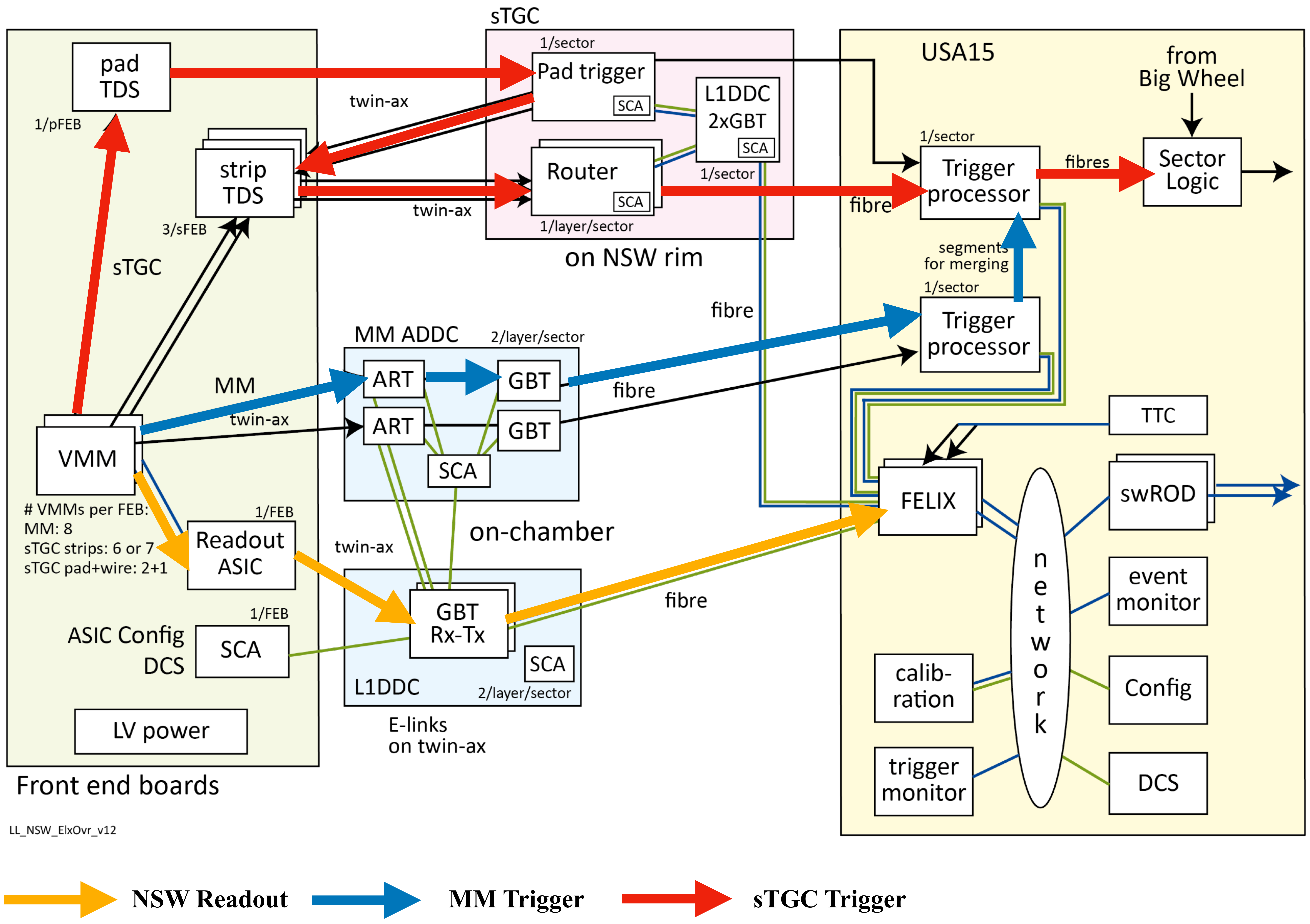
Thank you for listening!

Back-up Slides



NSW Electronics & DAQ Data Flow



Latency from IP to SL limited to 1075 ns

PCBs:
pFEB/sFEB(sTGCpad/strip front-end board)
MMFE8(Micromegasfront-end board)
L1DDC(Level-1 Data Drive Card)
Pad Trigger
Router
ADDC
FELIX(Front-End LInkeXchange)
Trigger Processor

Radiation tolerant ASICs:
VMM (amplifier, shaper, digitizer)
Readout ASIC
Trigger Data Serialiser(TDS)
Address Real Time (ART)
Slow Control Adapter (SCA)
GigaBitTransceiver (GBTX)

sTGC Performance