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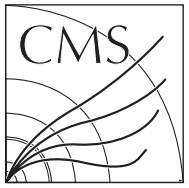

The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

07 January 2021 (v3, 24 February 2021)

The TOFHIR2 readout ASIC of the CMS Barrel MIP Timing Detector

Joao Varela for the TOFHIR2 team

Abstract

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Presented at *IEEE-NSSMIC2020 2020 IEEE Nuclear Science Symposium (NSS) and Medical Imaging (MIC) Conference*

TOFHIR2: The readout ASIC of the CMS Barrel MIP Timing Detector

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***Abstract*– The CMS Detector will be upgraded for the HL-LHC to include a MIP Timing Detector (MTD). The MTD will consist of barrel and endcap timing layers, BTL and ETL respectively, providing precision timing of charged particles. The BTL sensors are based on LYSO:Ce scintillation crystals coupled to SiPMs with TOFHIR2 ASICs for the front-end readout. A resolution of 30-40 ps for MIP signals at a rate of 2.5 Mhit/s per channel is expected at the beginning of HL-LHC operation. We present an overview of the TOFHIR2 requirements and design, simulation results and the first measurements with TOFHIR2A silicon samples.**

I. Introduction

The Phase II Upgrade Program of the CMS experiment at CERN's Large Hadron Collider includes the construction of a new MIP Timing Detector to measure the time of charged particles with high precision [1]. This detector will provide timing of charged particles with high precision allowing to extend to the time domain the association of charged particles to the ~200 concurrent proton collision vertices occurring at each bunch crossing in the High-Luminosity LHC (HL-LHC).

To accomplish this objective a timing layer will be added in front of the CMS calorimeters [2]. In the barrel section, the Barrel Timing Layer (BTL) is a thin standalone detector based on LYSO:Ce crystals read-out with silicon photomultipliers (SiPMs). With an internal radius of 114.8 cm and an outer radius of 118.8 cm, the BTL has a length of 496 cm covering the pseudorapidity region up to $|\eta|=1.48$ with a total active surface of about 38m^2. The individual cell consists of a crystal bar associated to two SiPMs in both ends. The full BTL detector has about 330 thousand SiPM channels.

Dedicated ASIC electronics will be used to readout the SiPM arrays. The readout solution uses the new TOFHIR2 chip. The main requirements for the BTL electronics are: (1) to measure the timing of minimum ionizing particles (MIP) with a precision of 30 (60) ps at the beginning (end) of HL-LHC; (2) and to provide a measurement of the signal amplitude with <5% precision for time-walk corrections. Additionally, the chip has to cope with a MIP input rate of 2.5 M hit/s corresponding to the expected maximum channel occupancy of 7% and to have an output bandwidth of 640 Mb/s. Last but not least, the chip should have a static power consumption lower than 15 mW per channel.

A first version of the chip (TOFHIR1) was implemented in technology CMOS 110nm of the UMC foundry [3]. TOFHIR1 was largely based on the existing TOFPET2 chip [4], allowing the development of detector modules and the validation of system integration within a tight schedule. TOFHIR2 is a completely new chip developed in technology CMOS 130nm of the TSMC foundry. This technology has an improved behavior under radiation (small V_{th} shifts and leakage current).

A summary of the TOFHIR specification parameters is given in Table I. In this paper, we present the results of the measurements with TOFHIR2A obtained since July 2020. Fig.1 shows a photograph of the chip as well as its layout. The chip dimensions are 8.5 x 5.2 mm^2. TOFHIR2A is a complete version of the final chip, nevertheless it doesn't implement the final DCR cancellation circuit neither the final SEE protection (see sections V and VII). The final ASIC (TOFHIR2B) is expected to be submitted in April 2021.

Table I – TOFHIR specification parameters.

	TOFHIR1	TOFHIR2
Number of channels	16	32
Technology	CMOS 110nm	CMOS 130 nm
Voltage supply	1.2 V, 2.5 V	1.2 V
Reference voltages	External	Internal
Radiation tolerance	No	Yes
DCR noise filter	No	Yes
Number of analog buffers	4	8
TDC bin (ps)	20	10
10-bit SAR ADC (MHz)	10	40
I/O links	LVDS	CLPS
L1, L0 Trigger	Yes, No	Yes, Yes
Max MIP rate/ch (MHz)	1	2.5
Max low E rate/ch (MHz)	3	5
Clock frequency (MHz)	160	160

Manuscript received November 1, 2020.
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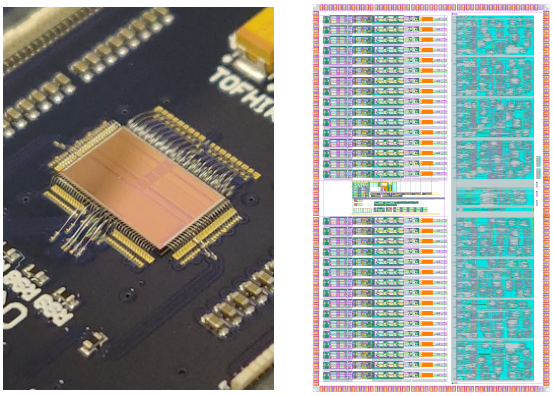


Figure 1 – Photograph of the TOFHIR2A chip (left) and chip layout (right). The chip dimensions are 8.5 x 5.2 mm^2.

II. Requirements and Architecture

The main challenges of the TOFHIR2 ASIC are: (1) to minimize the impact of SiPM dark count noise (DCR) and of pileup of LYSO pulses on the time resolution; (2) to cope with the very high MIP rate of 2.5 MHz and the low energy hit rate of 5 MHz per channel; (3) to handle the variation of dynamic range along the detector lifetime by a factor of 4, within tight power consumption limits.

A block diagram of one TOFHIR2 channel is shown in Fig.2. Each ASIC channel contains one pre-amplifier, two post-amplifiers, three leading edge discriminators, two time-to-amplitude converters (TAC), one charge-to-amplitude converter (QAC), one 40MHz 10-bit SAR ADC and local control logic. The input pre-amplifier provides a low impedance input to the sensor's current signal. The input current is replicated into three branches for timing, energy discrimination and charge integration.

Pulse filtering is included in the post-amplifiers to mitigate the deterioration of time resolution due to the large DCR induced by radiation (up to 50 GHz) and due to pile-up of LYSO pulse tails. The filter creates an inverted and delayed replica of the input current that is added to the original signal. The processing is done in current mode which allows for large bandwidth in a simple implementation. The delay line is implemented as a set of RC nets with programmable taps.

TOFHIR2A has three voltage discriminators per channel. The first discriminator (T1) has very low threshold (~2% of peak amplitude), sensitive to the arrival of the first photo-electrons for timing measurement; the second discriminator (T2) is used to reject low energy hits before arming the TACs; the third discriminator (T3) provides the selection of MIP signals for digitization. In TOFHIR2B, fast current discriminators will be used matching directly the current output of the pulse filters.

In each channel, two TAC arrays and one QAC array are each implemented with eight-fold buffers storing events while waiting for digitization. The two TAC arrays allow for two time measurements of the leading or trailing edges of the discriminator outputs selected by configuration. The TAC integrates a current source in the time interval between the discriminator output and the next leading edge of the clock, providing time interpolation and allowing good time resolution with low power consumption. The QAC integrates the pre-amplifier output current using a configurable integration window. The QAC provides linear pulse amplitude measurement in the full dynamic range. The short conversion time of the SAR ADC allows that a single ADC per channel is used for digitizing the two TACs and the QAC voltage amplitudes.

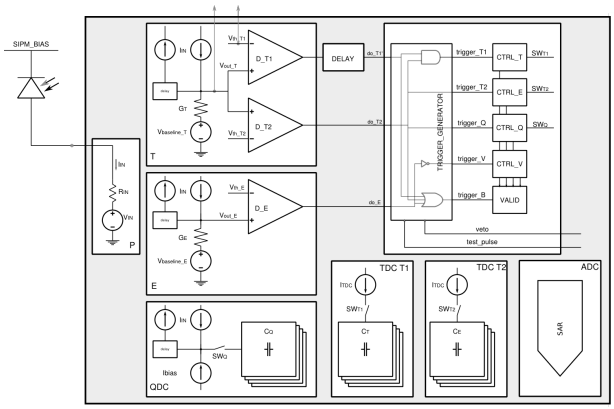


Figure 2 – Block diagram of the TOFHIR2 channel.

A robust and predictable bias current distribution and voltage references were implemented, which is mandatory to ensure uniform and predictable behavior of about 10'000 ASICs in BTL. All voltage and current references are generated internally. The DAC voltages are derived from a common bandgap using a compensation technique. Bias can be calibrated on demand resetting to default values to mitigate PVT variations and radiation. The circuit is robust in the 16 PVT corners. From experience with similar chips, these corners contain the radiation effects observed in tests.

The digital I/O is directly compatible with the CERN's gigabit transceiver lpGBT [5]. Two output data links each running at 320 Mb/s provide the required bandwidth. Three input links at 80 Mb/s are used for configuration, external triggering and synchronization. The clock frequency is 160 MHz. TOFHIR2 includes two 8-bit DACs to adjust the two SiPM bias voltages provided by the ALDO2 chip [6].

III. Simulations

Extensive simulations were performed. As an illustration, Fig.3 shows the SiPM current pulse and the corresponding current pulse at the output of the DCR filter for different settings of the delay line.

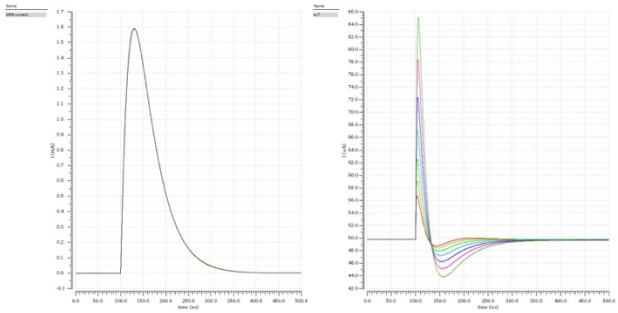


Figure 3 – Pulse shapes at TOFHIR2 input (left) and at the output of the DCR filter for different setting of the delay line between 200ps and 496ps (right).

A simulation of time resolution for End of Life (EoL) conditions was performed assuming MIP pulses with 6000 photoelectrons (p.e.), SiPM dark count rate (DCR) of 55 GHz and SiPM gain of $1.5x10^5$. In Table II we give the expected time resolution (for double readout of a LYSO bar) estimated as the ratio of the DCR noise to the slew rate of the pulse rising edge. We conclude that the time resolution at the output of the SiPM is 180 ps whereas the time resolution at the output of the DCR noise cancellation module the time resolution is 52 ps, which corresponds to an improvement by a factor 3.5.

Table II – Simulation of the time resolution in End of Life conditions obtained at the output of the SiPM and at the output of the DCR noise cancellation module.

	SiPM ouput current	DCR module output current
Slew rate (A/ms)	135.9	9.93
Noise r.m.s (A)	$2.45x10^{-5}$	$5.12x10^{-7}$
σ_{noise}/ SR (ps)	180	52

IV. Experimental Setup

The TOFHIR2A ASIC was assembled in the TOFHIR2 test board. Each board includes two TOFHIR2 chips, one ALDO2 (LV and BV regulator) and SiPM input connectors. Dedicated connectors allow access to probing pads in the TOFHIR2 chip. Access to data via the ASIC I/O digital links was done using the PETsys Readout System [7]. Flexible cables connect the test board to the FPGA board (FEB/D). The readout system allows to read the two TOFHIR2 ASICs. The FEB/D unit provide the ASIC test board with all the necessary power, SiPM bias voltages, configuration and readout.

Measurements were performed using laser pulses generated by the HPK PLP-10 Picosecond Light Pulser. The light pulses were attenuated as necessary with optical filters. A blue LED emulating DCR noise was also used. The SiPM HDR2 from HPK, one of the candidates for use in BTL, was used in the present TOFHIR2A characterization tests. All measurements were done at 20°C. Fig.4 and Fig.5 show pictures of the test setup and of the TOFHIR2 test board, respectively.

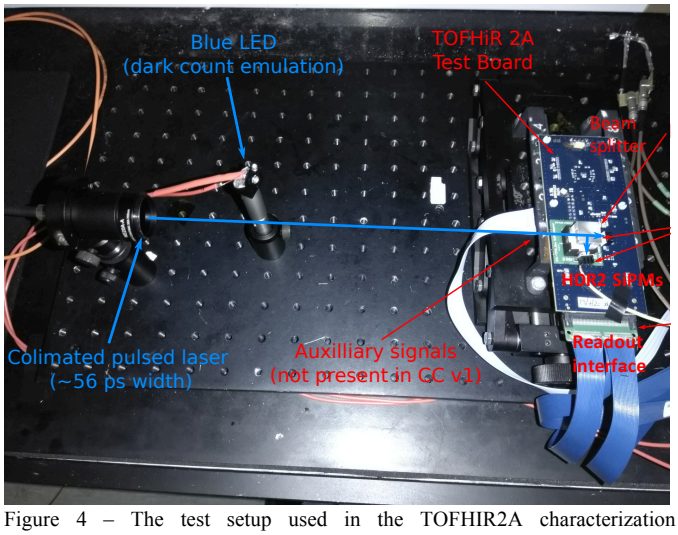


Figure 4 – The test setup used in the TOFHIR2A characterization measurements.

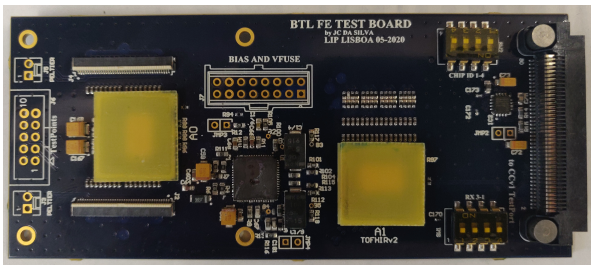


Figure 5 – The TOFHIR2 Test Board.

V. Characterization Results

A. Chip infrastructure

The measured consumption of the 32-channel chip was 485mA matching the simulation predictions. The TOFHIR2 global service block features a number of DACs used to set different DC levels in the chip. Probing pads allow to measure voltage levels at different points in the circuit including at different points in one test channel (see Fig.6).

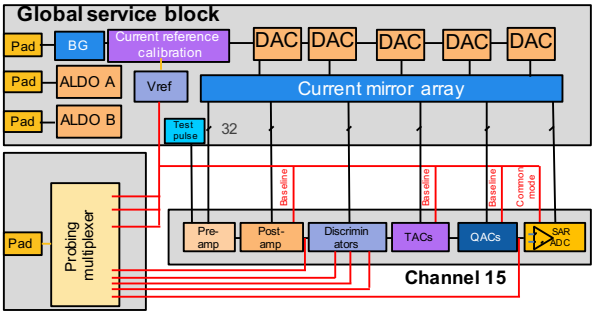


Figure 6 – Structure of the Global Service Block and probing points in the test channel (channel 15).

All DACs behave as expected. As an example, Fig.7 and Fig.8 show, respectively, the simulation and the measurement of the DAC responsible for the amplifier baseline adjustment. The simulation (Fig.7) is performed in all 16 PVT corners showing a spread of 5.1 mV in the low end (450 mV) and of 7.4 mV in the high end (550 mV). The scan of the amplifier baseline DAC shown in Fig.8 matches the simulation expectations with deviations from the nominal values compatible with the simulated spread.

Fig.9 illustrates the differential non-linearity (DNL) of one of the two ALDO DACs. A DNL< ± 0.5 LSB was measured.

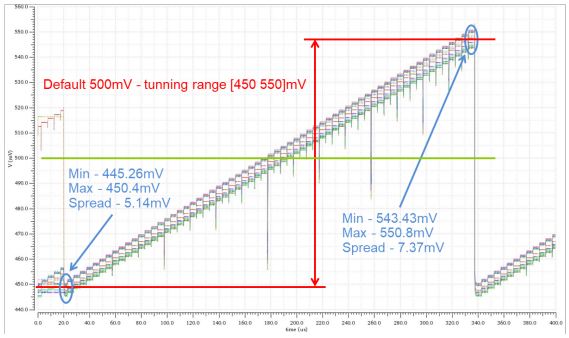


Figure 7 - Simulation of amplifier baseline DAC.

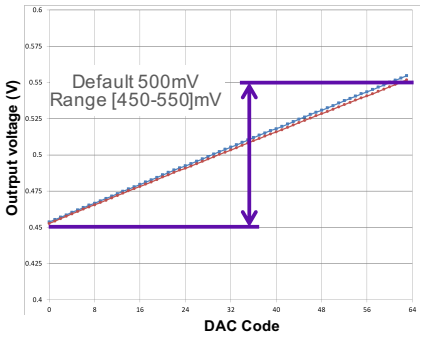


Figure 8 - Measurement of the amplifier baseline DAC in the global bias block (blue line) and in the post-amplifier of channel 15 (red line).

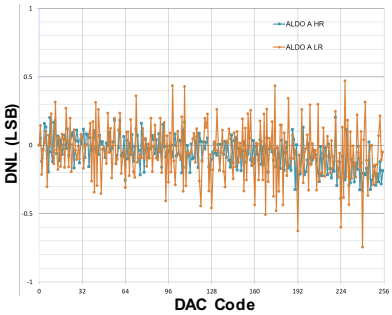


Figure 9 – DNL of the ALDO DAC (low and high gain settings).

B. *Front-end performance*

The electronics noise of the front-end amplifiers is estimated using a scan of discriminator T1 threshold DAC close to the baseline. An internal counter is used to measure the fraction of time the output of the discriminator is active. The data is shown in Fig.10 as a function of the DAC code. The DAC LSB is set to 2 mV. The data is fitted with an S-curve allowing to extract the noise r.m.s. of σ= 0.94 mV. From simulation, the expected noise is 1.2 mV.

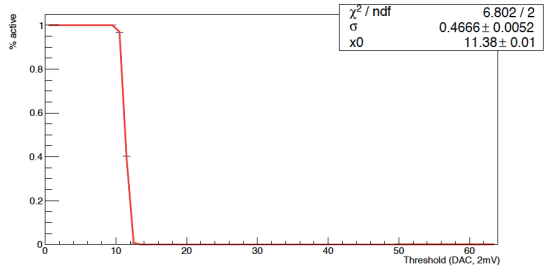


Figure 10 – Discriminator output active fraction as a function of the discriminator threshold above the baseline. The data is fitted with an S-curve allowing to extract the noise r.m.s. of σ= 0.94 mV

The shape of pulses generated by the SiPM HDR2 when illuminated by the picosecond pulsed laser was obtained by scanning the discriminator T2 threshold (LSB of 8 mV). The time of the leading and trailing edges of discriminator output pulse are measured by the TDC1 and TDC2, respectively, allowing to reconstruct the pulse shape. Using this method, the peak of pulse is not observed due to the minimum voltage above threshold required for the discriminator to respond and to the LSB step of the discriminator threshold scan. Fig.11 shows good agreement between simulation and data.

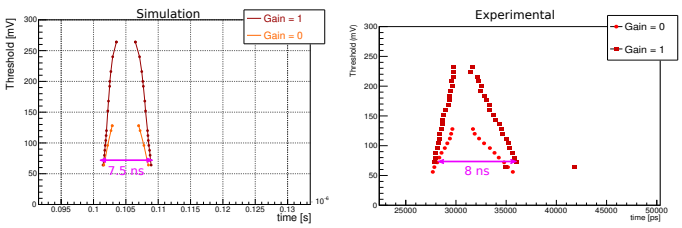


Figure 11 – Pulse shape at the input of the discriminator reconstructed with a threshold scan as obtained with simulation data (left) and experimental data (right). In both cases, the plot shows the pulses obtained with two different gain configurations of the pre-amplifier.

C. *TDC performance*

The TDC calibration uses an external digital pulse synchronous to the system clock and distributed internally to all TDC inputs in the chip. The time of the test pulse relative to the clock edge, defined in the FPGA of the readout board, is scanned in steps of ten picoseconds. The distribution of the TDC binning derived from the calibration data is shown for 2032 TACs in 4 different ASICs in Fig.12. The average bin size is 11.3 ps which matches well the value of 10 ps expected from simulation. It is worth noting the low dispersion of TDC binning (r.m.s.=0.4 ps).

The linearity of the TDC is derived from the code density distribution measured with random digital pulses following a uniform distribution in time. Fig.13 shows the Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL) as a function of the TDC code obtained for a typical TAC. Before linearity correction, DNL is less than ± 0.5 LSB and the INL is less than ± 2 LSB.

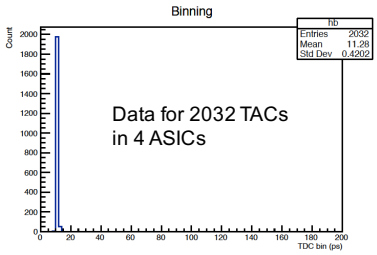


Figure 12 - Distribution of the TDC binning derived from the calibration data is shown for 2032 TACs in 4 different ASICs.

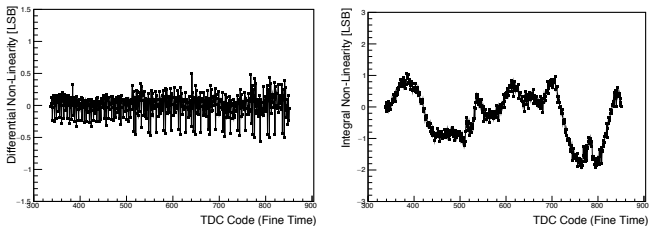


Figure 13 – DNL (left) and INL (right) as a function of the TDC code obtained for a typical TAC.

The TDC resolution is derived from coincidences between two TDCs in the chip receiving a common test pulse. This method is used to cancel common jitter (e.g. clock jitter). The average coincidence time resolution (CTR) estimated with 28 TDC pairs as shown in Fig.14 is 18.8 ps, from which we derive a TDC resolution of 13.3 ps. In this measurement, the dispersion of the resolution is 5.3% r.m.s.

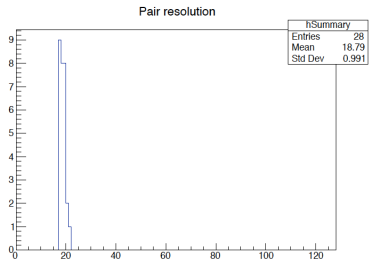


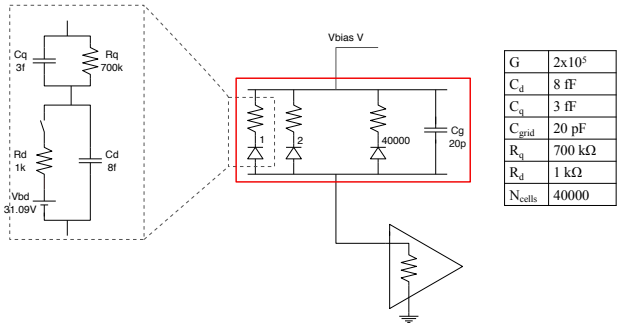
Figure 14 – Distribution of CTR for 28 TDC pairs, from which we derive an average TDC resolution of 13.3 ps.

D. *Time resolution with laser*

The time resolution of laser pulses is derived from the CTR of two channels. The laser pulse is optically split to illuminate two SiPMs HDR2 operated at overvoltage of 3.5 V (SiPM gain 3.8×10^5). Different pulse amplitudes are studied using optical attenuators.

The experimental data is compared to the results from the electrical simulations of the ASIC including electronics noise. In the simulation, the ASIC inputs are connected to an equivalent electrical model of the SiPM depicted in Fig.15 using the parameters indicated in the figure. The results presented here were obtained for SiPMs with 40'000 cells of $15 \times 15 \mu m^2$ each corresponding to $3 \times 3 mm^2$ devices. The simulation reproduces individual photoelectrons detected in one of the SiPM cells producing a certain number of charges according the SiPM gain simulated. SiPM dark counts were included when indicated assuming a uniform distribution of single photoelectrons with a certain average rate. SiPM cross-talk was included in the simulation. The timing for each photoelectron is smeared emulating the intrinsic SiPM jitter. We assumed a Gaussian distribution with 100 ps r.m.s.

Fig.16 show the channel time resolution as a function of laser pulse amplitude for experimental data and for simulation. A good agreement between both is obtained. For a laser pulse amplitude of 100 mV the time resolution is around 20 ps. For larger amplitudes, the combined contribution of the front-end noise and pulse slew rate is negligible and the time resolution becomes dominated by the TDC resolution (~13ps).



G	2×10^5
C_d	8 fF
C_q	3 fF
C_{grid}	20 pF
R_q	700 kΩ
R_d	1 kΩ
N_{cells}	40000

Figure 15 - SiPM equivalent electrical model assumed in the TOFHIR2A simulations.

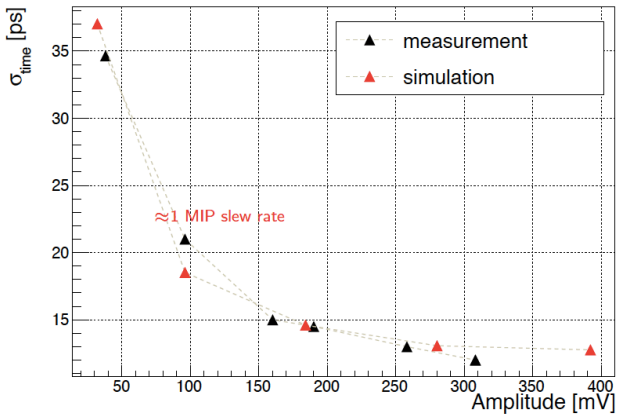


Figure 16 – Channel time resolution as a function of laser pulse amplitude for experimental and simulation data. The slew rate of the rising edge of a laser pulse with amplitude of 100 mV is expected to correspond to the slew rate of LYSO pulses for the average MIP energy deposit in the crystal.

E. *Test of DCR noise cancellation*

The test of the DCR noise cancellation module in TOFHIR2A was performed using laser pulses and background LED blue light emulating the SiPM dark counts. We have measured the channel time resolution of laser pulses using the method described in the previous section, while in parallel illuminating the SiPMs with blue light emitted by the LED (see Fig.4). Two SiPMs of HDR2 type, operated at overvoltage 3.5V (SiPM gain 3.8×10^5), were used. The calibration of the LED light was established by measuring the SiPM current as a function of the LED voltage. The SiPM current is converted in equivalent dark count rate taking into account the SiPM gain.

In order to compare with experimental data, we performed the simulation of laser pulses with a given number of photo-electrons superimposed to a given rate of dark counts, using the methods described in the previous section. In the simulation, the time resolution is extracted at the discriminator output.

Fig.17 shows the time resolution as a function of equivalent DCR for two different pulse amplitudes. The pulse amplitude is estimated from a scan of discriminator T2 threshold (DAC LSB 8 mV) as described in section V-B. A good matching between experimental data and simulation is observed.

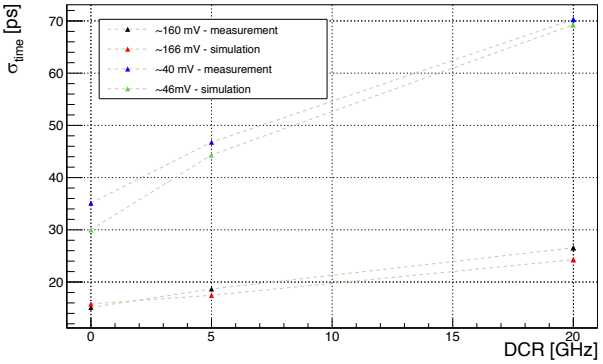


Figure 17 - Time resolution of laser pulses as a function of equivalent DCR emulated with LED blue light for two different pulse amplitudes for experimental data and simulation.

VI. TID RADIATION TEST

The resistance of TOFHIR2A to Total Ionization Dose (TID) was tested at the X-ray irradiation facility at CERN. The maximum expected dose in the barrel MTD is 3 Mrad. We have irradiated two ASICs, the first one up to 7 Mrad in steps of 0.5 Mrad and the second ASIC up to 3 Mrad in steps of 1 Mrad. The irradiations were performed at room temperature.

Between steps several measurements were performed. Using the ASIC test pads and an external digital multimeter, we measured the current consumption and the bandgap voltage, and we performed several DAC voltage scans (amplifier baseline, discriminator threshold, QAC/TAC baseline, ALDO DAC). Using TOFHIR2 data acquisition, we monitored the front-end noise making a scan of the T1 discriminator threshold, measured the shape of the internal analog test pulse using a scan of the T2 discriminator threshold, and performed the TDC and QDC calibration in all TACs and QACs in the two ASIC. The time interval between steps was of the order of 10 minutes preventing annealing effects. The same measurements were performed 12h after the irradiation in order to assess the effect of annealing at room temperature. Additionally, the time resolution with laser pulses was obtained using the ASIC irradiated at 3 Mrad.

We observed effects due to the large leakage current at dose ~1 Mrad reported for the technology TSCM 130nm produced in Fab 14 [8]. Fig.18 shows an increase of 20% of the current consumption after a dose of 1 Mrad followed by a decrease for larger doses. In agreement with previous observations [8], the current consumption returns to the original value after 12h annealing at room temperature. The increase of leakage in NMOS transistors originates a decrease by 15-20% of DAC's voltage range. Fig.19 illustrates this effect in the ALDO DAC.

The effects due to transistor leakage should not be visible in TSMC Fab 6, where the final chip production will be made, since the increase of leakage current at 1 Mrad in this Fab is ~100 times smaller than in Fab 14 [8].

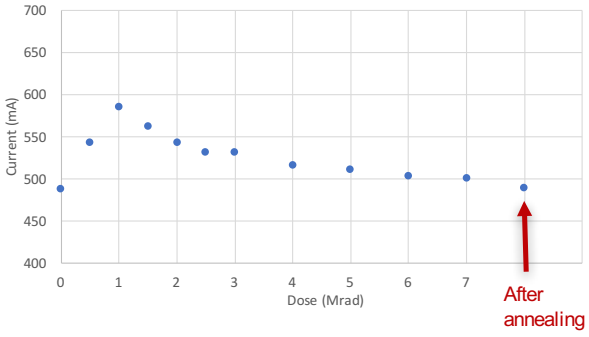


Figure 18 – TOFHIR2A current consumption as a function of dose.

On the other hand, we have observed negligible or minor effects on the frontend amplifiers, TDC and QDC up to 7 Mrad. Fig.20 shows the reconstruction of the internal analog test pulses after irradiation at different dose values. The pulse amplitude is reduced by ~6% after 7 Mrad. This reduction may be an indirect consequence of the change of transistor's biasing due to the radiation effects on the DACs. Fig.21 shows the coincidence time resolution between two TDCs as a function of the irradiation dose and Fig.22 shows the time resolution of laser pulses with amplitude ~40 mV as a function of discriminator threshold before and after irradiation at 3 Mrad. Within measurement uncertainties no sizable effects are observed.

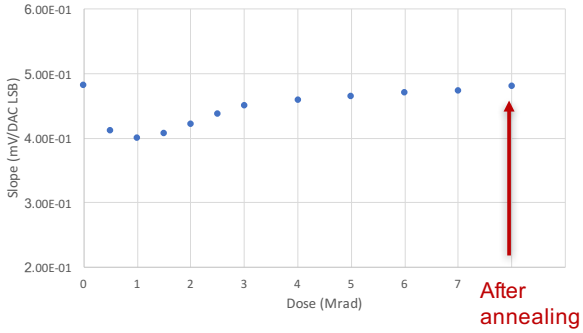


Figure 19 – Slope of the ALDO DAC as a function of dose.

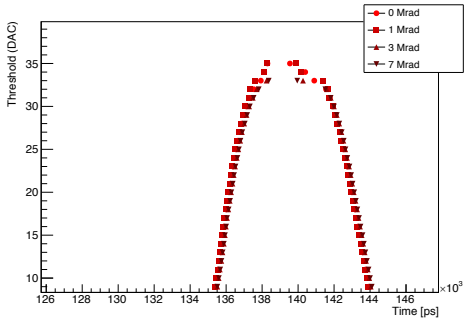


Figure 20 – Internal analog test pulse reconstructed for different irradiation doses.

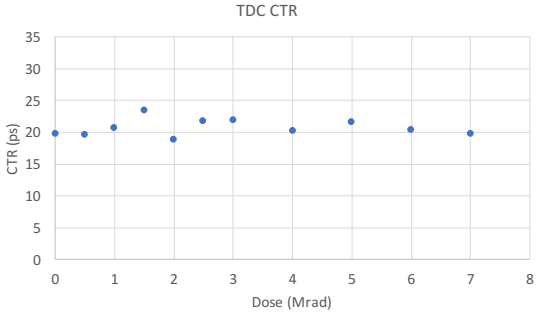


Figure 21 - Coincidence time resolution between two TDCs as a function of irradiation dose.

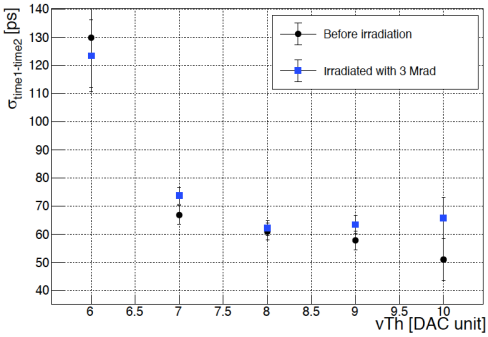


Figure 22 - Time resolution of laser pulses with amplitude 40 mV as a function of discriminator threshold before and after irradiation at 3 Mrad.

VII. SEE RADIATION TEST

The test of Single Event Effects (SEE) of TOFHIR2A due to localized ionization was performed at the Heavy Ion Facility (HIF) in Louvain-la-Neuve.

TOFHIR2A implements SEE protection using Triple Modular Redundancy (TMR) on the configuration bits (15'558 flip-flops) and automatic correction of Single Event Upsets (SEU). An internal counter (SEU counter) is used to count the number of corrections.

Possible transients (SET) in the clock and resync tree are not protected. Therefore, spurious resets or synchronization errors are to be expected. Additional protection for these effects will be implemented in TOFHIR2B.

We performed irradiations with different ions ($^{53}Cr^{16+}$, $^{36}Ar^{11+}$, $^{27}A^{18+}$, $^{22}Ne^{7+}$, $^{13}C^{4+}$, $^{84}Kr^{25+}$) and different incident angles (0^o, 30^o, 45^o) covering a wide range of linear energy transfer (LET) that allow to extrapolate the SEU errors to the LHC environment. The maximum beam flux used was $1.4x10^4$ ions/s/cm^2. The beam homogeneity of 10% on a diameter of 25 mm ensured uniform irradiation of the whole chip area.

During the HI irradiation, we operated the ASIC with the readout system described in section IV and acquired events generated by external test pulses. We checked the events content looking for SET, in particular changes in the synchronization counter (coarse time tag). Additionally, every five seconds, we read the SEU counter and all configuration bits. These observations allowed to monitor the cumulative SEU counter (corrected SEU errors), the number of configuration bits flipped (non-corrected errors) and the number of errors in the coarse time tag (synchronization errors).

Fig. 23 shows the measured cross-section of corrected SEU errors as a function of LET. The cross-section is parametrized by a Weibull distribution:

$$\sigma = \sigma_0 \cdot \left(1 - e^{-\left(\frac{L-L_0}{w}\right)^s}\right)$$

with the following fit parameters: σ_0 =6.0x10^{-4}cm^2, L_0=8.0x10^{-1} MeV.cm^2.mg^{-1}, w=15 and s=1.2. The resulting cross-section for the LHC environment (similar for the outer tracker, BTL and the calorimeters), is around $4x10^{-10}$ cm^2/chip which matches well the expectations for the technology used.

We have observed two uncorrected SEU errors in a long run (fluence of 4.5 M ions/cm^2) with Kr^{25+} ions at 30^o incidence, corresponding to a large LET of 37.4 MeV/mg/cm^2. The extrapolation to LHC indicates an expectation of <<1 uncorrected error/chip/year.

As expected, we have observed a few transient effects:

- 78 synchronization errors in the run with Cr^{16+} and 45^o incidence angle (LET=22.8 MeV.cm^2.mg^{-1}) and total fluence of 25 M ions/cm^2;
- 10 synchronization errors with Kr^{25+} and 30^o incidence angle (LET=37.4 MeV.cm^2.mg^{-1}) and total fluence 4.5 M ions/cm^2.
- 3 spurious chip resets were observed in the above two runs.

No destructive latch-up was observed.

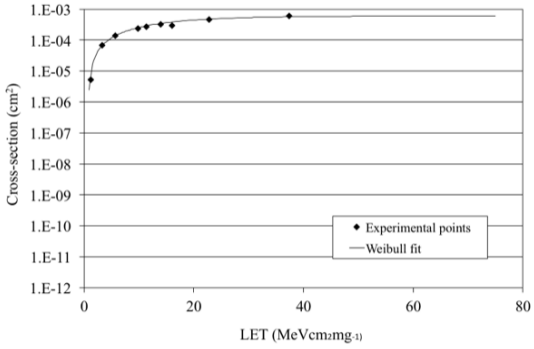


Figure 23 - Measured cross-section of corrected SEU errors as a function of LET and the Weibull fit.

VIII. CONCLUSIONS

The first full version (32 channels and complete functionality) of the readout chip for the CMS barrel MIP Timing Detector was developed. First measurements of TOFHIR2A match very well the simulation expectations. The service blocks, digital readout, front-end amplifiers, DCR noise cancellation, TDCs and QDCs were validated. Successful TID and SEU radiation tests have been performed.

ACKNOWLEDGMENT

We thank the MTD sensor team for providing the SiPMs used in the measurements and more generally the MTD project for all the support provided to the TOFHIR2 development. We also thank the CMS collaboration for creating the conditions that made this work possible.

We thank Federico Faccio, Giulio Borghello and André David for helping in the preparation of the radiation tests. In particular we are thankful to Federico Faccio for the extrapolation of the heavy-ion SEE data to the LHC environment presented in this paper.

We also thank the coordinators of the CERN X-ray irradiation facility and of the Heavy Ion Facility (HIF) in Louvain-la-Neuve for making available these facilities and for the help provided.

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