ISBN: 978-3-95450-204-2 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2019-WEPP046

TECHNOLOGY AND FIRST BEAM TESTS OF THE NEW CERN-SPS BEAM POSITION SYSTEM

M. Wendt*, A. Boccardi, M. Barros Marin, T. Bogey, I. Degl'Innocenti, A. Topaloudis
CERN, Geneva, Switzerland

Abstract

The CERN Super Proton Synchrotron (SPS) uses 215 beam position monitors (BPMs) to observe the beam orbit when accelerating protons or ions on a fast ramp cycle to beam energies of up to 450 GeV/c. In the frame of the CERN LHC Injector Upgrade (LIU) initiative the aged, and difficult to maintain homodyne-receiver based BPM read-out system is currently being upgraded with A Logarithmic Position System – ALPS. As the name indicates, this new BPM electronics builds upon the experience at CERN with using logarithmic detector amplifiers for beam position processing, and is well suited to cover the large range of beam intensities accelerated in the SPS. The system will use radiation tolerant electronics located in close proximity to the split-plane or stripline beam position monitor with GB/s optical data transmission to the processing electronics located on the surface. Technical details of the analog and digital signal processing, the data transmission using optical fibers, calibration and testing, as well as first beam tests on a set of ALPS prototypes are presented in this paper.

INTRODUCTION

After more then 20 years of operation, the Multi-turn Orbit POsition System (MOPOS) [1, 2] will be replaced by A Logarithmic Position System (APLS) to monitor the beam orbit and provide beam trajectory information of the Super Proton Synchrotron (SPS) at CERN. Figure 1 gives an overview of the new ALPS BPM read-out electronics in the form of a simplified block schematic, with more details in terms of BPM system requirements, beam conditions in the SPS and the initial R&D on ALPS found in [3].

Of the 215 BPM pickups distributed around the 6.7 km circumference of the SPS, most are single-plane "shoe-box" (split-plane) style BPMs, with a few stripline monitors in special locations. Apart from the mechanical structure of these BPMs themselves, all the existing BPM read-out hardware will be replaced, with a dedicated optical fiber infrastructure added. Due to the large variety of beam formats, intensities, particle species and operational modes of the SPS, a dynamic compression in the form of a set of logarithmic power detectors is applied to condition the BPM pickup signals to accommodate the required dynamic range of 90 dB without gain switching, see also [3]. Here the intensity normalization of the BPM electrode signals is based on the well-known principle:

$$\begin{aligned} \text{pos} &= \frac{1}{S_{\text{dB}}\,k} 20\log_{10}\left(\frac{A}{B}\right) \\ &= \frac{1}{S_{\text{dB}}}\left[\frac{1}{k_A^{\text{rg}}} 20\log_{10}(A^{\text{rg}}) - \frac{1}{k_B^{\text{rg}}} 20\log_{10}(B^{\text{rg}})\right], \end{aligned} \tag{1}$$

where A and B are the signals of the BPM pickup electrodes of a single plane and S_{dB} is the sensitivity of the BPM pickup. For the SPS $S_{\text{dB}}^{\text{hor}} = 0.2\,\text{dB/mm}$ and $S_{\text{dB}}^{\text{vert}} = 0.4\,\text{dB/mm}$ for the split-plane BPMs. Once the BPM pickup signals are detected, post-amplified and digitized, a linear calibration constant k (unit: ADC counts/dB) represents the transfer characteristic between the analog input and the digital output of the read-out electronics.

A key element of the analog front-end-electronics is the *Analog Devices* ADL5519 dual logarithmic detector amplifier. This is preceded by two matched 200 MHz band-pass filters, and has its outputs connected to ADC driver amplifiers followed by anti-aliasing low-pass filters. A calibration signal circuit is also present. The analog and digital front-end are assembled in a 19-inch, 1U housing that is installed

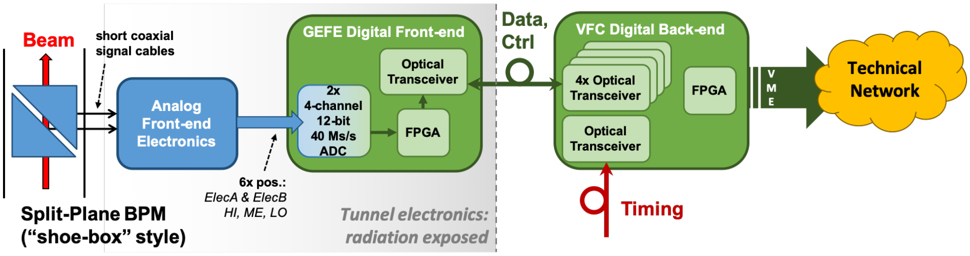

Figure 1: Simplified layout of the new CERN-SPS BPM read-out electronics (ALPS) – one channel shown.

---

[*] manfed.wendt@cern.ch

ISBN: 978-3-95450-204-2 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2019-WEPP046

in the SPS tunnel, in most cases, in close proximity to the BPM pickup. All its components are required to be radiation tolerant. Even though the ADL5519 logarithmic detector components claims to have a dynamic range > 60 dB, the usable dynamic range with reasonable low error of the logarithmic slope is limited to a maximum of 40 dB. Therefore, to meet the required 90 dB dynamic range, the pickup signal is split into three sensitivity ranges, spaced by approximately 20 dB to accommodate some range overlap: high (HI), medium (ME) and low (LO) – indicated by the index “rg” in Eq (1). The signal of each range is acquired simultaneously. While the ADL5519 holds two logarithmic detectors and a subtracting operational amplifier, the digitalization of the analog subtracted position signal caused fundamental calibration problems as the logarithmic slopes of the two detectors inside the ADL5519 were not sufficiently matched due to the manufacturing tolerances of the chip. Therefore, as indicted in Eq. (1), each electrode signal is digitized individually, allowing for different linear calibration factors k_A an k_B for both channels, with the final subtraction realized in the back-end gateware.

The output of each log-detector channel is digitized by a radiation tolerant 12-bit analog-to-digital converter (ADC). The raw ADC data is serialized and transmitted via an optical fiber link in a dedicated front-end transmission card, the Giga Bit Transceiver based Expandable Front-End, GEFE [4], a multi-purpose FPGA-based radiation tolerant card. A VME-based digital back-end located outside the SPS tunnel in a service building on the surface then receives and processes the transmitted data.

DIGITAL FRONT-END

The AD41240 digitizer was chosen for the ALPS system, a 4-channel, 12-bit, 40 MB/s, radiation tolerant ADC with 10.8 ENOBs (effective number of bits), originally designed for the CMS experiment at CERN. The AD41240 does not show any measurable degradation or drifts due to irradiation up to a total ionizing dose of 10 kGy. It also fulfils the resolution requirements imposed by the low position sensitivity of the SPS BPMs pickups. The 10.8 ENOBs of the AD41240 operating on an intensity range of 40 dB leads to a single bunch, single turn measurement resolution resolution limit of 150 µm, imposed by the digitalization of a single acquisition measurement. This is still within the specification for the SPS BPM system.

The ADL5519 has a very broad input bandwidth of 10 GHz, however, the bandwidth of the detected output signal is limited to a few-MHz. To accomplish the lower detection sensitivity for a single 2 ns long bunch containing $5 \cdot 10^9$ charges a compromise for the bandwidth of the 200 MHz input filter had to be made. This results in a response of the detected output signal of ~80 ns duration for a single bunch. Such a single bunch response gives only three valid signal samples from the digitizer, which is operating at a clock-speed of 40 MS/s, with none of them can be guaranteed to be on the peak of that signal due to the free-running ADC clock. The sampled waveform can nevertheless be digitally upsampled in the back-end gateware as its bandwidth remains in the *Nyquist* limit, which enables the peak value of the detected waveform to be extracted. It is worth to mentioning that the SPS is a fast cycling synchrotron operating with protons and ions in a range of 26-to-450 GeV/c and 14-to-400 GeV/c, respectively. This implies that the accelerating radio frequency varies during the energy ramp, making synchronous RF sampling difficult to achieve.

BACK-END GATEWARE

The back-end electronics are located in six service buildings on top of the SPS tunnel. This stores and processes the incoming data from the front-end tunnel electronics, before forwarding the results to the software tools used by the SPS control room operators. The main hardware component of the back-end electronics is a "field-programmable gate array" (FPGA)-based electronics board, the so-called "VME FMC Carrier HPC-DDR3" (VFC-HD) [5]. The ALPS project requires ten VFC-HD boards per service building, all of them inserted into a single "Versatile Module Europe" (VME) crate [6]. Each VFC-HD communicates with four front-ends through dedicated, radiation-tolerant, high-speed optical links, know as "GBT/Versatile Links" [7]. A block diagram highlighting the main building blocks of the back-end gateware running in each VFC-HD is illustrated in Fig. 2.

BPM Channel Module

The BPM channel module is the core of the back-end gateware. Its principal task is to process, store and forward the incoming data from the front-end electronics to the operational software. It also generates the control signals used to inject test and calibration pulses in the front-end electronics. Each BPM channel is connected to a dedicated GBT-FPGA core [8]. The GBT-FPGA core decodes and parallelizes the incoming serial stream from the GBT/Versatile Link, as well as encodes and serializes the front-end calibration control signals. All four BPM Channels are connected to a common Wishbone [9] (Wb)/VME bus interface which communicates with the single-board computer of the VME crate for both, control and data readout. The BPM channel module may be be divided into five blocks: conditioning of the raw digital signal data stream, sample validation, acquisition mode selection, calibration controller, and control / timing / trigger.

Conditioning of the Raw Digital Data Signals

The raw data from the pick-up electrodes needs to be conditioned in order to provide an accurate and precise measurement of the beam position. This digital signal conditioning procedure is performed in six steps:

Programmable delay A precise alignment of the sampling time of the data stream of the two electrode signals is critical for a correct normalization, i.e. calculating the difference of the data samples of $20\log_{10}(A)$ and $20\log_{10}(B)$.

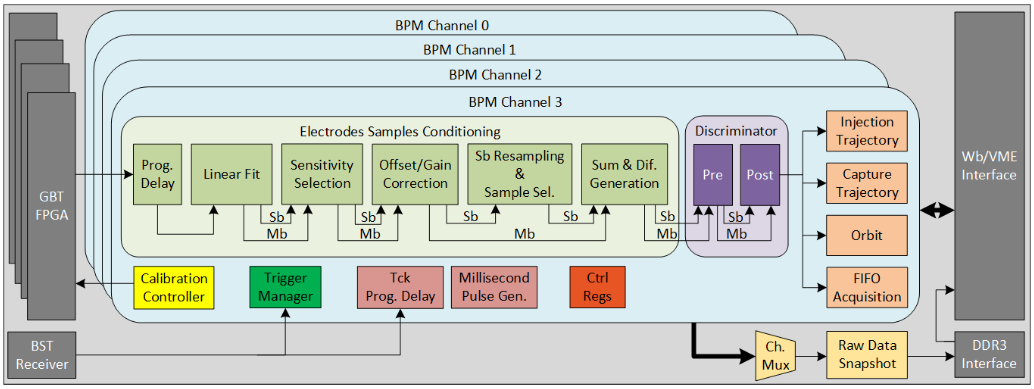

Figure 2: Block diagram of the ALPS back-end gateware.

However, due to mismatches in the transmission lines, as well as the time uncertainty in the sampling process and serial data transmission, data from both electrodes may not arrive on the same clock cycle. A programmable delay block allows to the two data streams to be aligned, compensating for any time misalignment.

Linear fit Each of the ALPS front-end read-out electronics units is characterized on a test bench, with the transfer coefficients k_A^{rg} and k_B^{rg} for each range $\mathrm{rg} \in$ HI, ME, LO stored in a database. The linear fit module applies the corresponding coefficients to the raw data, along with the relevant pickup sensitivity S to calculate the beam position in millimetres.

Sensitivity selection In order to select the most adequate sensitivity range (high, medium or low), the sensitivity selection block implements the following algorithm:
First, the data from both electrodes of each sensitivity range is averaged depending on the beam format, e.g. single bunch or long series of bunches. The high sensitivity channel is selected by default. In case the averaged high sensitivity value reaches a predefined threshold, the sensitivity selection moves to medium. The change from medium to low sensitivity follows the same process. To avoid a continuous flip-flop effect switching between two ranges, a hysteresis is added to the sensitivity thresholds.

Offset/gain correction The offset and gain of the digitized signals may present significant differences from board to board. With the purpose of having consistent measurements along the different channels of the ALPS system, the offset and gain mismatch is minimized using calibration values obtained during the qualification process of the analog electronics.

Single bunch resampling and sample selection As previously mentioned, single bunch (SB) measurements require a resampling of the data. With the aim to find the best compromise between performance and resources utilization, a variety of different implementations to perform this resampling were analyzed. For this specific case, the most appropriate implementation was found to be a factor 8 interpolation followed by an infinite-impulse response (IIR) lowpass filter of first order. This resampling process is performed in parallel to avoid requiring a factor 8 increase in the clock frequency of the system, at the cost of a substantial increase in logic resources utilization. To minimize the order of the subsequent IIR lowpass filter and thus its logic resources utilization, the interpolation uses a simple linear fit, instead of zero padding. The parallel processing IIR lowpass filter implementation is based on a look-ahead technique. Following the resampling process, the peak sample of the single bunch is selected and forwarded to the next block in the data conditioning chain.

Sum and difference calculation This block finally calculates sum and difference of the previously selected sensitivity range (high, medium, or low) for the data of the two BPM electrodes A and B. The sum is proportional to the beam intensity, while the difference, having applied the correct calibration factors k and S, represents the beam position in mm.

Discriminator

Sample validation is carried out by the discriminator module based on the sum data. Conceptually the validation algorithm is quite simple. If the sum data reaches a predefined threshold and its slope is lower than a predefined value, the difference (position) data stream are considered to be valid. However, as a result of the different beam conditions in the SPS, other constraints must be added to avoid unwanted samples to be taken as valid. As a result, the sample validation algorithm is separated into two modules, a pre-discriminator and a post-discriminator.

Pre-discriminator The previously mentioned conceptual algorithm is implemented in the pre-discriminator, but in this case with a dynamic threshold that varies based on the value of the sum data. This dynamic threshold is required due to the high dynamic range of the system. On the one hand, single bunches of low intensity require the setting of a low-value threshold, while high intensity beam data requires high threshold values to avoid spurious data.

Post-discriminator At this stage of the sample validation, a second algorithm performs the following two tasks:

1. Distinguishes between single bunch (SB) and multi bunch (MB) data.
2. If MB data is detected, it masks the first seven and last seven samples of the valid data, which are affected by residual ringing generated by the 200 MHz hairpin band-pass filter.

Acquisition Modes

The system features four operational acquisition modes:

Injection trajectory Provides the turn-by-turn position of the first 64 turns of a batch after its injection.

Capture trajectory Provides the turn-by-turn position of the beam, averaged over a selectable range of bunches, for a predefined number of turns.

Orbit Provides the average of the position of the whole beam, averaged over a programmable period of time.

FIFO acquisition Self-triggered mode for machine commissioning, where no beam synchronous timing signals are required. Provides the turn-by-turn position of the first 64 turns of a single bunch after its injection.

Raw data snapshot Used for calibration and debugging and shared by all four BPM channels. Provides up to 100 s of raw data at selectable times along the data stream.

Control, Timing, Trigger

The back-end gateware features a register-based control architecture. The timing and trigger modules decode signals from various timing cards, and forwards them to the relevant gateware processing modules.

Calibration Signal Controller

The calibration signal controller emulates bunch pulse signals from a memory. Once generated, this module forwards the test pulses to the front-end, along with the control signals for attenuators located at the analog RF inputs in the tunnel.

CALIBRATION

An automatized calibration bench is used to generate BPM pickup-like pulse signals which are fed into the RF inputs of the ALPS front-end. A special ALPS back-end is used to analyze the transfer characteristic of each channel for a variety of simulated beam formats (e.g. single bunch, multi-bunch batches with 5, 25 and 50 ns bunch separation), while sweeping over a sufficient range of beam intensities. Figure 3 shows a typical result of for a 5 ns multi-bunch calibration measurement displaying the response of all 6 acquired channels (channel *A* and *B* for all three ranges).

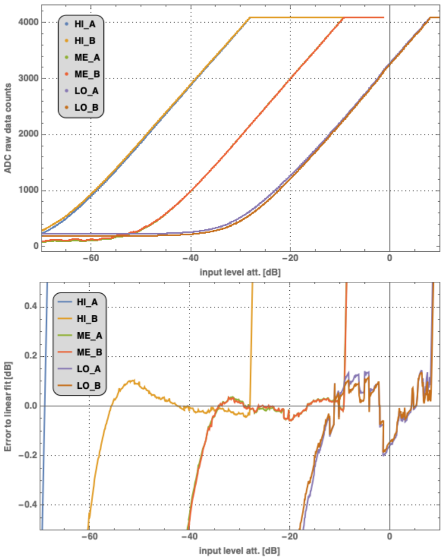

Figure 3: Result of a calibration sweep on the front-end.

The upper graph shows the transfer characteristics, while the lower plot displays the linearity error with respect to a linear fit. The results for the two channels of each gain are seen to be matched nearly perfectly, implying a very low error for centered beams. For larger position excursions the two channels will sample at different locations on these curves. However, it can be seen that the maximum error for a given channel over a range of 20dB does not exceed 0.1 dB, corresponding to a maximum position linearity error of $<500\,\mu m$ over the complete position range. The poorer quality of the lowest sensitivity range is due to a combination of factors, including the mismatch of attenuators on the calibration test bench and the switch to a high power amplifier to mimic the extremely high intensity signals obtained from the beams destined for the LHC.

VALIDATION WITH SPS BEAM

At the end of 2018 a pre-series of the ALPS system was installed into the SPS on 12 BPMs, to validate the performance under realistic beam conditions. The BPM pickup signals were split between the standard MOPOS and new ALPS read-out electronics, which enabled a direct comparison. BPM measurements were performed over several days and analyzed under all the different beam conditions in the SPS. This demonstrated that the new system achieving a turn-by-turn resolution of $<200\,\mu m$ for long batches (>200 ns) and $\sim 30\,\mu m$ in orbit mode. The detection sensitivity for low intensity ion bunches was sown to be $<5 \times 10^9$ charges, which also meets the requirements.

As a result of this successful validation, the decision was taken to restart the SPS operation in 2021, at the end of the current long shut-down, with the new ALPS BPM read-out system.

REFERENCES

[1] W. Rawnsley *et al.*, "An RF signal processing module for the SPS orbit observation system Upgrade", in *Proc. of the PAC'97*, Vancouver, Canada, 1997, May 12 – 16, 2P066, pp. 2049–2051.

[2] C. Boccard *et al.*, "Performance of the new SPS beam position orbit system (MOPOS)", in *Proc. of the DIPAC 1999*, Chester, UK, 1999, May 16–18, PS12 session, pp. 126–128.

[3] M. Wendt *et al.*, "UPGRADE OF THE CERN SPS BEAM POSITION MEASUREMENT SYSTEM", in *Proc. of the 9th Int. Particle Accelerator Conf (IPAC'18)*, Vancouver, BC, Canada, Apr.-May 2018, pp. 2047–2050. `doi:10.18429/JACoW-IPAC2018-WEPAF085`

[4] M. Barros Marin *et al.*, "The GBT-based Expandable Front-End (GEFE)", in *Proc. of the Topical Workshop on Electronics for Particle Physics (TWEPP 2015)*, Lisbon, Protugal, September 2015.

[5] A. Boccardi *et al.*, "A Modular Approach to Acquisition Systems for the Future CERN Beam Instrumentation Developments", in *Proc. of the ICALEPCS 2015*, Melbourne, Australia, October 2015, pp. 1103–1106, THHB2O02.

[6] ANSI/VITA, American National Standard for VME64, 1-1994 (R2002).

[7] P. Moreira *et al.*, "The GBT Project", in *Proc. of the Topical Workshop on Electronics for Particle Physics (TWEPP 2009)*, Paris, France, September 2009, pp. 342–346. `doi:10.5170/CERN-2009-006.342`

[8] M. Barros Marin *et al.*, "The GBT-FPGA core: Features and Challenges", *JINST*, vol. 10, p. C03021, 2015. `doi:10.1088/1748-0221/10/03/C03021`

[9] The Wishbone B4 specification: `https://cdn.opencores.org/downloads/wbspec_b4.pdf`