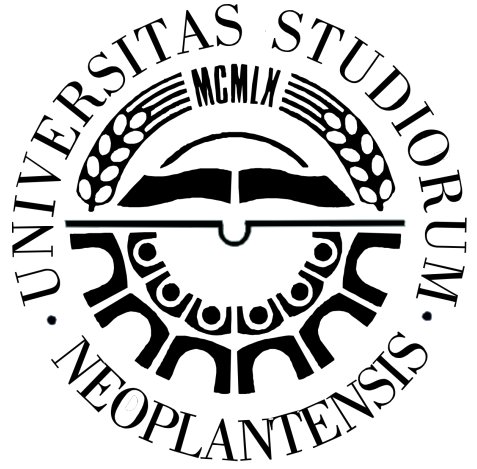
Карактеризација наменског примопредајног интегрисаног кола мале снаге за потребе експеримената у високоенергетској физици

Никола Рашевић

Дипломски рад



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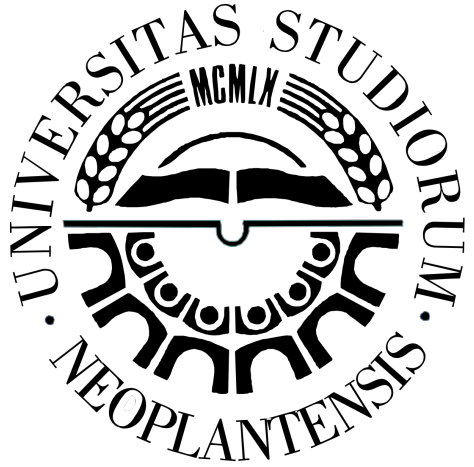
Универзитет у Новом Саду
Србија
Септембар, 2020.

Characterization of a Low Power Gigabit Transceiver ASIC for High Energy Physics Experiments

Nikola Rašević

Bachelor Thesis



Faculty of Technical Sciences
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To my parents Dragana and Ljubisav
who dedicated their lives
to make me and my sister become good persons.

To all my teachers
who selflessly shared their knowledge with me
and made me become an engineer.

Abstract

The high energy physics experiments developed at CERN for the High Luminosity Large Hadron Collider (HL-LHC) are based on optical links that provide the clock distribution and control towards the front-end electronics located in the experiments, and data transmission back from these electronics circuits to remote data acquisition systems. The corresponding data is encoded and decoded by custom integrated circuits able to stand the high level of radiation in this specific environment. In particular for the Trackers at the HL-LHC, a low power gigabit transceiver was developed (LPGBT).

This bachelor thesis will cover the following points:

- Introduction to CERN and the CMS experiment at the HL-LHC with focus on the Tracker.
- Summary of the features of the LpGBT chip.
- Design, fabrication, assembly and debugging of a multilayer printed circuit board, rated up to 10Gbps, for the characterization of the LpGBT features and to specify integration requirements.
- Measurement of the electrical properties of the LpGBT with the characterization board.

This project is supported at CERN by the CMS Tracker Upgrade engineering team and by the LpGBT chip design and back-end support teams.

Сажетак

Експерименти у високо-енергетској физици, развијени у ЦЕРН-у, за нови супер хардонски сударач честица велике луминозности, су базирани на оптичким комуникационим везама, које обезбеђују дистрибуцију тактног сигнала и контролу електрониских компоненти постављених у самим детекторима честица, као и пренос информација од детектора до удаљених система за прикупљање и обраду података.

Одговарајући подаци се кодирају и декодирају коришћењем специјализованих интегрисаних кола, способних да издрже велике дозе радијације у посебним радним условима околине. Специјално за детекторе у новом супер хадронском сударачу честица, развијено је наменско примопредајно интегрисано коло, мале снаге, за рад на фреквенцијама реда гигахерца.

У овом раду ће бити обрађени следећи аспекти:

- Упознавање са истраживањима у ЦЕРН-у и ЦМС експериментом у новом супер хардронском сударачу честица велике луминозности, са фокусом на самом детектору честица.
- Скуп карактеристика LpGBT примопредајног интегрисаног кола.
- Пројектовање, производња, састављање и поправљање вишеслојне штампане плоче, предвиђене за рад до 10Gbps, намењене за карактеризацију LpGBT интегрисаног кола и дефинисање правила за његову интеграцију у друге системе.
- Мерење електричних карактеристика LpGBT интегрисаног кола коришћењем карактеризационе плоче.

Овај пројекат је подржан у ЦЕРН-у од стране инжењерског тима за унапређење детектора честица на ЦМС екперименту као и тимова који се баве пројектовањем LpGBT интегрисаног кола.

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1 Introduction

1.1 The European Organization for Nuclear Research - CERN

Founded in 1954, the CERN laboratory sits astride the Franco-Swiss border near Geneva. It was one of Europe's first joint ventures and now has 23 member states.

Physicists and engineers at CERN use the world's largest and most complex scientific instruments to study the basic constituents of matter – fundamental particles. Subatomic particles are made to collide together at close to the speed of light. The process gives us clues about how the particles interact, and provides insights into the fundamental laws of nature. We want to advance the boundaries of human knowledge by delving into the smallest building blocks of our universe.

The instruments used at CERN are purpose-built particle accelerators and detectors. Accelerators boost beams of particles to high energies before the beams are made to collide with each other or with stationary targets. Detectors observe and record the results of these collisions, [2].

1.2 Large Hadron Colider - LHC

The Large Hadron Collider (LHC) is the world's largest and most powerful particle accelerator. It first started up on 10th September 2008, and remains the latest addition to CERN's accelerator complex. The LHC consists of a 27-kilometre ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way.

Inside the accelerator, two high-energy particle beams travel at close to the speed of light before they are made to collide. The beams travel in opposite directions in separate beam pipes – two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. The electromagnets are built from coils of special electric cable that operates in a superconducting state, efficiently conducting electricity without resistance or loss of energy. This requires chilling the magnets to -271.3°C – a temperature colder than outer space. For this reason, much of the accelerator is connected to a distribution system of liquid helium, which cools the magnets, as well as to other supply services.

All the controls for the accelerator, its services and technical infrastructure are housed under one roof at the CERN Control Centre. From here, the beams inside the LHC are made to collide at four locations around the accelerator ring, corresponding to the positions of four particle detectors – ATLAS, CMS, ALICE and LHCb.

1.3 Compact Muon Solenoid - CMS

The Compact Muon Solenoid (CMS) detector sits at one of these four collision points. It is a general-purpose detector; that is, it is designed to observe any new physics phenomena that the LHC might reveal.

CMS acts as a giant, high-speed camera, taking 3D "photographs" of particle collisions from all directions up to 40 million times each second. Although most of the particles produced in the collisions are "unstable", they transform rapidly into stable particles that can be detected by CMS. By identifying (nearly) all the stable

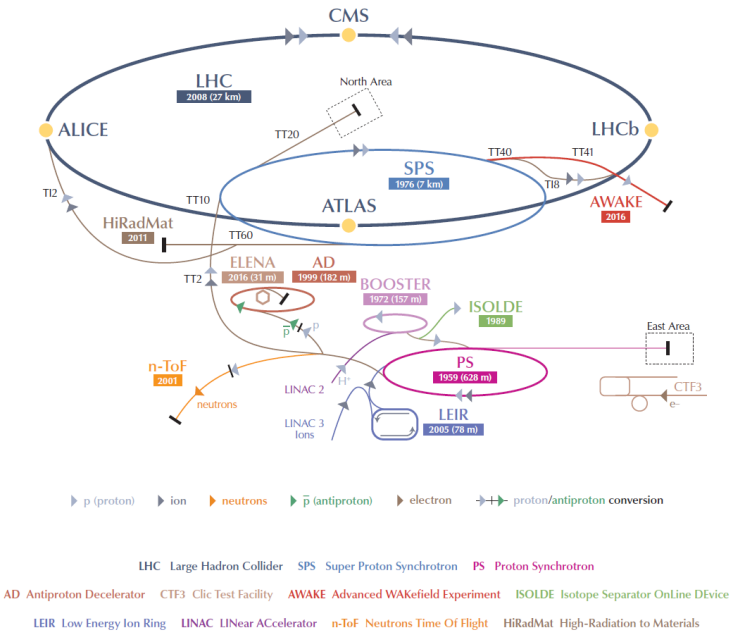

Figure 1: Large Hadron Colider - LHC

particles produced in each collision, measuring their momenta and energies, and then piecing together the information of all these particles like putting together the pieces of a puzzle, the detector can recreate an "image" of the collision for further analysis, [3].

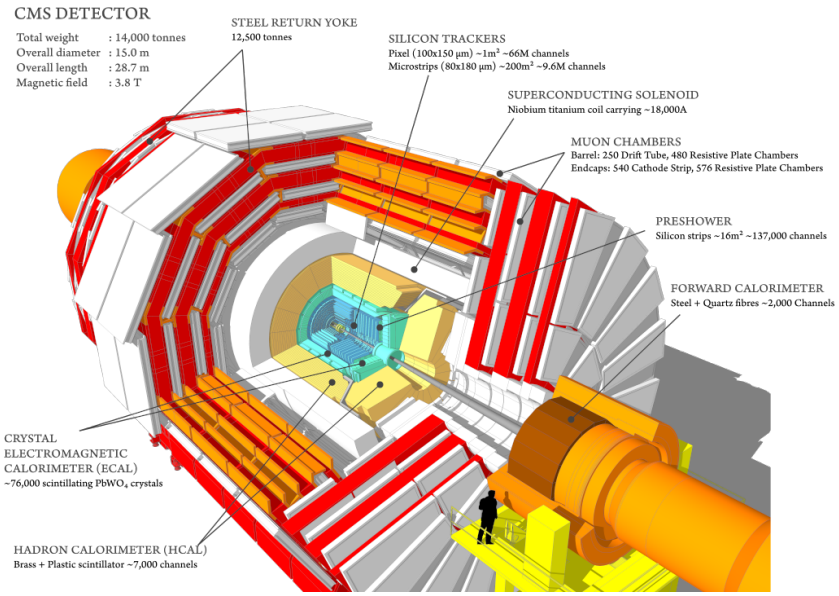

Figure 2: Compact Muon Solenoid - CMS

1.4 Low Power Giga Bit Transceiver - LpGBT

Every sensor module which is installed in the LHC detectors, need some interface which can provide stable data link between that sensor module and control room computers. The new high luminosity LHC provides more collisions per second than

it was in the previous versions of the LHC. The number of events on the single sensor for HL-LHC, as it was said earlier in the text, exceeds few tens of thousands per second, so it is huge amount of data which should be filtered and transmitted to the control computers. Because of the required data rate, the best communication type which was selected for this specific use is optical link. Another difficulty is very high dose of ionising radiation in the area where the sensor module is placed. The previous version of the Giga Bit Transciever (GBTx) does not meet the requirements of the new accelerator regarding transmission speed and power consumption, and it led to the design of the new generation chip, Low Power Giga Bit Transceiver (LpGBT), which can handle described difficulties, [8].

The LpGBT is a radiation tolerant ASIC that can be used to implement multi-purpose high speed bidirectional optical links for high-energy physics experiments. The ASIC supports 2.56 Gb/s links in the direction from the control room to the detectors (downlink) and 5.12 or 10.24 Gb/s links in the direction of the detectors to the control room (uplink). The architecture of the LpGBT is shown on the Figure 3.

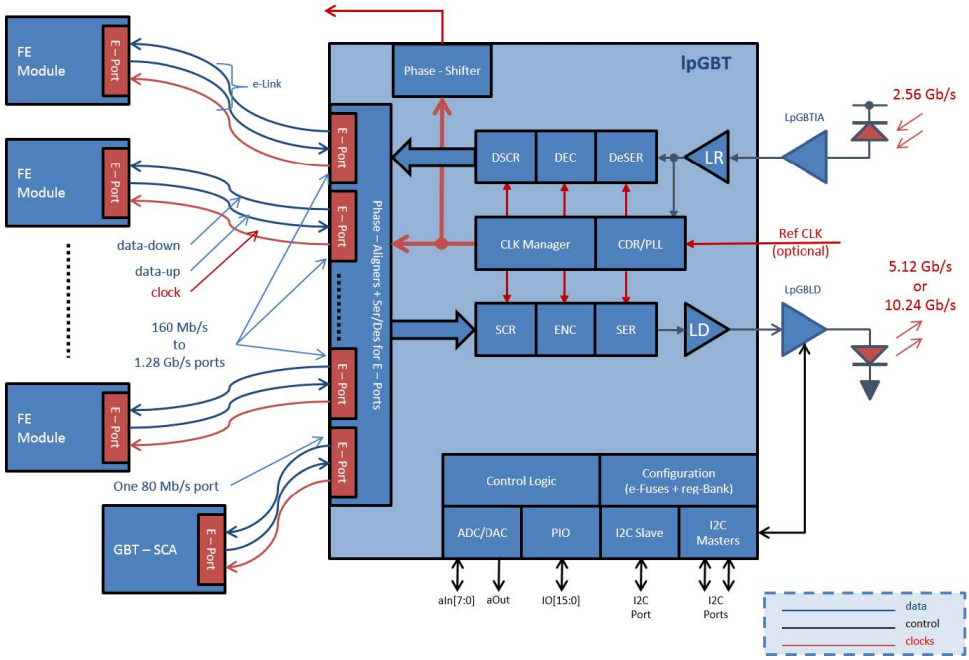

Figure 3: The LpGBT architecture.

Logically the link provides three "distinct" data paths for Timing and Trigger Control (TTC), Data Acquisition (DAQ) and Slow Control (SC) information. In practice, the three logical paths do not need to be physically separated and are merged on a single optical link. The aim of such architecture is to allow a single bidirectional link to be used simultaneously for data readout, trigger data, timing, experiment control and monitoring. Such an architecture establishes a point-to-point bidirectional optical link (two fibres) with constant latency that can function with very high reliability in the harsh radiation environment typical of high energy physics (HEP) experiments at LHC, [6].

The lpGBT is a highly flexible link interface chip with a large number of programmable options to enable its efficient use in a large variety of front-end applications:

- Can be configured to be a bidirectional transceiver, a simplex transmitter or a simplex receiver;
- Several front-end interface modes and options;
- Extensive features for precise timing control;
- Several features for experiment control and monitoring;
- Robust operation against SEUs.

1.5 VLplus Characterization Board

This board should be designed to characterize the LpGBT chip, to allow the testing of basic features and the chip functionality in a high radiation environment and to define a reference design for all the LpGBT based boards.

The characterization board is a six layer rigid board, with dimensions of 170 mm x 160 mm. It hosts the LpGBT, which is the only active component on the board, and several connectors and switches.

The characterization board allows access to seven e-link data inputs, four e-link data outputs, four e-link clocks, four phase-shifting clocks, 40 MHz reference clock input, high-speed data transceiver, two master I2C lines and one slave I2C line. On-board DIP switches enable setting the chip address, the chip mode of operation, lockmode, I2C slow-control pin and optional I2C pull-ups. The mode configuration is also available through the I2C ten-pin header connector.

The power supply is provided from outside through two-pin power connectors, which enables complete independence from on-board power regulators and sources.

Most hybrids are designed to host components on just one side, which is also the case with the most of on-detector boards, which could be a potential problem in terms of chip power decoupling, because the LpGBT chip is designed with the requirement to have the decoupling below the chip (on the opposite side of the board). That is the reason why we are designing the characterization board with two optional decoupling positions.

2 System Requirements

The VL+ characterization board should meet certain requirements and satisfy the user's desire in order to test the characteristics of the LpGBT ASIC chip. The board must provide the environment for our chip with as low as possible influence on the chip's characteristics and to provide the best possible integrity of signal and power lines. The board should also reduce the possibility of mistakes caused by the user testing the chip and to be easy to use.

The Figure 4 represents the block diagram which shows components that should be placed on the board and their interconnection. The board should provide I2C interface, that will allow access to the LpGBT configuration and this will be available trough 10-pin header connectors. The access to the chip's e-links, clocks, data inputs, data outputs and high speed serial link has to be with as low as possible influence on the integrity of the signals and it was decided to be realized using high-quality SMA (SubMiniature version A) connectors. This type of connectors is specially designed for high speed applications. The basic configuration of the chip (mode of operation, I2C chip address, I2C pull-up resistors, source of the reference clock) should be accessible with on-board components and it will be realized using the three four-state DIP switches.

To ensure stability and availability of a power supply and to reduce the influence of the power regulation circuits, the power will be provided from outside, using the two terminal block connectors. The board has to meed radiation hardness standards, which introduces additional constrains as for example the commercial semiconductor components must not be used on the board. The board should also provide testing of the different decoupling schemes.

The use of the LpGBT chip in the detectors will be in a configuration with four chips connected in series, controlled with the same I2C bus and same channel of a high-speed link. The VL+ characterization board has to provide adequate testing of this configuration and it means that four boards need to be connected in series.

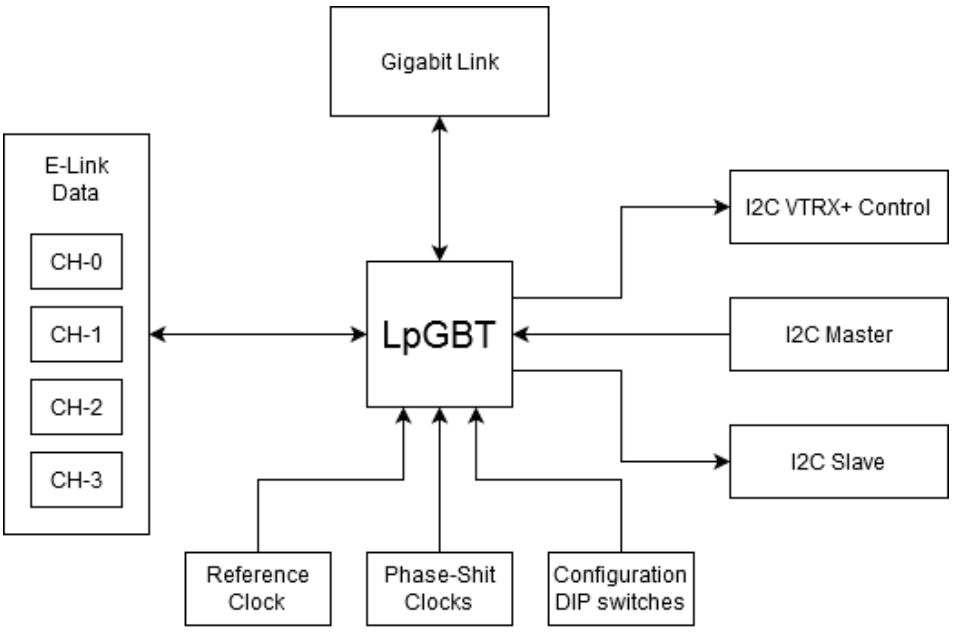

Figure 4: The block diagram of the VL+ Characterization Board.

3 Hardware Design

According to the requirements given by the users of the VL+ characterization board, a detailed layout of the hardware design was made. The design workflow, explanation of the board layout and placement of the components on the board will be given in this section.

3.1 Board Stackup

One of the key moments in the very beginning of the board design process comes when the number of layers should be defined. The number of layers is not trivial thing, it is very important part on the path of the good design routine, in terms of board functionality, reliability and production price. Technology evolves and progresses every day, and today number of layers in PCB moved up to few tens. From the other aspect the production price should be reasonable, and because the fact that every new layer increases the price exponentially, but not just the price, also the debugging time. If the operating conditions allow, the number of layers should be as low as possible.

Sometimes also the materials or type of the board, whether flexible or rigid, can limit our decision. Materials are very important, especially when board is made for higher frequency operations. As the technology improves there are always new materials on the market, which should be considered. The first step is to define the type of a dielectric material, core or prepreg, conductor is usually copper, but sometimes there is also need for different conductor materials. The other thing that plays a role is a dielectric constant of the material, which shows significant influence also on lower frequencies. The third thing about materials represents the placement and orientation of the fibers of which material consists, but this is important just on either very high frequencies or very high current consumption.

The Figure 5 shows the stackup of the board that was designed here. The word *stackup* is used, between the engineers, to represent the detailed explanation about number of layers, dielectric and conductor materials, layer thicknesses and vias that interconnect layers. This detailed explanation on how and why the shown stackup was chosen will be given further in the text in this section.

The VL+ characterization board is choosen to be six layer rigid board. The dielectric materials are different between the layers. The central one is FR-4 core material with relative permittivity of 4.5 and thickness od 0.8 mm. The other four dielectric layers are made of *Rogers* RO-4450-F prepreg with relative permittivity of 3.52 and thickness of 0.1 mm. The *Rogers* dielectric materials are made for applications that operate on higher frequencies, also this type of materials are good choice when controlled impedance is required on PCB. Over the outer copper layers are layers of solder mask, with thickness of 15 µm and relative permittivity from 3.9 to 4.

The copper weight of all metal layers is 1 oz and thickness is 35 µm, except outer layers, which are 50 µm thick because of the final board plating.

Between the layers for internal connections are used different types of vias. There is one big through hole drilled via, also in the middle between third and fourth layer vias are drilled. The connections between internal layers (L2_GND to L3_POW and L4_POW to L5_GND) are made with laser buried vias and between outer and

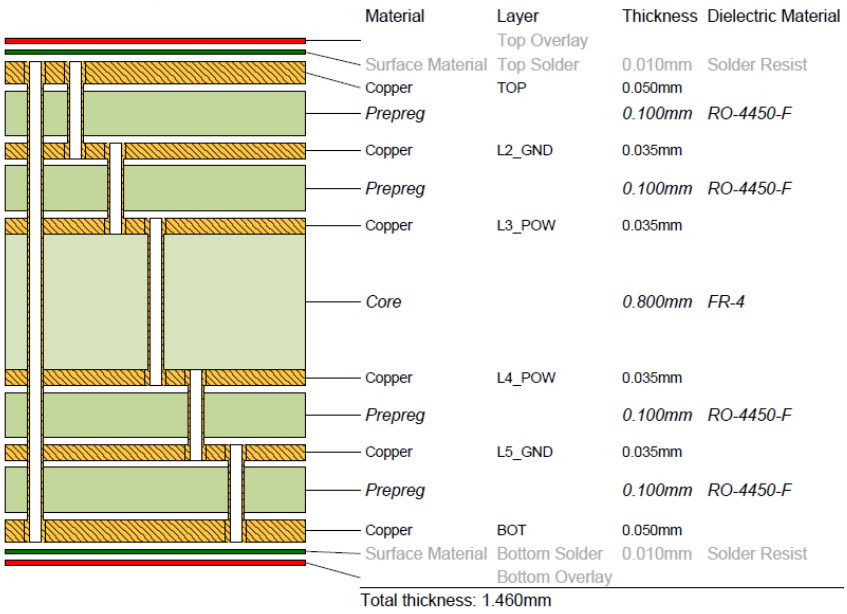

Figure 5: The board stack-up

inner layers (TOP to L2_GND and L5_GND to BOT), are made also with laser vias but blind.

This geometry was the best possible choice to match all the requirements, also to be similar with on-detector electronics.

3.2 Component Placement

The first challenge when starting to design PCB is to place the components in the best possible way. The design of the VL+ characterization board requires even more attention when placing components and the reason is a lot of high speed lines that should be routed to SMA connectors, also three I2C (Inter-Integrated Circuit) buses, GPIO (General Purpose Input Output) lines and power lines.

One of the important aspects for this board when talking about placement of the components is position of the decoupling capacitors, because the board has to provide two different variants of decoupling scheme.

3.2.1 ASIC Chip

The LpGBT chip, which is the central component of the VL+ characterization board, should be carefully placed. The LpGBT ASIC chip is in BGA (Ball Grid Array) package with 289 bumps. There are requirements that should be followed, high speed gigabyte lines should be short, and far from other analog and digital lines on the board. The length of the lines between the chip and SMA connectors for E-link clocks, data input and outputs, should be approximately equal.

3.2.2 Decoupling Capacitors

The purpose of the decoupling capacitors is to decouple one part of an electrical network or circuit from another. Noise caused by other circuit elements is shunted

through the capacitors, reducing the effect it has on the rest of the circuit. The position of the capacitors has influence on decoupling response, good practice is to keep them as close as possible to a network that should be decoupled, which is in our case the LpGBT chip.

The LpGBT chip is designed to have power decoupling capacitors right bellow the chip on the opposite side of the board, but in most on-detector PCBs this requirement cannot be met, because of stiffeners which are placed bellow the board. One of the purposes of the VL+ characterization board is to test the behaviour of the chip for two different decoupling scheme, regarding the position of capacitors. The first option is when capacitors are right bellow the chip, as it should be, following the designer's recommendation, and the second option is when the chip and capacitors are in the same layer, as it is usual case in most of applications with the LpGBT chip.

The decoupling capacitors are placed around the chip when they are on the same side of the board, and right bellow the chip when they are on opposite sides of the board.

On the Figures 6 and 8 are shown side views for two configurations of the decoupling capacitors, which are explained above. The Figures 7 and 9 show the decoupling capacitors in the board layout view, and their position regarding the chip, which is marked with the white square.

Figure 6: Side view of the chip and the decoupling capacitors position, when they are on the different layers.

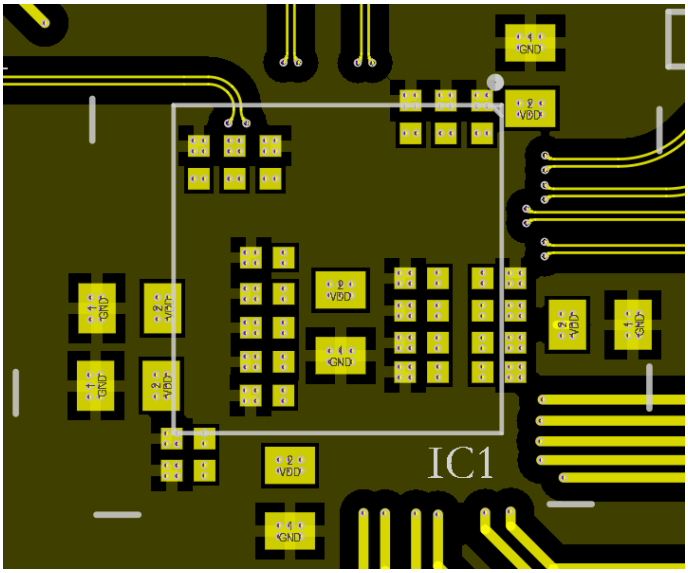

Figure 7: Layout view of the chip and decoupling capacitors position, when they are on the different layers.

Figure 8: Side view of the chip and the decoupling capacitors position, when they are on the same layer.

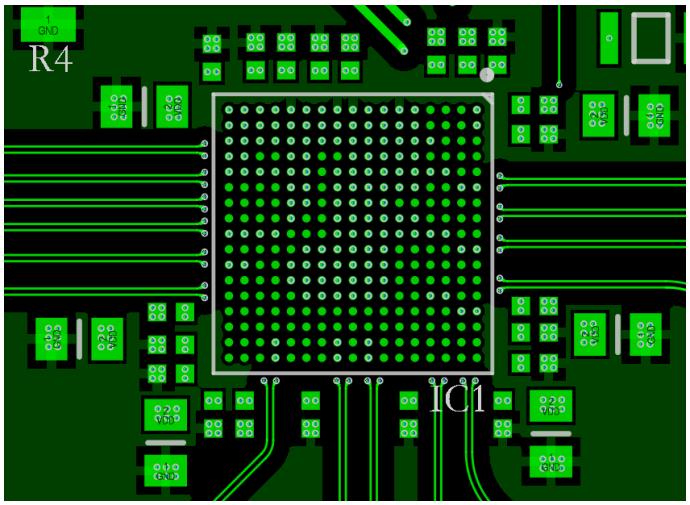

Figure 9: Layout view of the chip and decoupling capacitors position, when they are on the same layer.

3.2.3 Connectors

On the VL+ characterization board access to the E-link clocks, data inputs and data outputs, also high speed link of the LpGBT chip is provided via SMA connectors. The SMA connectors are big trough hole components and require some space around them, because wires need to be easily screwed on the connectors. Also this type of the connectors have signal pin in the middle. The low speed connectors have four ground pins around, but high speed connectors, are with nine ground connections. This geometry of the connectors sets new constraints when talking about component placement.

On this board it was decided to place all SMA connectors around the ASIC on approximately same distance from the chip. All the differential lines go in pair on two neighbouring connectors.

3.3 The PCB Layout

Before we start working on the layout of the VL + characterization board, we need to define some constraints. After few iterations it was decided that differential pairs are going to be placed on top and bottom layers. Inner layers are determined for power and ground planes. As it is mentioned before, when it was discussed about stackap, the power planes are defined to be in the middle of the board and the ground planes are in first inner layers, from top and bottom sides. The reason for setting ground planes bellow the layers with the differential pairs, is the practice to reference impedance controlled lines to the ground line.

Single-ended lines does not have predefined layers for routing and they are routed in the way to interact as little as possible with lines that transmit signals at high speeds. The only restriction is not to make too big plane cuts, especially on the paths between the LpGBT chip and the power and ground terminals.

The layouts of the VL+ characterization board top and bottom layers are shown in the Figures 10 and 11, respectively.

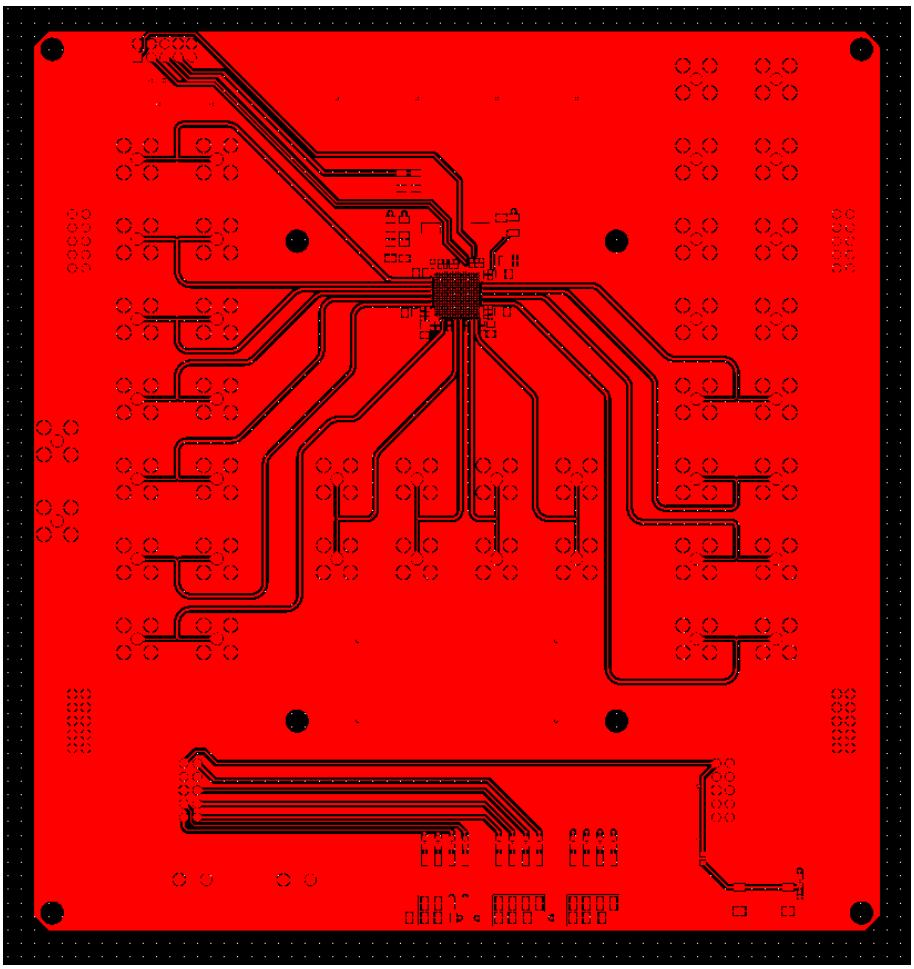

Figure 10: The VL+ characterization board leyout of the top layer.

One of the important rules that also must be followed when designing boards for high-speed operations, is the shape of the transmission lines, in our case transmission lines are differential pairs. The shape must have smooth curves, the right angles and sharp angling are absolutely not desirable. Instead the right angled and sharp curved lines we used rounded tracks. This shape of the transmission lines helps in reducing antenna effects along the line, which causes electromagnetic interference spreading over the board and reflections that can affect and attenuate other signals on the board.

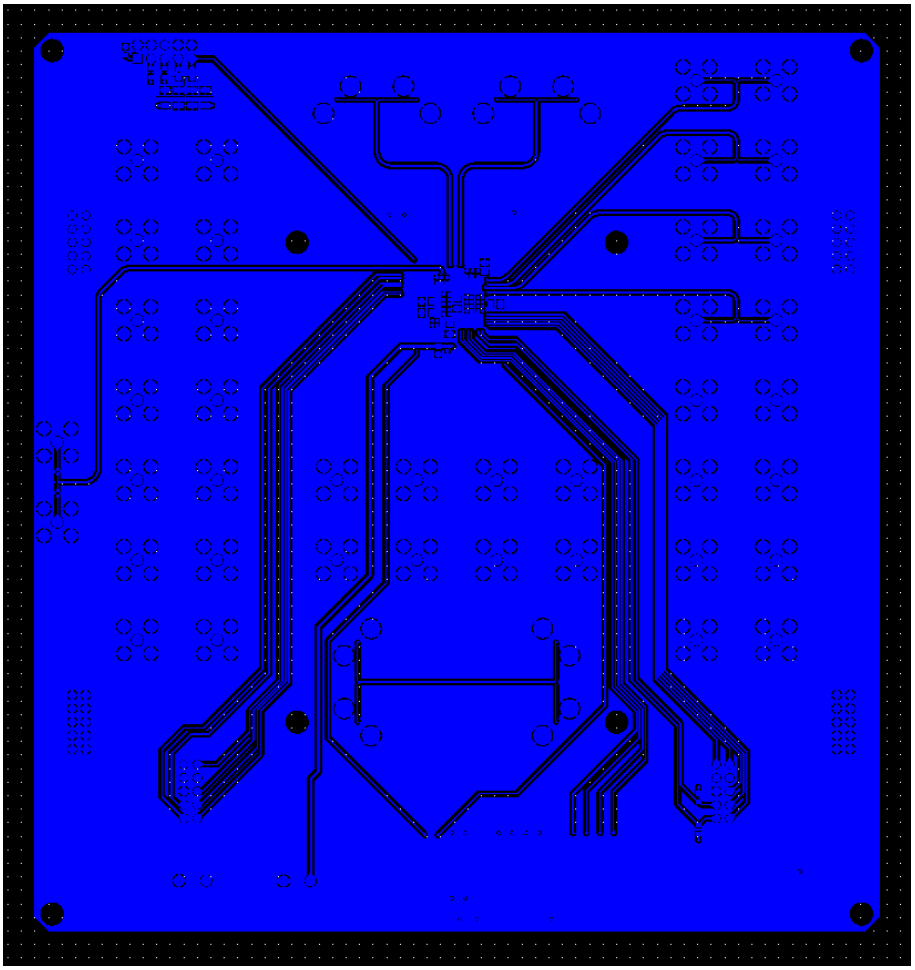

Figure 11: The VL+ characterization board leyout of the bottom layer.

3.3.1 Differential Pairs

The input and output links of the LpGBT are realized as LVDS (Low-Voltage Differential Signaling) lines. The LVDS is a differential signaling system, meaning that it transmits information as the difference between the voltages on a pair of wires, the two wire voltages are compared at the receiver. In a typical implementation, the transmitter injects a constant current of 3.5 mA into the wires, with the direction of current determining the digital logic level. The current passes through a termination resistor of about 100 Ω to 120 Ω (matched to the cable's characteristic impedance to reduce reflections) at the receiving end, and then returns in the opposite direction via the other wire. From Ohm's law, the voltage difference across the resistor is therefore about 350 mV. The receiver senses the polarity of this voltage to determine the logic level, [5].

The controlled impedance of lines is required and has to match the value of the termination resistor, which is in our case 100 Ω, because we want to reduce reflection to a minimal value. The problem that can occur in the circuit if the impedance is not matched is reflection of a signal and reducing the previously explained logic levels, in that case the differential voltage is not 350 mV anymore, it goes lower and depending on a level of impedance mismatch and reflections, the signals may become unusable. Understanding the influence of impedance mismatch on signals will be more clear in the following sections, where eye diagrams and S-parameters are explained.

On the Figure 12 is shown the part of the differential pair we used in the characterization board design. The differential impedance is calculated using the software tool Saturn PCB and checked by the manufacturing companies. The geometry that is obtained after calculation is 100 µm trace width, 100 µm gap spacing and 100 µm dielectric material thickness. Later in the text will be explained more details regarding the impedance and it's calculation.

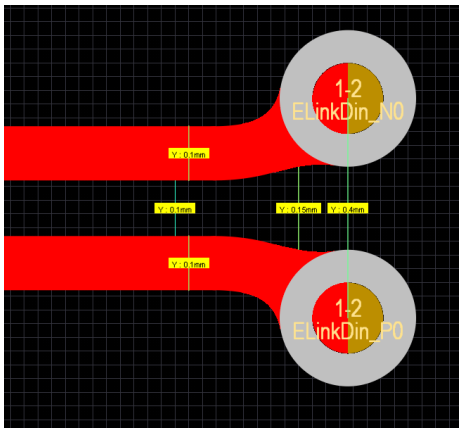

Figure 12: The differential pair geometry.

The next Figure 13 shows the differential pair on the side of the SMA connector. It can be seen that at one point the differential pair is divided, because of the geometry and size of the connectors. This short part can be critical, the differential coupling in this single ended section does not exist and we can not calculate the differential impedance, but there is one option for overcoming this problem. The impedance of single ended parts must be the half of the differential impedance,

which is in our case 50 Ω. The geometry of a single ended lines regarding the desired impedance is 120 µm trace width and 100 µm dielectric thickness. Tthe transition between trace parts with different widths must be mitigated, because this is the point where mismatch can also occur, so the transition in trace width is realized gradually.

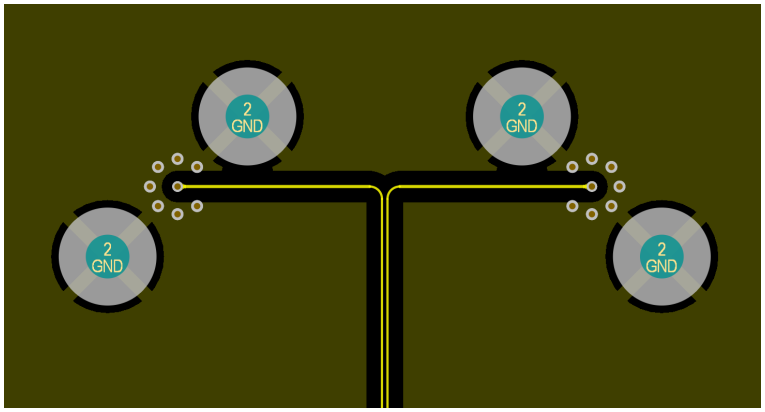

Figure 13: The differential pair on the side of SMA.

When routing the differential pair on the transmission line, it was necessary to change the layer from top to bottom. The need to change the layers arises due to the specific construction of the SMA connector, with which the differential pair should be connected. The technology constraints does not allow using the trough hole vias in the area around the chip and the layer changing was done using five vias in series. Every time when signal passes through via, impedance mismatch occurs and it causes multiple mismatches which affects the differential pair impedance, but this can not be avoided. The solution of this transition between the layers using vias is shown on the Figure 14.

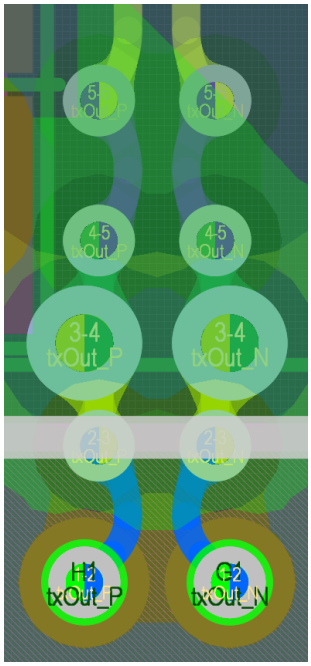

Figure 14: The position of vias on the transmission line differential pair.

3.3.2 BGA Chip Fanout

The BGA package with 0.5 mm pitch, as it is the case with our board, requires some attention to be properly routed. A lot of differential pairs, high speed link, analog and digital lines on such a small area, makes headache because the space between two rows of the BGA bumps allow just one trace to be placed, and we need tens of traces to escape the chip area. The problem was solved by using via in pad technology for chip fanout. Via in pad technology allows placing vias right in PCB pads, where the BGA bumps are going to be soldered. That technique allowed us to route lines bellow the BGA in inner layers, which is much easier because of more available space. The Figure 15 shows the BGA footprint with placed vias in pads.

Another problem that can happen when routing lines bellow the BGA chip in the same layer with the chip is leaking of solder along the traces. That problem can be solved, by using solder mask defined pads, but it requires bigger copper pads and then appears the new problem because the pads are too close to each other. This is another reason why we used via in pad technology.

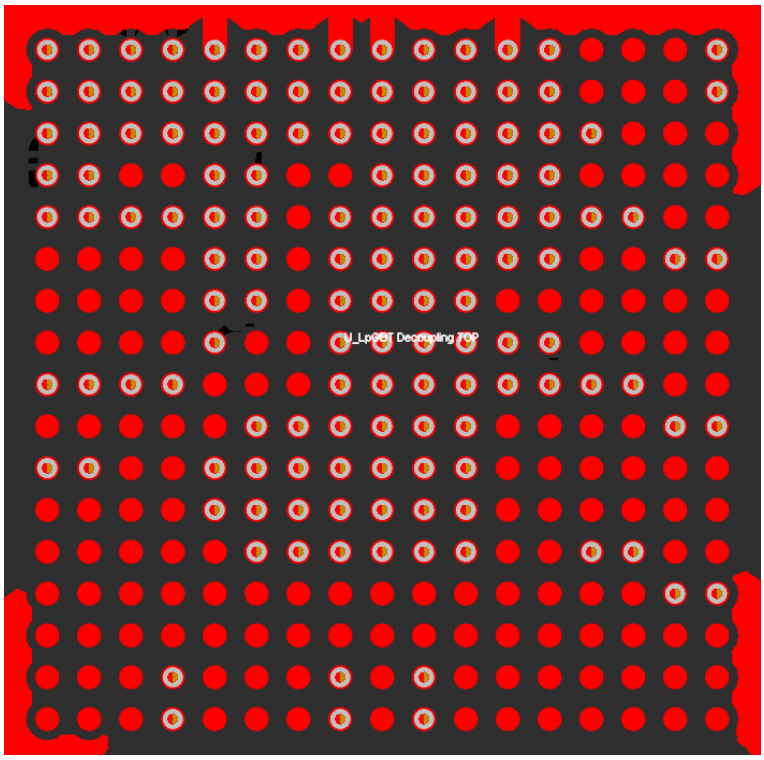

Figure 15: The BGA fanout using via in pad technology.

The via in pad technology is realised by filling vias with the conductive epoxy material and plating the copper on the top of the via, then there is a conductive connection between the layers, but without a hole, which makes soldering easy and there is no way for a solder to leak trough holes in the inner layers. The cross section of the via in pad can be seen on the Figure 16.

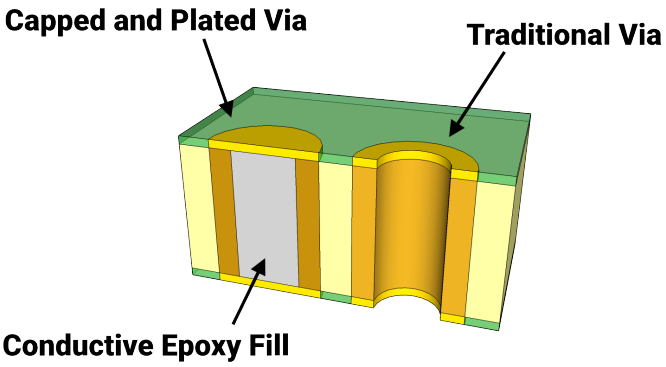

Figure 16: Via in pad cross section.

3.4 Designed Board Overview

The Figure 17 shows the 3D view of a designed VL+ characterization board. Assigned numbers relate to all components placed on the board.

Starting with the LpGBT ASIC chip as a central component, placed in the middle part of the board, surrounded with the components that chip is connected to, marked with number (1). The high-speed gigabyte link transmission (TX) and reception (RX) lines marked on the board with number (2), which is placed near the chip but also near the board outline, to provide easy access to SMA connectors from outside sources. The next module marked with the number (3) refers to E-Link data channels, of which there are 4 in total, surrounding the chip, and provides easy access to all SMA connectors. Number (4) refers to a chip reference clock input. The phase-shifting clock outputs, of which there are 4 outputs in total, grouped in one place, are marked with number (5). With the number (6) is marked I2C slave interface input, while on the other side of the board is the same connector used for I2C master interface output. The number (7) marks I2C master interface directed toward the VTRX+ laser module, used for it's control, placed near the high-speed link, which is also connected to the VTRX+ module. The DIP switches used to configure the chip on start-up are marked with the number (8), placed on the bottom outline of the board, far from other components and easy accessible by the user. The terminal block connector marked with the number (9) refers to power input line, next to it is located another connector of the same type, used to provide power for the chip fusing.

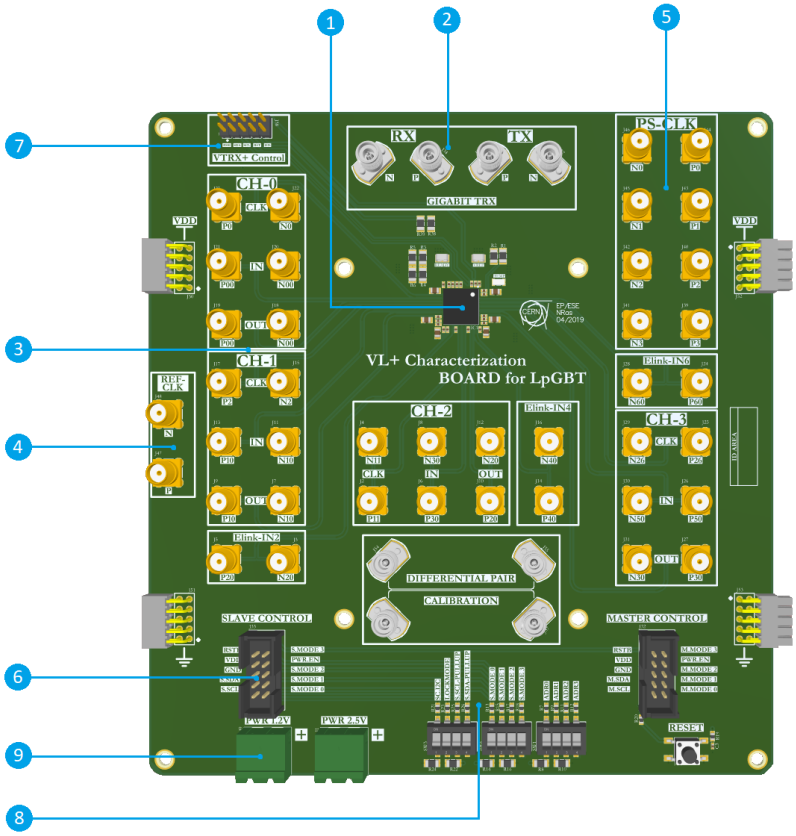

Figure 17: The VL+ characterization board 3D view with marked components.

As it is mentioned before in text, in the detector applications, LpGBT chip works in configuration with other three chips connected in series. The first one is master, and it is controlled over I2C interface or over high speed serial link, while other three chips are in slave mode and they are controlled with master chip. The VL+ characterization board should also provide possibility to test this configuration of the chips.

The board is designed to have power connectors on it's sides, left and right, which are placed in such a way as to allow the board to be connected in series, and to share power supply. The I2C connectors are also set up to allow the boards to be connected with as few cable crossings as possible.

The Figure 18 shows the 3D view of the configuration when four boards are connected in series, sharing the power supply using 10-pin header connectors for power and ground lines and and I2C connectors next to each other.

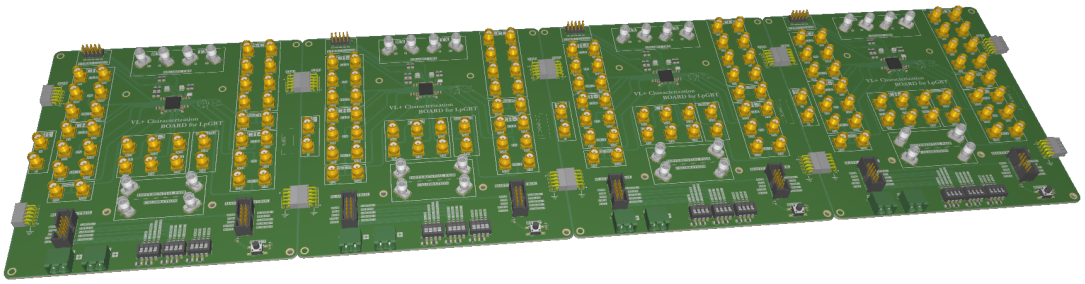

Figure 18: Four VL+ characterization boards connected in series.

One the Figure 19 are shown two assembled boards connected in series, with the RaspberryPi mini computer next to them, which is used to control the boards over the I2C interface.

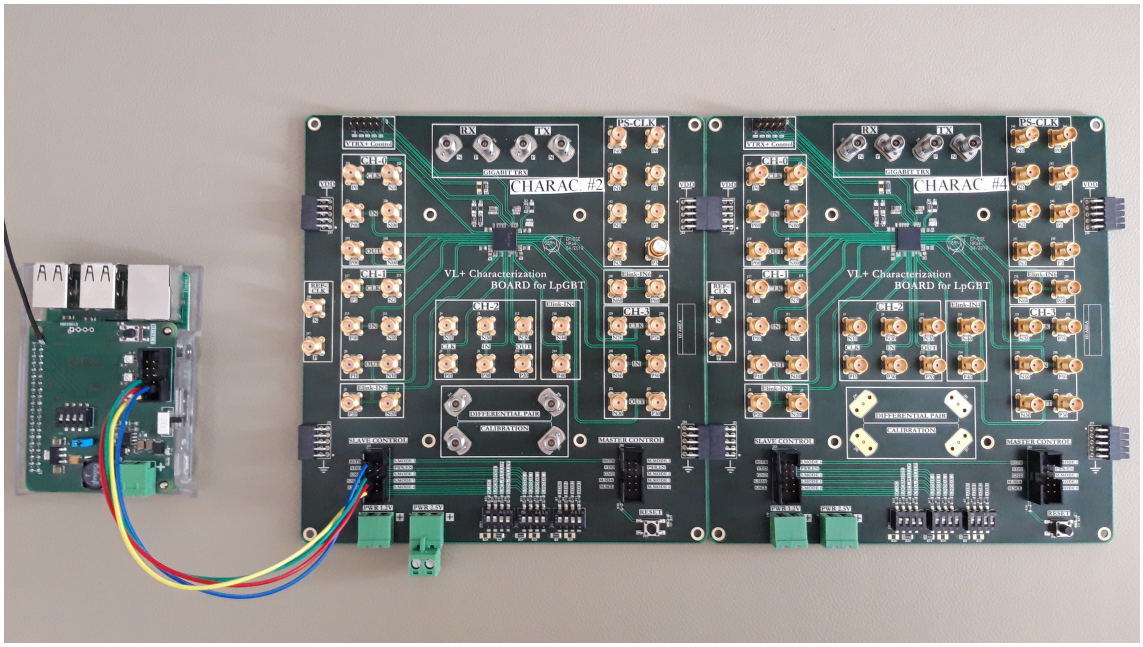

Figure 19: Two assembled boards connected in series and RaspberryPi next to them.

The Figure 20 shows the fully assembled and functional VL+ characterization board, with the LpGBT chip as the board central component, which is shown on the Figure 21.

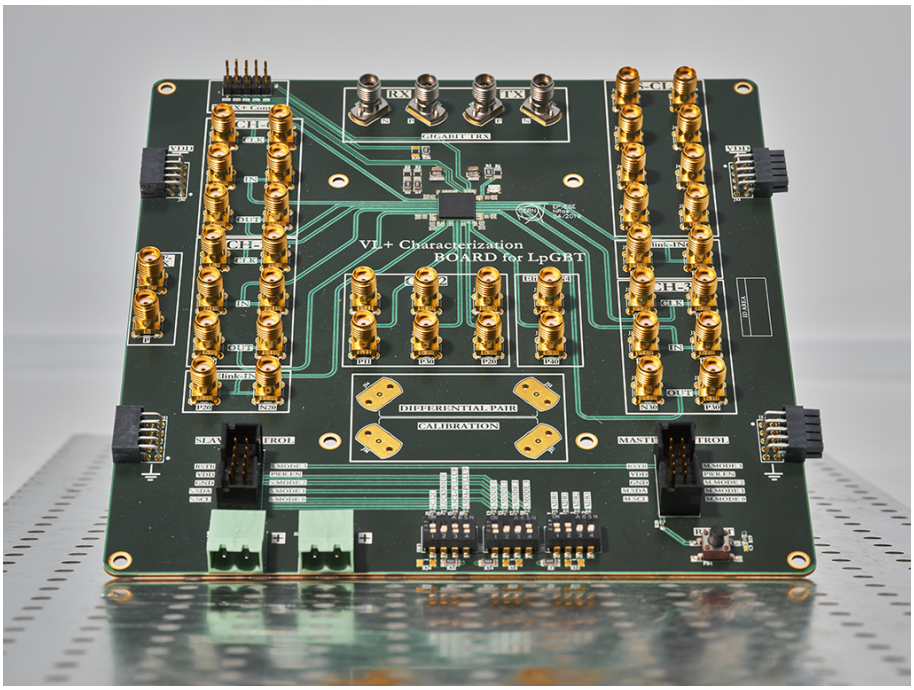

Figure 20: The fully assembled VL+ characterization board.

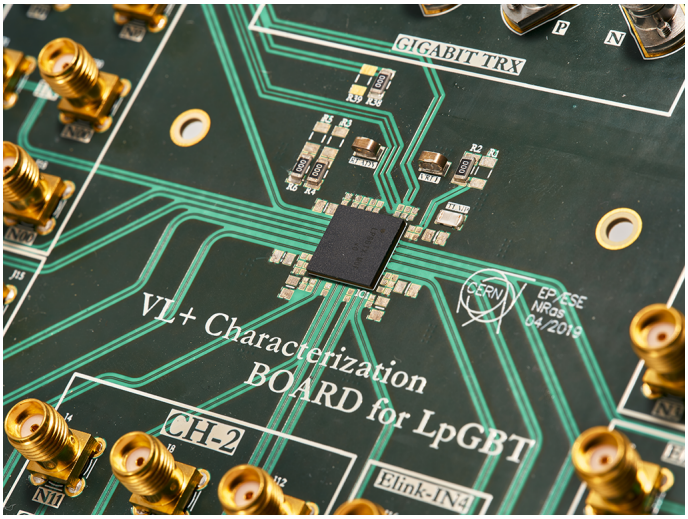

Figure 21: The LpGBT ASIC chip assembled on the VL+ characterization board.

4 Simulation and Measurements

4.1 Signal Integrity

In this section, it will be presented theoretical background on signal integrity in comparison with measured and simulated data of the designed board.

The signal integrity aspects that are covered here are impedance control and impedance matching techniques, transmission line's scattering parameters and eye-diagrams.

4.1.1 S-Parameters

Fundamentally, a behavioral model describes how an interconnects interacts with a precision, incident waveform. When describing in the frequency domain, the precision waveform is, of course, sine wave. However, when describing behaviour in the time domain, the precision waveform can be a step edge or even an impuls waveform. As long as the waveform is well characterized, it can be used to create bahavioral model of the interconnect or device under test, DUT, [7].

In the frequency domain, where sine waves interact with the DUT, the behavioral model is described by the S-parameters. In the time domain, we use labeling scheme of S-parameters, but interpret results differently, [1].

S-parameters can be conveniently measured with a modern VNA (Vector Network Analyser). They also lend themselves well to rapid mathematical manipulation, and thus offer the potential for use in circuit simulations.

S-parameters can be defined for single port or multi port applications, and are therefore suitable for single-ended and differential applications. S-parameters can be mapped directly to parameters such as insertion loss (S21), return loss (S11), and crosstalk (S13, S14), so in theory, they can be used to fully characterize an interconnect path, [4]. The most significant parameters in our application are S11 and SDD11. The first one (S11) shows the return loss along the signal path and the second one (SDD11) was used to calculate differential impedance along the lines, which will be explained later in text.

On the Figure 22 is the graph of S11 parameter on the transmission line obtained from computer simulation. From the graph we can see the level of the return losses and the resonant frequencies. The important parameter here is the return loss and it's value is around $-10\,\mathrm{dB}$, which is good enough for our application.

The Figure 23 shows the graph of the measured S11 parameter of the transmission line on the board. Similar with the simulated data, when measured we obtained return loss of around $-10\,\mathrm{dB}$.

From presented graphs it is visible that simulated data and measured data are very similar and that our board design was done properly. Also the obtained values of S11 parameter show good board characteristic.

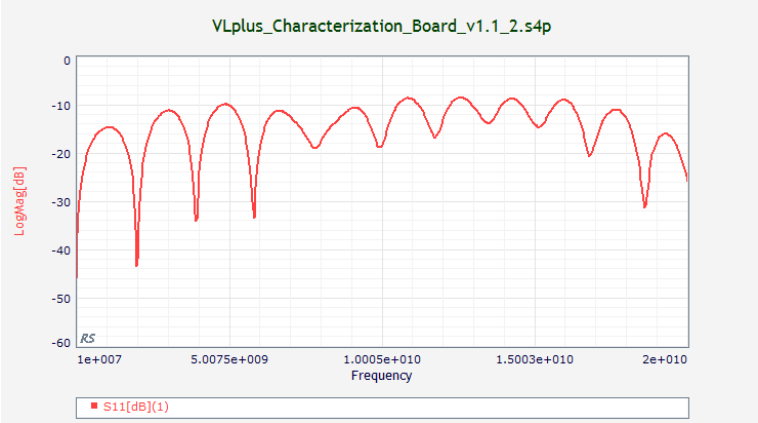

Figure 22: Simulated S11 parameters of the transmission line.

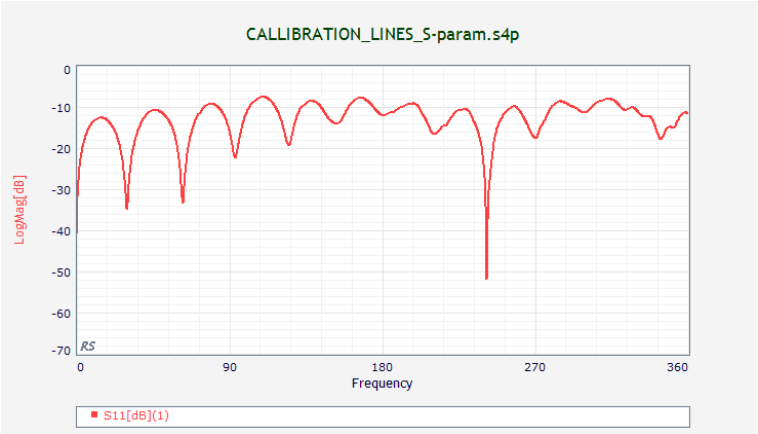

Figure 23: Measured S11 parameters of the transmission line.

4.1.2 Eye Diagrams

Eye patterns are a time domain characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver, and overlaying the received signals upon one another. Over time, the received data builds to resemble an eye. Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to "close." Specifications, such as an eyemask template, can be placed on the amount of open area required in the eye to ensure a functional system.

Eye pattern specifications may be placed on an entire interconnect path, that is, from a transmitter to a receiver. However, when used to evaluate a particular component of that path, say, a single connector, eye patterns fall short. While it is likely that a single component that fails to meet an eye pattern requirement will also cause an entire interconnect path to fail, the converse is not necessarily correct. In other words, a component (or all components in an interconnect path, for that matter) might pass an eye pattern test when tested separately, but a complete path containing that component might not pass the same test, [4].

The Figure 24 shows the measured eye diagrams of transmission line on the VL+ characterization board. The shown diagrams are obtained by generating bit-stream on the LpGBT chip and measuring the signal on the SMA connectors, using

real-time oscilloscope.

We can see that on the shown figure are four eye diagrams measured for different board configurations. Upper row of the eye diagrams are measured for two operating speeds, 5.12 Gbps and 10.24 Gbps, when the decoupling capacitors are placed around the chip, on the same side of the board. The bottom row shows the eye diagrams, also for two mentioned speeds, but when the decoupling capacitors are bellow the chip, on the opposite side of the board. From the shown data, we can see that every configuration gives pretty good response, the eyes are completely open.

The only significant difference is when the board operates on 10.24 Gbps and when the decoupling is around the chip (which is not recommended by the chip designer), the jitter is a little bigger, which can be seen on signal level transition parts, from low to high and from high to low. This situation shows the negative effect when the designers recommendations, regarding the position of the decoupling capacitors are not followed. In our application this does not make problem and effects are minimal, but shows that influence exists and that in some applications may cause the problems.

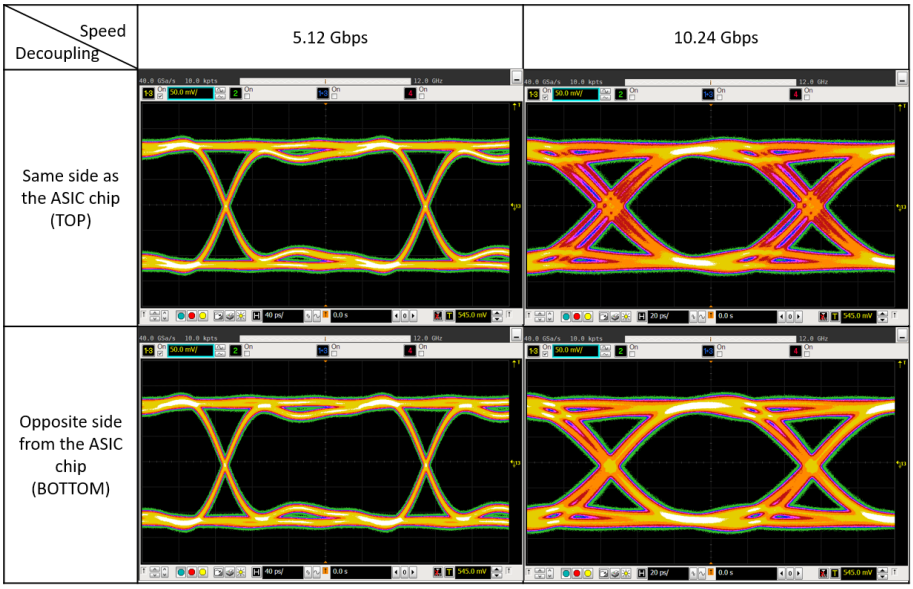

Figure 24: The eye diagrams of the transmission lines by operating speeds and capacitors position.

4.1.3 Transmission Line Impedance

When designing the high speed circuits, one of the important requirements is controlled value of impedance on lines between the circuits. The value of impedance that should be obtained along the lines is determined by input and output impedance of that circuits, usually defined with termination resistors. In our case the value of impedance between the lines in differential pairs, or differential impedance is set to 100 Ω.

The calculation of the exact line impedance value on the PCB board is very difficult because of many variable parameters. Some of the parameters that influence the impedance value are the distance between the lines, the thickness of the dielectric layers above and bellow the lines, the relative permittivities of the dielectrics. Every

configuration of lines has its conventional name, for example microstrip line (Fig. 25) relates to situation when differential lines are above the plane layer, with the dielectric in between and with air above the conductors. Our case is coated edge-coupled microstrip line configuration (Fig. 26), which means that there is solder mask above the conductors instead of air and edge-coupled is related to trapezoidal shape of the lines instead of rectangular shape. Mathematical equations that describe differential impedance calculus, for such a complex configurations are very complicated to derive and they are not available for free, so we used the approximated expressions for basic microstrip lines.

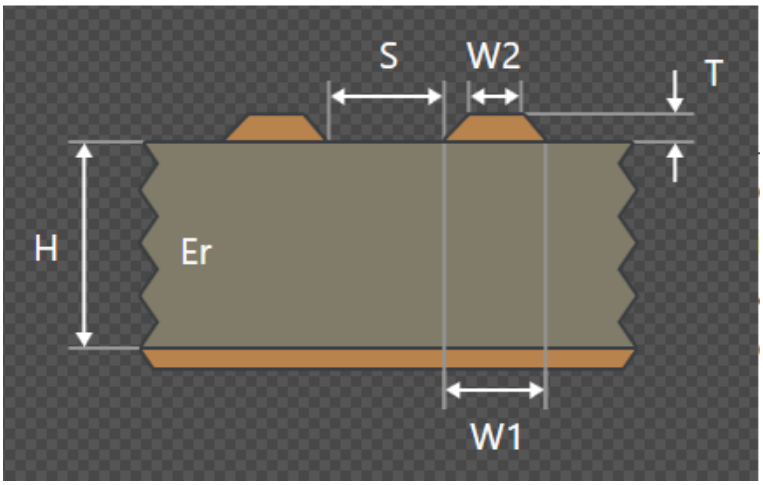

Figure 25: The ende-coupled microstip topology.

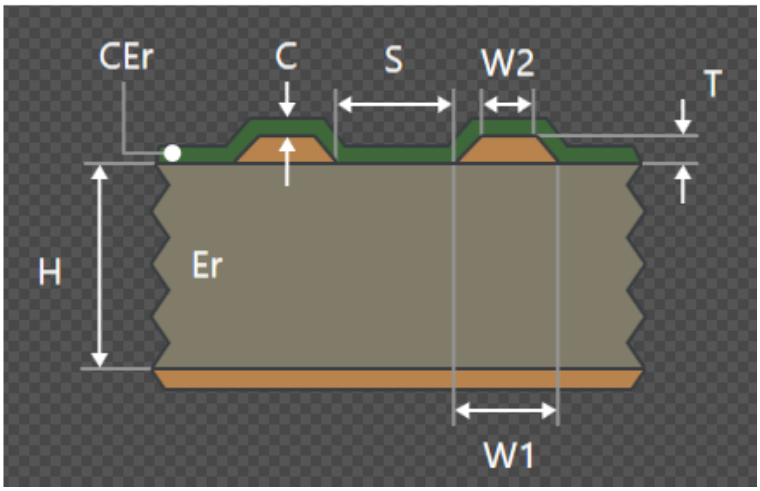

Figure 26: The coated edge-coupled microstip topology.

The equation (1) represents the mathematical formula which describes the value of differential impedance for microstrip line configuration, [9]:

$$Z_d = \frac{174}{\sqrt{\epsilon_r + 1.41}} ln\left(\frac{5.98 \cdot H}{0.8 \cdot W_1 + T}\right)\left(1 - 0.48 \cdot e^{-0.96\frac{S}{H}}\right) \quad (1)$$

Where:
Z_d is the differential impedance,
S is the trace separation,
W_1 is the trace width,
T is the trace thickness,
H is the dielectric thickness and
ϵ_r is the dielectric constant (relative permittivity).

This formula is very complex for calculation when we have a lot of lines, which goes in many different ways around the board, with a lot of obstacles on their path, for example vias. The situation that is also very usual in practice is discontinuities in ground planes, which also influences impedance value.

The Figure 27 represents the graph, obtained using computer simulation, which shows the value of the differential impedance along the transmission line. All the influences on the impedance value, that are described before in text, are now visible on this graph. On the very beginning we can see that impedance value rises for about 20 % of nominal value, which is caused by SMA connectors and single-ended part of the traces after the connectors. Next section is part where the differential pair is properly coupled, but here we have also mismatch of about 5 % and this is most likely caused by software tool. The final section on the shown graph is part when the signal passes trough five vias, and we can see the great mismatch of almost 50 % and we can not avoid that.

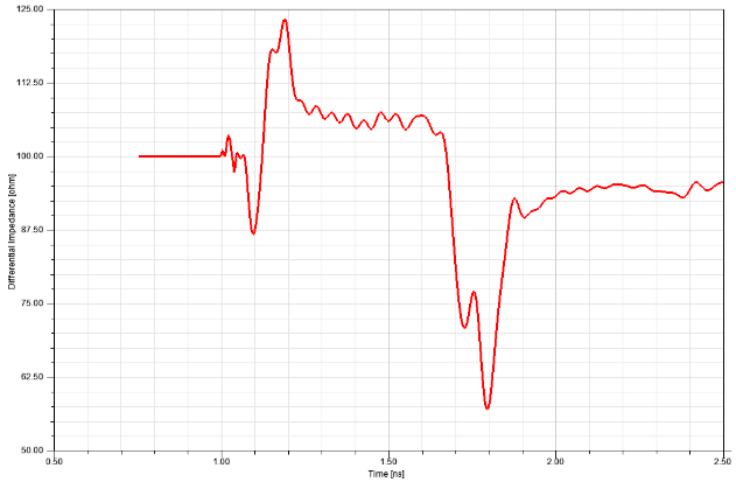

Figure 27: Simulated differential impedance value along the high-speed link transmission line.

The Figure 28 shows the measured differential impedance of the transmission line, obtained from measured SDD11 parameter, previously explained. From the shown graph we can see that there is not much difference in the simulated and measured data. The significant difference is the value of the impedance along the properly coupled part of the differential pair, which measured value is 110 Ω, comparing to 105 Ω obtained from simulation. The other part where the difference between measured and simulated value is significant is part where the signal goes trough a lot of vias, where the measured impedance value is 80 Ω, comparing to the simulated value of 60 Ω.

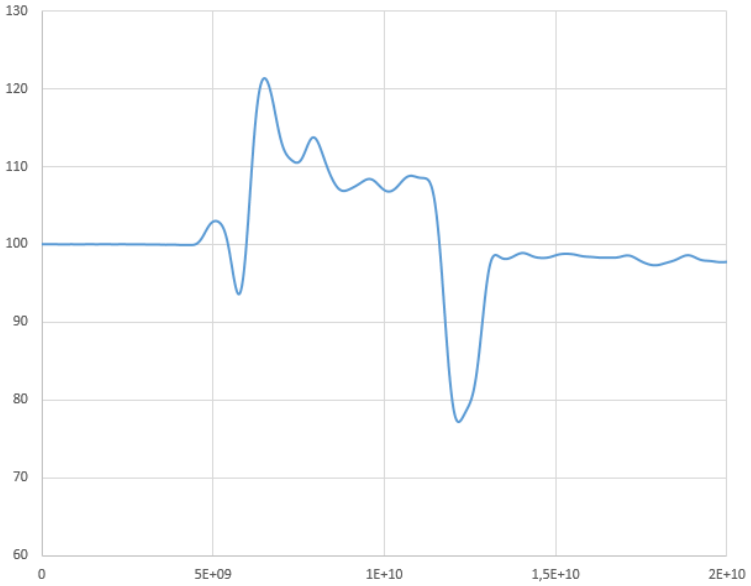

Figure 28: Measured differential impedance value along the high-speed link transmission line.

4.2 Power Integrity

The power integrity of the electrical components describes the behaviour of signals on the power lines depending on the different operating conditions. The most basic aspects of power integrity will be covered in this section.

4.2.1 Voltage Drop

One of the important characteristics when designing the printed circuit boards is the voltage drop along the power and ground lines. It describes the value of the voltage that will be lost from the source to the consumer. This value should be kept as low as possible, especially in the applications with low voltage power supplies, as it the case also in this application.

The Figure 29 shows the voltage drop on the power line (VDD), along the power plane, that is obtained using computer simulation. From the color map beside the board it is visible that maximum voltage drop is 0.3 mV, which is negligibly low.

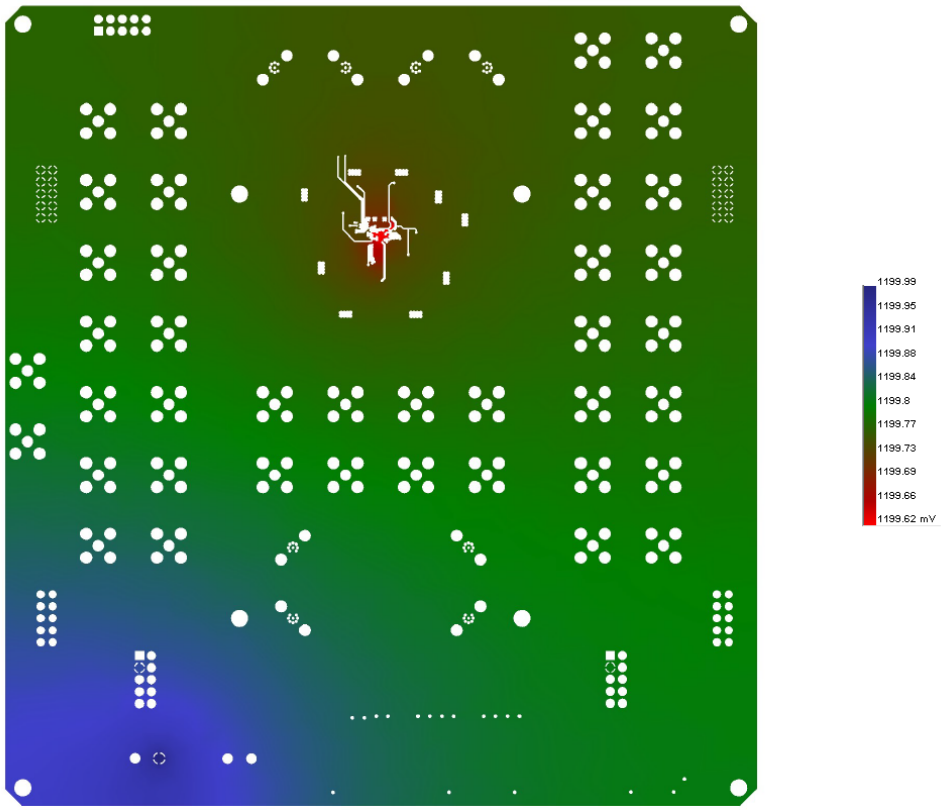

Figure 29: The voltage drop on the power line.

On the Figure 30 is depicted the voltage drop on the ground line (*GND*), which is also obtained using computer simulations. The shown figure shows that the voltage drop on the ground plane is also negligibly small with value of 0.6 mV.

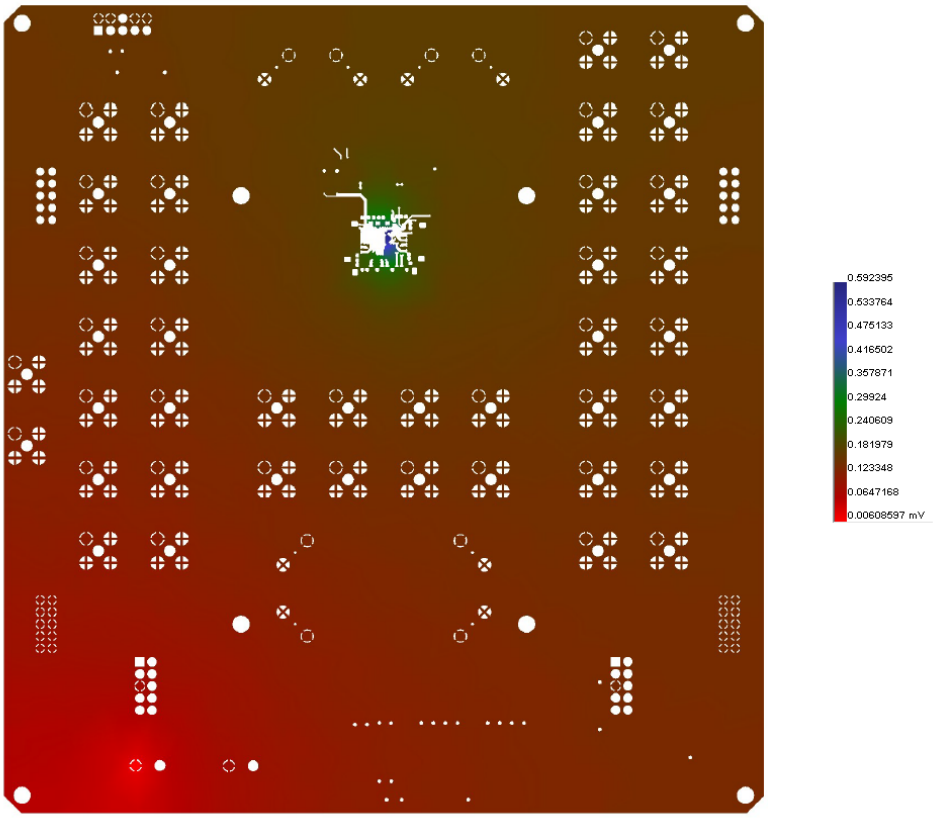

Figure 30: The voltage drop on the ground line.

4.2.2 Decoupling

The importance of the decoupling capacitors in the circuits was explained in previous sections. In this section will be covered the procedure on how to determine good values of the decoupling capacitors. Also to have a look on the response of the capacitors on the VL+ characterization board, obtained using computer simulation, for different configurations.

To determine the value of the decoupling capacitors, first we need to know the response of the bare board and chip. After that we need to choose the capacitors that will attenuate the impedance value on resonant frequencies, which are critical for our design. Every capacitor has it's frequency response characteristic, which shows the dependence of the capacitor's impedance in relation to the frequency. By combining different types of the capacitors with different values, we can obtain the flat response, that has no resonances.

In our application, we did not calculate the capacitors from the beginning, because the LpGBT chip is used also in other applications, where the decoupling capacitors are properly determined, so we used the same values. The reason for measuring the decoupling response on the VL+ characterization board is to see the difference for two different options and to conclude the possible usages of the chip.

The Figure 31 shows the response of the decoupling capacitors when they are placed around the chip, on the same layer. We can see the existence of one peak in impedance value at around 15 MHz. This peak is not critical because the impedance value stays low at maximum value of about 25 mΩ, which is acceptable. The oscillations that appear after 100 MHz are caused by simulation software and can not be taken into consideration.

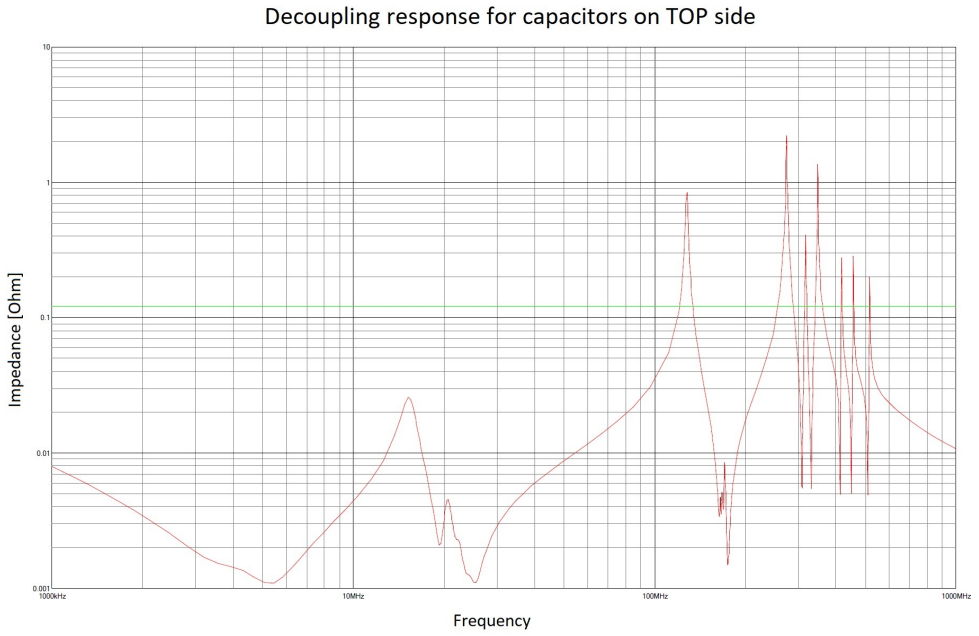

Figure 31: The frequency response of the decoupling capacitors when placed around the chip.

The following Figure 32 shows the simulated response of the decoupling capacitors, but for variant when the capacitors are placed bellow the chip, as it is recommended by the chip designer. Here we can see that resonance peak at about 15 MHz disappeared and now the impedance value is more less stable, with small oscillations. The value of the impedance never goes over 8 mΩ, which is a pretty good value for the LpGBT chip.

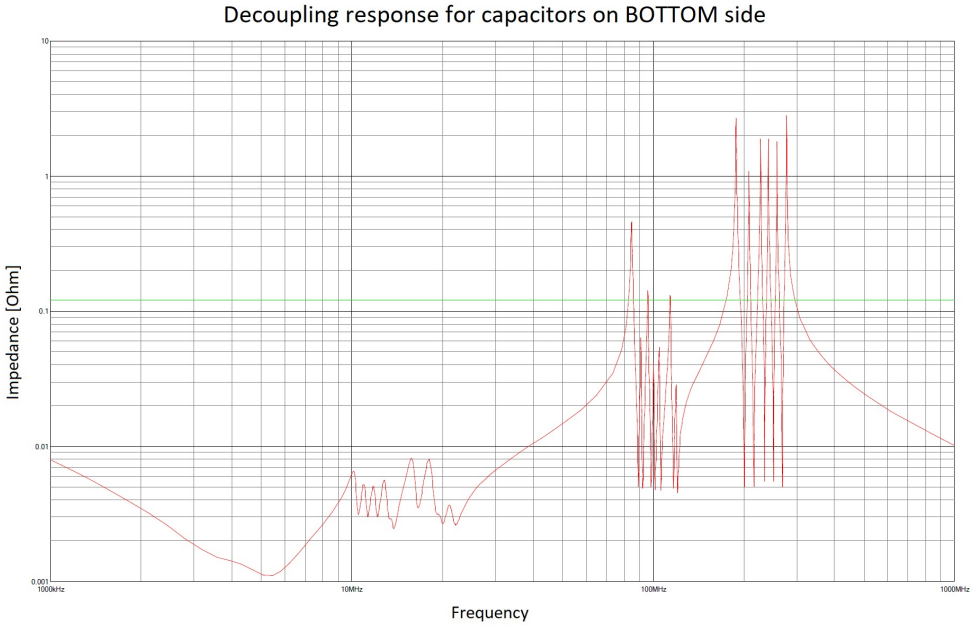

Figure 32: The frequency response of the decoupling capacitors when placed bellow the chip.

After we compare obtained results, the difference when using two variants for the decoupling capacitors position is significant. When we take a look back on the other measurements we can see that this does not affect the chip functionality a lot and it means that this difference is acceptable.

5 Conclusion

This thesis gives an overview of the basic functionalities of the LpGBT chip as well as the requirements that must be met when implementing it in a real application.

The main goal was testing the performances and characterization of the LpGBT ASIC chip. Also defining a reference design for future applications containing this chip. The VL+ characterization board provides simple, easy to use LpGBT testing environment.

There was a lot of difficulties in design process for many reasons, such as the chip package size, number of impedance controlled differential and single-ended lines that needed to be routed in a narrow space. Restrictions regarding types of vias made a lot of problems and they are the main source of bad influence on the characteristics and functionality of the chip. The operating speeds were also a special topic for consideration, because at these speeds many side effects on the board come to the fore, to which special attention must be paid.

After designing and making the working hardware, following the chip designer recommendations and combining with the user necessities, we got the results which describe the behaviour of the LpGBT chip under different working conditions.

The simulated and measured data gave us an overview of expected and obtained results. The S-parameters, eye diagrams, impedance measurements, voltage drop and decoupling response results led us to conclusion that obtained chip characteristics are not ideal, but very close to expected. At the end of the day VL+ characterization board represents the design that provides good working environment for the LpGBT chip and it's design can be used in future applications as a reference design.

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