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RD53 analog front-end processors for the ATLAS and CMS experiments at the High-Luminosity LHC

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PoS(Vertex2019)021

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This work discusses the design and the main results relevant to the characterization of analog front-end processors in view of their operation in the pixel detector readout chips of ATLAS and CMS at the High-Luminosity LHC. The front-end channels presented in this paper are part of RD53A, a large scale demonstrator designed in a 65 nm CMOS technology by the RD53 collaboration. The collaboration is now developing the full-sized readout chips for the actual experiments. Some details on the improvements implemented in the analog front-ends are provided in the paper.

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PoS(Vertex2019)021

1. Introduction

The Phase-II upgrades of ATLAS and CMS will require a complete new tracker with readout electronics facing striking requirements on particle rates and radiation hardness. The design of new pixel readout chips is being tackled in the framework of the RD53 collaboration [1], [2] using a 65 nm CMOS technology. The collaboration's goals, besides the development of the production chips for the high-luminosity upgrades of the experiments, include the detailed understanding of the radiation effects taking place at the 65 nm CMOS node [3], [4] and the design of a shared rad-hard IPs library.

The efforts of the collaboration led to the submission, in 2017, of RD53A, a large scale demonstrator chip integrating a 400×192 pixels matrix. The chip includes a number of design variations, among which three different analog front-ends and two digital readout architectures, to allow for detailed performance comparisons. The RD53A chip has been thoroughly investigated during the last two years, and the three analog front-ends underwent a detailed review process in view of their integration in the production chips.

The design of the final chips is being carried out by the collaboration in a common design framework called RD53B, with two submissions, one for the ATLAS chip and the other for the CMS one, planned for November 2019 and April 2020, respectively.

2. RD53A analog front-ends

RD53A chip is mainly conceived to demonstrate in a large format IC the suitability of the chosen 65 nm technology for the HL-LHC upgrades of ATLAS and CMS in terms of radiation tolerance, stable low threshold operation and high hit and trigger rate capabilities. The main specifications of the chip are shown in Table 1. The chip includes a 400×192 pixels matrix with a pitch of 50 μm×50 μm and features, approximately, half the size of the production chips. The periphery is placed at the bottom of the chip and includes the circuitry needed to bias, configure, monitor and read out the matrix: the analog building blocks are integrated in a macroblock called analog chip bottom surrounded by the logic blocks, grouped in the so-called digital chip bottom. The wire bonding pads are organized as a single row at the bottom chip edge. A row of test pads, conceived for debugging purposes, is also integrated in the top region of the chip. RD53A is designed to op-

Table 1: Main specifications of RD53A chip [5].

Specification	Value	Comments
Hit rate	3 GHz/cm^2	-
Trigger rate	1 MHz max	-
Trigger latency	12.5 μs	-
Hit loss	< 1%	at max hit rate
Detection threshold	< 600 e$^-$	-
In-time threshold	< 1200 e$^-$	-
Noise occupancy per pixel	$< 10^{-6}$	50 fF load; in a 25 ns interval
Radiation tolerance (TID)	500 Mrad (1×10^{16}1 Mev eq. n/cm^2)	replacement after ∼5 years operation

PoS(Vertex2019)021

erate with serial powering and integrates shunt LDOs [6] already dimensioned for the production chip.

The RD53A matrix is divided into 3 regions featuring different analog front-ends, called synchronous (128 matrix columns), linear (136 columns) and differential (136 columns), sharing the general architecture shown in Fig. 1. The three front-ends feature a charge sensitive amplifier (CSA) connected to a threshold discriminator whose output drives a time-over-threshold (ToT) counter used for the analog-to-digital conversion of the signals. In RD53A the ToT is run at 40 MHz and provides 4 bits for digitization.

The synchronous front-end (SYNC) integrates a CSA with Krummenacher feedback [7] which provides, on one hand, a linear discharge of the CSA feedback capacitance and, on the other hand, a compact solution to cope with the large radiation-induced increase in the detector leakage current. A synchronous discriminator is AC-coupled to the preamplifier and includes an offset compensated differential amplifier and a positive feedback latch. The SYNC front-end does not require any in-pixel DAC for local threshold adjustment, since tuning is performed by means of autozeroing. The SYNC can be operated in a fast ToT counting mode in which the latch is turned into a local oscillator running at up to 900 MHz.

The linear front-end (LIN) features a Krummenacher feedback preamplifier DC-coupled to a current comparator. The latter consists of a transconductance stage followed by a Träff amplifier [8] with low input impedance. Threshold tuning is performed by means of a 4-bit in-pixel current DAC based on a binary weighted architecture.

The differential front-end (DIFF) includes a continuous reset integrator with DC-coupled pre-comparator stage and a fully differential input comparator. The CSA stage integrates a constant current feedback capable of preventing the input from saturating in the presence of detector leakage currents of the order of few nanoamps. For larger currents, a leakage current compensation circuit, similar to the one integrated in the FEI4 chip [9], can be enabled. Local tuning of the threshold is performed by exploiting one 4-bit resistor ladder in each pre-comparator branch, resulting in an effective 5-bit adjustment.

Common to all front-ends is the calibration injection circuit, which makes it possible both to gen-

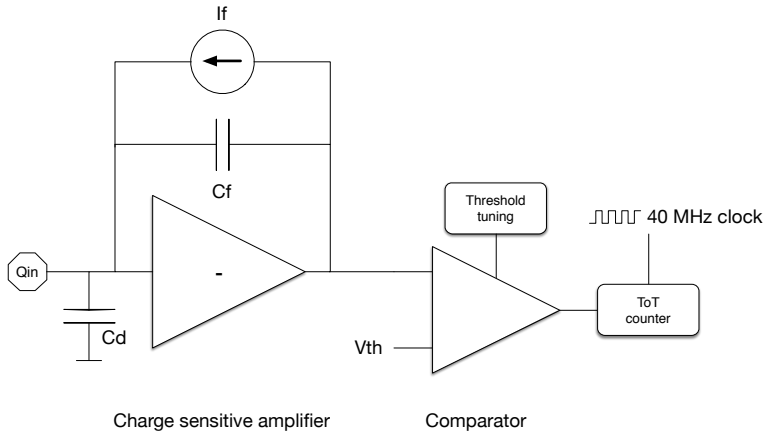

Figure 1: RD53A front-end architecture.

PoS(Vertex2019)021

erate two consecutive signals with the same polarity and to inject a different amount of charge in neighbouring pixels at the same time. The three front-end designs feature approximately the same layout area and bump bond pads, making them easily interchangeable on the pixel matrix layout. The bias distribution follows the same organization for all three front-end flavours. Further details on the analog front-ends integrated in RD53A can be found in [10], [11], [12].

3. Test results

In view of the integration of the analog front-ends in the production chips, an extensive testing campaign has been carried out within the RD53, CMS and ATLAS communities. Among RD53A specifications, reported in Table 1, noise occupancy requirements set severe constraints on both noise and threshold dispersion performance of the analog front-ends. Equivalent noise charge (ENC) and threshold dispersion have been measured for bare chips and assemblies. In particular, tests have been performed on readout chip connected to 50 μm $\times$ 50 μm and 100 μm $\times$ 25 μm planar sensors. Measured ENCs are in general below 100 electrons r.m.s., except for the synchronous front-end assemblies, featuring an average ENC close to 120 electrons r.m.s. [13]. The noise occupancy of the three RD53A front-ends is shown in Fig. 2 as a function of the per-pixel analog current consumption. Data reported in the figure are relevant to front-ends connected to 100 μm $\times$ 25 μm planar sensors with a threshold set to 1200 electrons. The differential front-end features excellent noise performance, even at low current consumption. The linear and the synchronous front-ends have to be operated with larger currents, 3.5 μA and 4.5 μA respectively, in order not to exceed the 10^{-6} noise occupancy specification.

At the HL-LHC, with its 25 ns bunch structure, the so-called in-time threshold is a key parameter. The absolute threshold does not depend on timing, and is defined as the input charge signal having a 50% probability of firing the discriminator. On the other hand, in-time threshold strongly depends on timing, and represents the minimum input signal that can be detected in the correct bunch crossing. Notice that, in general, a lower absolute threshold could be needed in order to achieve a given in-time threshold. A parameter called overdrive can thus be introduced, being simply the difference between the in-time and the absolute threshold. A 1200 e^- minimum in-time threshold

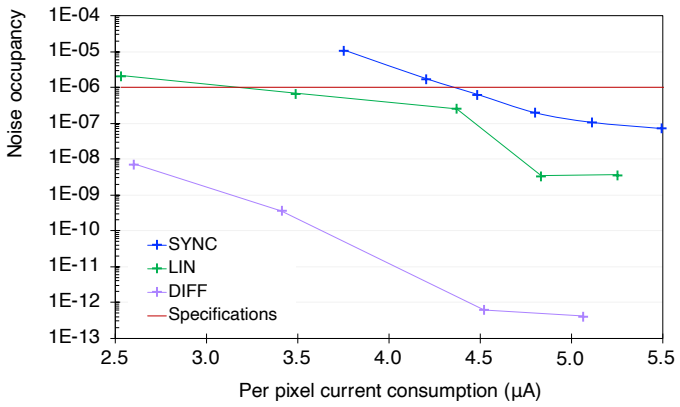

Figure 2: Pixel noise occupancy as a function of the per-pixel analog current consumption.

PoS(Vertex2019)021

Table 2: Overdrive (in e^-) for bare chips and assemblies tuned to 1000 and 1200 e^- in-time threshold.

	SYNC	LIN	DIFF
bare chip	0	147	17
bare irradiated 500 Mrad	1	146	33
50x50 μm^2 sensor	0	341	-
100x25 μm^2 sensor	0	293	36

specification has been set for RD53A, with a maximum overdrive of 600 e^-. Table 2 shows the overdrive of bare chips (also after X-ray irradiation with a total ionizing dose (TID) of 500 Mrad) tuned to an in-time threshold of 1000 e^- and of assemblies tuned to 1200 e^-. All the front-ends connected to sensors can be operated with an in-time threshold of 1200 electrons, with the LIN featuring the largest overdrive and the SYNC an overdrive close to zero, thanks to the synchronous structure of its comparator.

The radiation hardness properties of the RD53A chip have been thoroughly investigated in several irradiation campaigns during which the analog front-ends have been exposed to TIDs up to 1 Grad. In general, no major degradations in analog performance were detected after irradiation at temperatures compatible to the ones in use in the actual experiments, with all the three front-ends able to operate at low thresholds even at 1 Grad TID. As an example, Fig. 3 shows the ENC as a function of the pixel analog current consumption for different TIDs (200, 300 and 500 Mrad). Irradiation was performed with X-rays at cold, with RD53A powered on and read out continuously. No significant effects are detectable on the noise performance of the front-ends after irradiation [14].

4. RD53B developments on analog front-ends

RD53A, with the very promising results emerged from its characterization, is out of doubt one of the most important milestones toward the development of the final chips for ATLAS and CMS, being developed in a common design framework called RD53B. The production chips will include all the RD53A elements with bug fixes and, where needed, technical improvements. A number of additional features will be implemented in RD53B designs [15], such as dedicated bias of edge and top pixels of the matrix, triple modular redundancy for pixel configuration and optimized data formatting and compression, just to name a few.

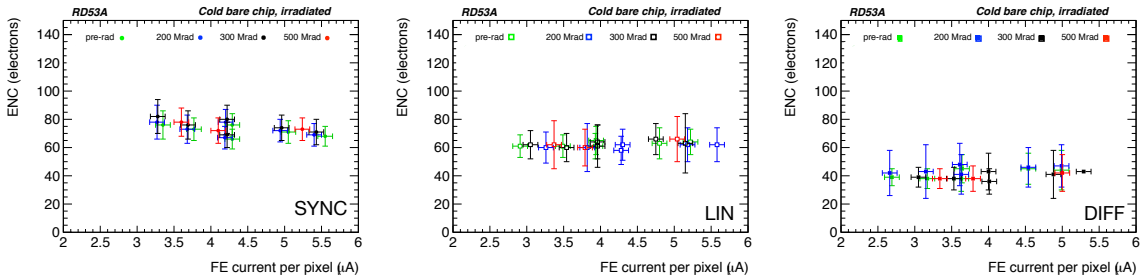

Figure 3: ENC as a function of the pixel analog current consumption for different TIDs.

PoS(Vertex2019)021

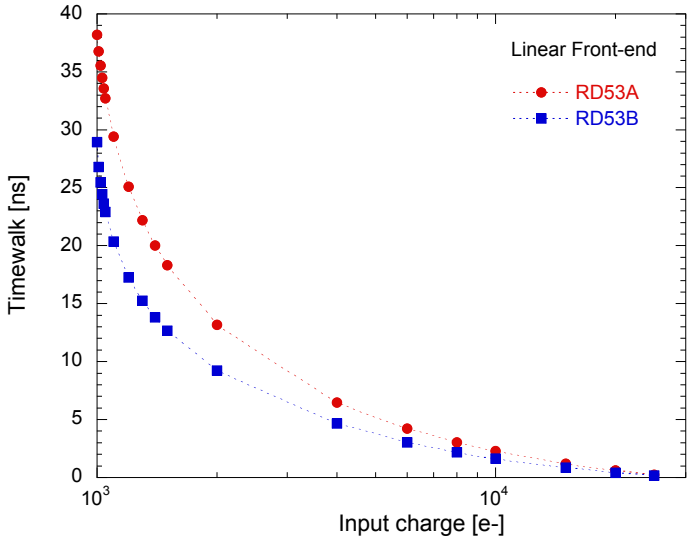

Figure 4: Time-walk as a function of input charge for the RD53A and RD53B versions of the linear front-end

After a detailed review process, the two experiments made their choice for the analog front-end integration in the production chips: the differential front-end will be integrated in the ATLAS chip, whereas the linear will be operated in CMS. The ATLAS choice was mainly driven by the excellent noise occupancy performance of the differential front-end, achieved even at rather low current consumption. On the other hand, the linear front-end has been recommended by the review committee as the lowest risk option for the integration in the production chips. Moreover, CMS requires a fast preamplifier return to baseline, with a target discharge rate of 3000 e^-/25 ns which is at the limit for the DIFF, but which the LIN can accomplish with some margin. These arguments, along with the capability of the linear front-end to cope with large detector leakage currents, drove the CMS choice [13].

In the RD53B framework, a number of improvements of the analog front-ends are being implemented according to reviewers' comments and to experiment requirements. As far as the LIN is concerned, a weak point that emerged from the test campaign is its large overdrive. In RD53B, a partial re-design of the comparator transimpedance stage led to significant improvements of the time-walk performance of the front-end. It is worth mentioning that time-walk is strictly related to the overdrive and is defined, for a given input charge signal, as the difference between the time needed to fire the discriminator in response to that specific input signal and the one needed for an arbitrarily large signal. The improvement is clearly visible in Fig. 4, which shows the time-walk as a function of the input charge for the RD53A and RD53B versions of the linear front-end. The RD53B LIN will also include an improved, 5-bit threshold tuning DAC to reduce channel-to-channel dispersion of the threshold.

An issue related to the differential front-end is a large and systematic ToT dispersion, detected in the initial testing of the RD53A DIFF. Such a dispersion is actually due to a missing "place & route" constraint at the front-end output in the basic building block of the matrix, called core (a region of 8×8 pixels). This, in turn, translated to varying load capacitances on the comparator outputs across

PoS(Vertex2019)021

the core and, ultimately, in a systematic variation of the ToT. The issue has been easily fixed in RD53B by pre-placing and pre-routing digital buffers at the comparator outputs in the matrix core. For the differential front-end a pixel by pixel variation of the hit signal edges has been also detected [14] (the hit signal being the digital signal toggling for an input signal crossing the threshold). Such a digital signal is triggered, in the RD53A version of the DIFF, by the comparator output falling edge which features a very low slew rate, resulting in a large dispersion of the hit leading edge. In RD53B the hit signal will be triggered by the faster rising edge of the comparator output, making the timing dispersion of the RD53B DIFF comparable to the dispersion measured for the linear front-end.

5. Conclusion

Future pixel detectors at the High-Luminosity LHC require a new generation of readout chips complying with tough requirements in terms of speed, noise, power consumption and radiation hardness. The design of such advanced chips is being tackled in the framework of the RD53 collaboration using a 65 nm CMOS technology. The collaboration submitted the RD53A demonstrator, a large scale chip that has been thoroughly characterized during the last two years, with very promising results. Three analog front-end flavours, called synchronous, linear and differential, were integrated in RD53A. The main analog performance has been assessed for each analog front-end. Very good noise properties, retained also after irradiation with X-rays for TIDs up to 1 Grad, have been obtained, in particular for the differential front-end. The success of RD53A is the baseline for the design of the pixel readout chips of CMS and ATLAS at the HL-LHC, being designed in a common framework called RD53B. ATLAS and CMS chips are planned to be submitted in November 2019 and April 2020 respectively, as implementations of the RD53B design, with the ATLAS chip featuring the differential front-end and the CMS integrating the linear front-end.

6. Acknowledgement

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PoS(Vertex2019)021