

Silicon vertex and tracking detector R&D for CLIC

Katharina Dort^{a,b,*} on behalf of the CLICdp Collaboration

^a CERN,

Espl. des Particules 1, 1211 Meyrin, Switzerland

^b *Experimental Physics II, University of Giessen,*

Ludwigstr. 23, 35390 Giessen, Germany

E-mail: katharina.dort@cern.ch

The physics aims at the proposed future high-energy linear e+e- collider CLIC pose challenging demands on the performance of the detector system. In particular, the vertex and tracking detectors have to combine a spatial resolution of a few micrometres and a low material budget with a time-stamping accuracy of a few nanoseconds. For the vertex detector, fine-pitch sensors, dedicated 65nm readout ASICs, fine-pitch bonding techniques using solder bumps or anisotropic conductive films as well as monolithic devices based on Silicon-On-Insulator technology are explored. Fully monolithic CMOS sensors with large and small collection electrodes are under investigation for the large surface CLIC tracker. This contribution gives an overview of the CLIC vertex and tracking detector R&D, focusing on recent results from test-beam campaigns and simulation-based sensor optimisation studies.

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*Speaker

1. Introduction

The Compact Linear Collider (CLIC) [1] is a concept for a future linear electron-positron collider to be built at CERN. It is proposed to be constructed in three centre-of-mass energy stages ranging from 380 GeV to 3 GeV. The principle physics objectives of CLIC revolve around Standard Model top quark and precision Higgs physics as well as searches for Physics Beyond the Standard Model [1].

2. Detector requirements

The physics-driven requirements and experimental conditions at CLIC pose challenging requirements on the detector system [2]. A hit time tagging resolution of ~ 5 ns is required to mitigate the impact of beam-induced background. Additionally, a single-plane spatial resolution of < 3 μm for the vertex detector and < 7 μm for the tracker, and a low mass constraint of $\sim 0.2\%X_0$ per layer for the vertex and $\sim 1 - 2\%X_0$ for the tracking detector are needed to comply with the required measurement accuracy. An average power dissipation of < 50 mW/cm² for the vertex is required for forced air cooling. The leak-less water cooling system foreseen for the tracker allows for an average power dissipation of < 150 mW/cm². The hit detection efficiency for both vertex and tracking detector should exceed 99.5 %.

3. Hybrid Pixel Detectors

A small pixel pitch of ≤ 25 μm is required to limit the occupancy in the vertex detector to a few percent. Hybrid pixel detector technologies, separating the readout circuit from the sensitive volume, are capable of incorporating complex functionalities in a small pixel volume. Different technologies for readout ASICs and sensors are therefore under investigation for the CLIC vertex detector.

To this end, a 65 nm CMOS process readout chip, the CLICpix2, has been designed with a pixel pitch of 25 $\mu\text{m} \times 25$ μm [3]. CLICpix2 ASICs have been solder bump-bonded to planar silicon sensors of various thicknesses ranging from 50 μm to 150 μm . The chip features an active matrix of 128×128 pixels and provides simultaneous 8-bit *Time of Arrival (ToA)* and 5-bit *Time over Threshold (ToT)* measurement.

A single-chip bump-bonding process for CLICpix2 ASICs has been studied. The interconnect yield of the fine-pitch bump bonding was tested extensively in laboratory measurements and a yield of up to 97.9% was found [4].

Moreover, CLICpix2 assemblies have been tested in various test-beam campaigns and a spatial resolution of down to 3.2 μm was found for a sensor thickness of 130 μm . For sensors sufficiently thin to comply with the vertex requirements on material budget, the spatial resolution degrades since charge sharing is not sufficient. Therefore, innovative sensor concepts with enhanced charge sharing in the sensor layer are under investigation [5].

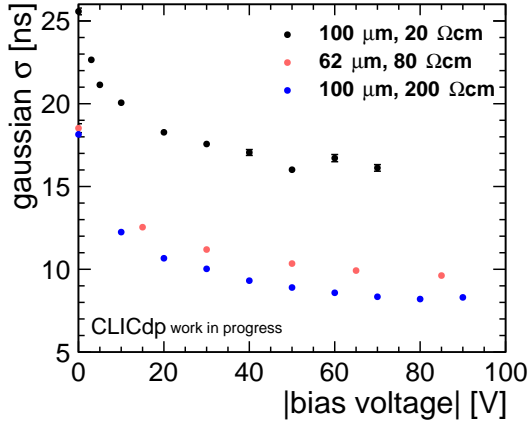


Figure 1: Timing resolution as a function of bias voltage for ATLASpix_Simple assemblies with various resistivities.

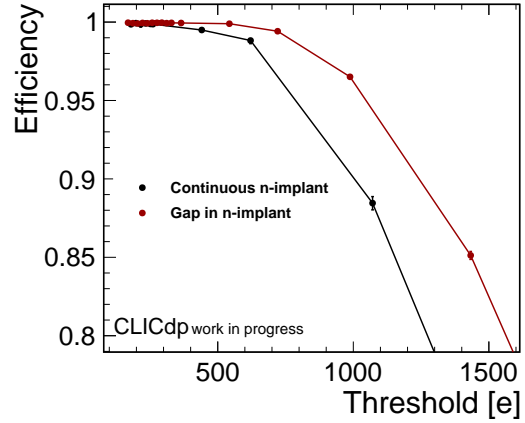


Figure 2: Hit detection efficiency as a function of detection threshold for the two CLICTD process variants with and without gap in the n-implant.

4. Monolithic Pixel Detectors

In monolithic pixel detectors, the electronics circuits are integrated in the sensitive volume of the detector. This design allows to reduce the material budget and avoids the challenge of fine-pitch hybridization. These advantages and their large-scale production capabilities, make monolithic sensors attractive candidates for the large-area CLIC tracker. However, as the electronics needs to be shielded from the high voltage applied to the sensor, it is placed in deep wells. In *High Voltage CMOS sensors (HV-CMOS)*, the circuitry is placed inside the collection electrode. With this design, high voltages can be applied. As a result, a large depletion zone and a high electric field are present in the sensing volume, which guarantee a fast charge collection via drift. However, the large collection electrode leads to a comparatively high sensor capacitance. It is beneficial to minimise the capacitance in order to profit from a lower power consumption, lower threshold and reduced noise level as well as an increased signal. In the *High Resistivity CMOS (HR-CMOS)* design, the electronics is placed in wells separated from the collection electrode. This allows to reduce the size of the collection electrode leading to a reduced sensor capacitance.

4.1 High-Voltage CMOS sensors

The ATLASpix_Simple monolithic HV-CMOS test chip is produced in a commercial 180 nm HV-CMOS process and features an active matrix of 25 columns and 400 rows of elongated pixels with a pitch of $130\ \mu\text{m} \times 40\ \mu\text{m}$ [6]. Each pixel records 10-bit ToA and 6-bit ToT information. The readout is realised in a data-driven column-drain scheme.

ATLASpix_Simple assemblies with wafer resistivities between $20\ \Omega\text{cm}$ and $200\ \Omega\text{cm}$ were studied in test-beam campaigns at the DESY II test beam facility [7]. The timing resolution as a function of bias voltage for three different resistivities is depicted in Fig. 1 [8]. The timing improves with increasing bias voltage and larger resistivity. The higher bias and larger resistivity generate a larger depleted volume from which fast charge collection via drift is possible. Moreover, a higher electric field is present in the sensor providing an additional acceleration in charge collection.

A hit detection efficiency well above 99.5 % has been measured. While the efficiency decreases with increasing threshold, it has been shown that a larger resistivity and a higher bias voltage extend the efficient operation window [8]. The larger depleted volume, giving rise to a higher signal, is the reason for the better performance.

A spatial resolution of $11.3\ \mu\text{m}$ has been measured in $r\Phi$ -direction. The spatial resolution is determined by the binary resolution ($\text{pitch} / \sqrt{12}$) since there is little charge sharing between neighbouring pixel cells. To improve the spatial resolution, the pixel layout has been adapted in a new test-chip based on the ATLASpix_Simple design. The chip is currently under investigation.

4.2 High-Resistivity CMOS sensors

The CLICTD chip is fabricated in a modified 180 nm CMOS imaging process. It features a matrix of 16×128 readout channels with a pitch of $300\ \mu\text{m} \times 30\ \mu\text{m}$. Each channel is segmented into eight $37.5\ \mu\text{m} \times 30\ \mu\text{m}$ sub-pixels with a dedicated analogue front-end. The sub-pixel comparator outputs are combined through a logical *OR* in the digital front-end of a channel, which provides an 8-bit ToA and 5-bit ToT measurement. The bit pattern of sub-pixel hits is stored as well. This readout architecture allows to reduce the digital logic while maintaining prompt charge collection [9].

The sensor consists of a $30\ \mu\text{m}$ high resistivity epitaxial layer in which full lateral depletion can be achieved owing to the introduction of an n-type implant below the collection diode [10]. CLICTD was fabricated in two sensor process variants, one featuring a continuous n-implant and the second one with a gap in the n-implant. The gap in the n-implant provides accelerated charge collection leading to an improved timing resolution and reduced charge sharing [11]. As charge sharing is desired in the $r\Phi$ -dimension of the detector to improve spatial resolution, the gap is only introduced in the perpendicular dimension, which corresponds to the direction along the $300\ \mu\text{m}$ pitch.

In test-beam campaigns at the DESY II test-beam facility, the spatial resolution of the detector in the $r\Phi$ -dimension was found to be $4.6\ \mu\text{m}$ and the timing resolution $5.8\ \text{ns}$ for the design with continuous n-layer. The efficiency of the chip is $> 99\%$ up to a threshold of $\sim 450\ \text{e}$, as illustrated in Fig. 2. The loss in efficiency for higher threshold values is less severe for the process with gap in the n-implant owing to the reduced charge sharing, which gives rise to a higher seed signal. The larger efficient operation window is essential for future detectors in 65 nm CMOS design in order to compensate for the reduced amount of charge generated in the thin sensors required for this technology.

The sensor design of CLICTD was optimised in 3D TCAD simulations. For verification, the response of the sensor to a particle beam was studied in a combination of Monte Carlo (MC) and electrostatic TCAD simulations. For this purpose, electrostatic sensor simulations in 3D TCAD were imported into the Geant4-based MC framework Allpix² [12], thereby harnessing the full potential of the accurate sensor modelling in TCAD and the high statistics thanks to the MC approach [13].

The threshold crossing time of the simulated pulses within a pixel cell is depicted in Fig. 3 for both process variants. For the process without the gap, the sensor timing resolution degrades towards the pixel edges and particularly towards the pixel corners due to the increased charge collection time. The gap, introduced at very low and high x-values in the pixel cell shown on the right of Fig. 3, compensates for this sensor timing degradation by providing accelerated charge collection

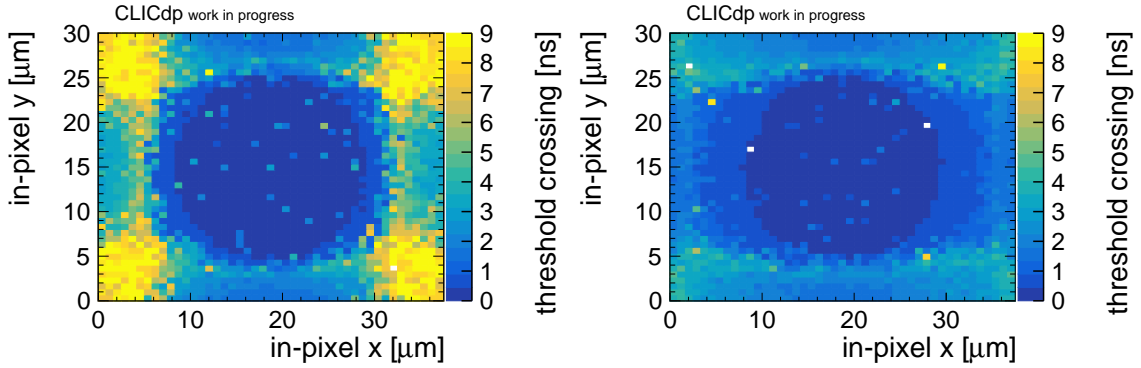


Figure 3: Simulated in-pixel threshold crossing time for the CLICTD process with continuous n-implant (left) and gap in the implant (right).

along the x-dimension. As a result, the threshold crossing time is improved and more homogeneous across the pixel cell. In the test-beam measurements, the timing resolution of CLICTD is limited by the sensor front-end circuits. Differences in timing resolution between the two process variants are therefore overshadowed by the front-end response.

The average power consumption for CLICTD has been estimated from simulations and static power consumption measurements. For the periphery, the average power consumption is 49 mW and for the pixel matrix 5.7 mW/cm^2 , which is well in line with the CLIC tracking detector requirements [9].

5. Summary and Outlook

A broad R&D programme is being pursued to meet the demanding requirements imposed on the vertex and tracking detectors for CLIC. For the research on hybrid pixel detectors, novel ASIC and sensor designs are developed and innovative interconnection technologies are explored. Both small and large collection electrode monolithic CMOS sensors are studied for the CLIC tracker. The HV-CMOS test chip ATLASpox_Simple has a timing resolution of 6.8 ns and a hit detection efficiency of $> 99.5\%$ which fulfil the CLIC tracker requirements. However, the spatial resolution of $11.3 \mu\text{m}$ is not compatible with the requirements. Therefore, a new test chip with modified pixel layout to improve the spatial resolution has been produced and is currently under investigation.

Test-beam results of the CLICTD HR-CMOS sensor have shown that a spatial resolution of $4.6 \mu\text{m}$, a timing resolution of 5.8 ns and full efficiency can be achieved, which meet the tracking detector requirements. Additionally, the estimated power consumption does not exceed the limit set for the CLIC tracker. The performance of CLICTD for inclined particle tracks is under investigation.

Acknowledgments

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