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Baby MIND Readout Electronics Architecture for Accelerator Neutrino Particle Physics Detectors Employing Silicon Photomultipliers

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The Baby MIND neutrino particle detector was installed at J-PARC in Tokai Japan in February 2018 and commissioned with first neutrino beam a few weeks later. It is instrumented with 3,996 Hamamatsu MPPCs type S12571-025C. A full readout electronics chain was developed to extract energy deposition and timing information of tracks left by charged particles from neutrino interactions in the Baby MIND and surrounding structures. Data from particle beam tests at CERN and commissioning at J-PARC are presented, to illustrate how the electronics readout architecture fulfills the physics requirements. A brief description of the adoption of this architecture for planned 60,000 MPPCs of a new 3D fine grained scintillator detector for operation at J-PARC from 2021 is given.

KEYWORDS: Neutrino oscillation, silicon photomultiplier, MPPC, readout electronics

1. Introduction

The Baby MIND detector was designed as a downstream muon spectrometer for the WAGASCI experiment E69, to study neutrino-nucleus interaction cross-sections [1]. These studies contribute to improvements in systematic errors for neutrino oscillation analyses at the T2K experiment in Japan. T2K measures the CP violation phase in the neutrino sector.

Given rapid progress in the development of silicon photomultipliers (SiPMs) and vast improvements in manufacturing techniques, our approach was to select a commercially available photosensor and focus on the development of customised readout electronics [2].

The detector consists of 18 plastic scintillator modules instrumented with 3,996 Hamamatsu Multi-Pixel Photon Counters (MPPCs). It is optimised for momentum reconstruction

and charge identification of muons between 0.3 and 1 GeV/c, enabled by a 70-tonne novel magnet system [3]. Baby MIND was assembled and tested on a charged particle beam line at CERN-PS in Geneva in 2017. It was installed at J-PARC and commissioned with T2K beam from February to May 2018. This paper discusses the electronics readout scheme, its architecture, main functional features, hardware and associated software.

2. Photosensor connectivity

Scintillating plastic bars are used (2880 mm horizontal bars and 1950 mm vertical bars), doped with 1.5% paraterphenyl (PTP) and 0.01% POPOP. A wavelength shifting (WLS) fiber type Kuraray Y11 fitted to the plastic transmits light from the hit position to the bar end [4]. MPPC type S12571-025C was chosen to match fiber diameter and transmission wavelength, each $1.0 \times 1.0\,\mathrm{mm}^2$, with 1,600 cells, $25\,\mu$m cell size, 5.15×10^5 gain, 100 kHz dark noise rate at 0.5 p.e. and 10% crosstalk probability. They are fixed to the edges of scintillator modules, sending signals down 5.5 m of co-axial cables to the electronics located in 8 minicrates on top of the detector, for ease of accessibility.

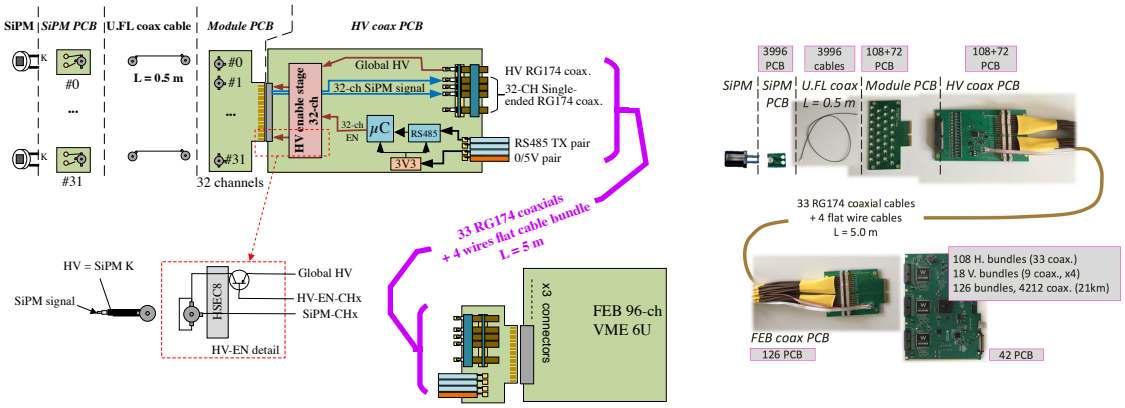

Fig. 1. Connection scheme from SiPM to readout electronics and sketch of main components.

The 32-channel cable bundles are shown in Fig. 1. Because the malfunction of one channel could affect all other channels (one MPPC connected with wrong polarity could destroy the CITIROC input stages), one high voltage (HV) line (per 32 ch) is drawn separately on the 5 m bundle (RG174 coax) from the Front End Board (FEB). The HV is applied to each channel at the MPPC-end of the cable bundle via an individual microcontroller ON/OFF enabling stage, and transmitted via a 0.5 m micro-coaxial cable through its shielded copper braid to the MPPC cathode. These cables are relatively short because their own signal integrity cannot be assured (copper braid is connected to HV rather than ground), however they, along with the MPPCs, are enclosed in a light-tight aluminium casing that is connected to ground. The 5 m coax cable copper braid is connected to ground for noise immunity of the MPPC signal carried in the inner conductor wire. An amplifier on the FEB side rather than the MPPC side ensures a current-mode signal transmission, with good noise immunity (preferable to a single-ended voltage mode signal transmission with amplification close to the MPPC).

The 3996 MPPCs have an average operating voltage (V_{op}) of 67.5 V, with a range of 67.1 V to 68.5 V. Each FEB provides a common high voltage of 69.7 V applied to all cathodes. Each MPPC V_{op} is adjustable independently from 69.7 V down to 65.2 V with the CITIROC embedded 8-bit 4.5 V DACs connected to the anode. Homogeneity of V_{op} for the 32 MPPCs connected to a given CITIROC was ensured by sorting MPPCs in batches of 32 with a V_{op} within $\pm$100 mV of the batch average. An optional external HV connector is also available.

3. Readout architecture

The Baby MIND electronics readout scheme includes several boards, Fig. 2. At the heart of the system is the FEB developed by UniGe, Fig. 3. Daisy chaining and synchronisation functions are carried out by two ancillary boards, the Backplane and the Master Clock Board (MCB), developed by UniGe and INRNE. The FEB architecture is based on 3 CITIROC chips that can each read signals from 32 MPPCs, one 8-channel ADC for the digitisation of the CITIROC analogue low gain (LG) and high gain (HG) outputs, one FPGA Altera Aria V to control and manage the timing and data flow from the CITIROCs and the ADC, some high speed transceivers for the FEB chain and MCB connectivity through the backplane, and a USB3 microcontroller for transmission of data to a data acquisition (DAQ) system.

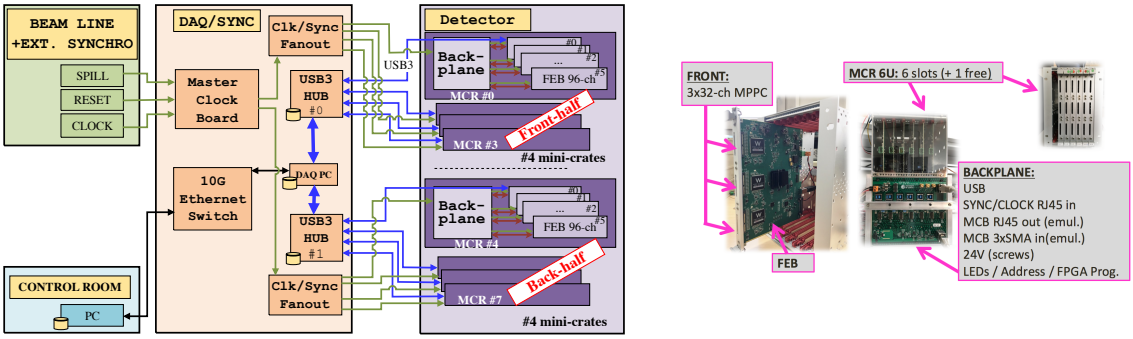

Fig. 2. Baby MIND readout electronics architecture (left), and hardware (right).

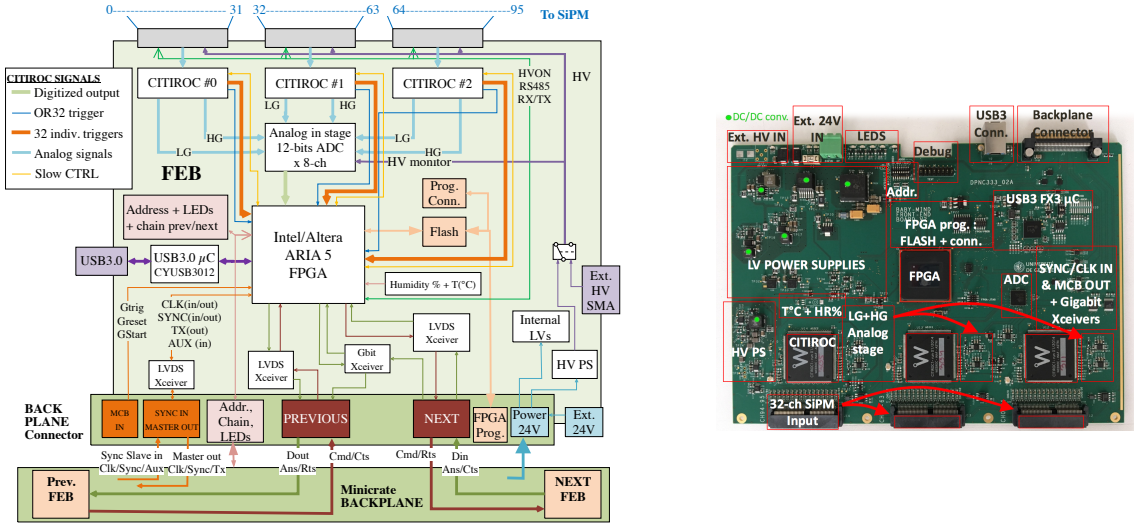

Fig. 3. Baby MIND Front End Board (FEB) bloc diagram with minicrate (MCR) backplane connectivity for multi-board daisy-chaining and illustrated photo of the FEBv2.

4. Deadtime-free signal sampling

The T2K beam spill is composed of 8 bunches of roughly 80 ns each in width separated by 580 ns. A spill duration is therefore $\sim 5\,\mu$s, repeated every 2.48 s, see Fig. 4. One obvious requirement for the electronics is to be capable of recording all neutrino-related events within a T2K spill. Given the low event rate, the probability that the same channel records multiple

neutrino-related hits within the same spill is $\ll 0.1\%$. Stronger requirements come from the necessity to discriminate real hits from MPPC dark counts, and from the need to operate with cosmic rays and at the CERN-PS beamline facility (∼400 ms spill length).

CITIROC is inherently a self-triggering device, for a detailed description of its features see [5]. Only one hit per channel can be recorded from each of the two analogue signal paths (HG & LG) during a pre-defined window in time for analogue data acquisition, T_{HOLD}, always sampled at the peak of the slow shaper output regardless of the hit time. The recorded hit for a given channel is then the hit with the highest amplitude, see Fig. 4. For T2K operation we choose $T_{HOLD} = 10\,\mu$s, at the end of which, the signals are multiplexed on the CITIROC and pushed out towards an external ADC.

The multiplexing and digitisation phases following the CITIROC analogue signal paths introduce a $9.12\,\mu$s deadtime. This deadtime combined with the hit multiplicity limitation leads to a maximum of 1 hit per channel per roughly $T_{HOLD} + 9.12\,\mu$s. To overcome this limit, we register the signal amplitude by sampling both the rising and falling edges of the fast shaper output (CITIROC trigger outputs, one per channel) with the FPGA at 400 MHz. This sampling is continuous and deadtime-free. The rising edge provides the event time stamp. The time difference between the two sampled edges (Time-over-Threshold or ToT) is proportional to signal amplitude. It is a reliable estimate provided calibration against the analogue stages is carried out for hits that have both ToT and HG/LG data. Fig. 5 shows HG vs ToT from the CERN beam tests, along with a pulse height distribution and a hit map for the detector obtained with 3 GeV muons. The hit time for the digitised analogue HG and LG hit amplitudes is defined by assigning the hit time stamp from the highest recorded ToT. The fast shaper has a peaking time of 15 ns, which effectively sets the minimum time interval for resolution of two independent consecutive hits on the same channel.

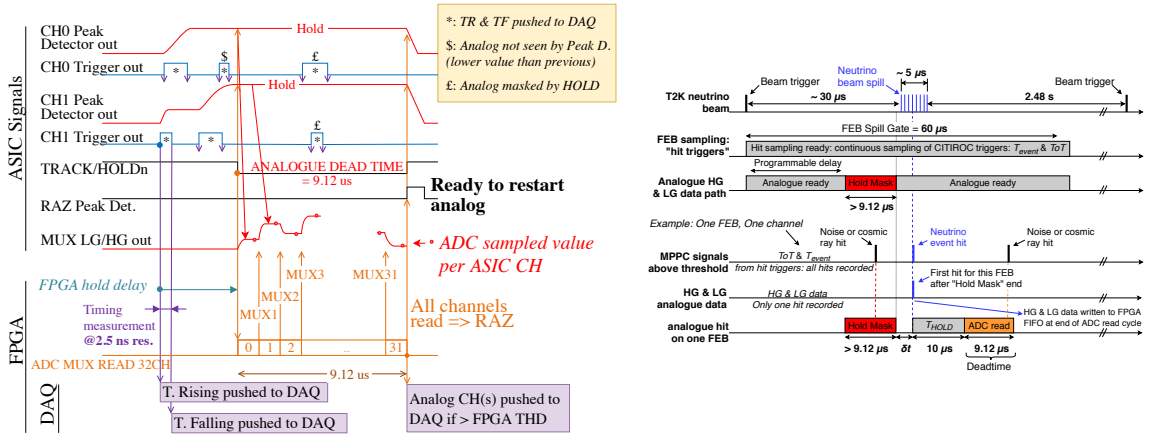

Fig. 4. Illustration of FPGA sampling of CITIROC individual trigger outputs (left), and analogue signal peak detector output processing. Hit recording with respect to beam occurence (right).

The full acquisition window width is set to $60\,\mu$s per T2K spill, during which the analogue output stage readout sequence can undergo more than one cycle (T_{HOLD} + deadtime).

Vertical and horizontal bars light yields were measured with this electronics during CERN beam tests (and separately with waveform digitizer-based electronics in brackets [6]) to be 15(19) p.e./MIP and 25(32.5) p.e./MIP. A gain of 40 ADC/p.e. during commissioning meant a useable dynamic range > 2 MIPs, on the HG analogue output stage. Time resolution is limited by plastic scintillator and wavelength shifting fiber properties, and was measured to be 0.95 ns with different electronics sampling at 5 GHz [7]. The 400 MHz FEB sampling with a time resolution of $2.5\ \text{ns}/\sqrt{12}$ is therefore well matched to these scintillator bars.

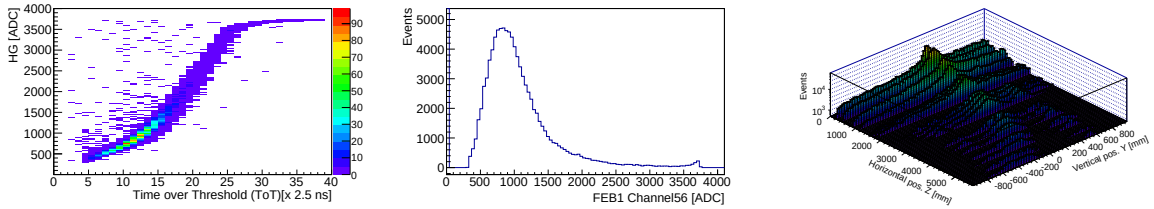

Fig. 5. Data from the CITIROC HG analogue output (left) plotted against ToT from the trigger path for one channel exposed to a 2 GeV muon beam at CERN-PS. Pulse height distribution (middle) for the same channel. Hits (right) from the 18 scintillator modules for 3 GeV muons at CERN, shown as a 2D histogram along the YZ projection, the horizontal Z positions are along the muon beam axis.

5. Synchronisation

A relativistic muon will cross the whole detector from front to back in 13.6 ns given the 4.084 m detector length. Determining the directionality of a crossing track requires a FEB time resolution at the ns level, provided by the 400 MHz FPGA sampling, and by trace length equalization for all 96 channels on all PCBs and cables along the full signal path from MPPC to CITIROC input at the sub-100 ps level, with the added requirement of good synchronisation of all FEBs in the system. Central to FEB synchronisation is the Global Trigger (GTRIG) signal which is a local reference clock issuing a time stamp every 10 μs (100 kHz). The GTRIG input can be selected from either:

- An external GTRIG signal decoded from the SYNC signal sent by the MCB.
- An internal generator with a programmable period (e.g. standalone mode).

The synchronisation subsystem is the MCB which produces a common detector clock (CLK) and combines user signals (reset, start readout), synchronization signals (GTRIG, Frame Synchronisation for inter boards communication) and input signals from the accelerator beam line including a spill number and a pre-beam trigger (spill gate) issued 30 μs before the beam, into a single digital synchronisation signal (SYNC).

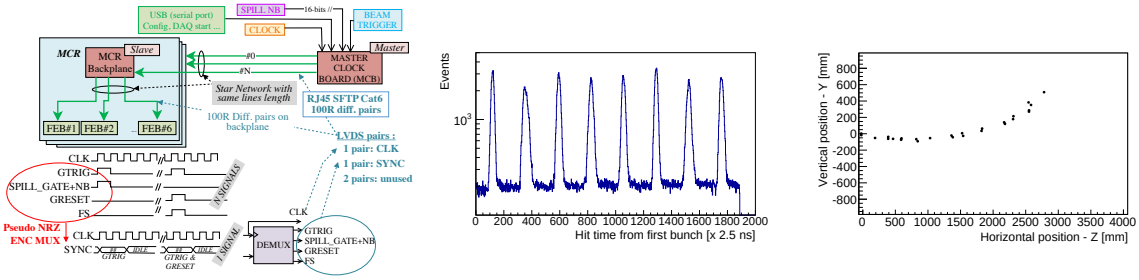

Fig. 6. Synchronisation scheme (left) with 1 MCB propagating signals over 2 of 4-pairs RJ45 LVDS to 8 MCRs each having a backplane sending signals to all MCR FEBs (1 to 6 star fanout network). Recorded hits (middle) from a commissioning run showing the T2K bunch structure. Muon track (right) from an anti-neutrino interaction upstream of Baby MIND.

The spill gate can be used to stop data flow when the window is closed to avoid pushing data without events. It could also be used to switch to another acquisition mode (e.g. calibration). The spill number is 16-bits encoded serially from a parallel 16-bit input from the beam line synchronously with the PRE-BEAM trigger. Finally the MCB can eventually be synchronised to an external experiment clock running at 100 MHz, Fig. 6. Both SYNC and CLK signals are transmitted from MCB via 2 pairs of a RJ45 cable and distributed locally to the FEBs within one minicrate via the backplane. A fanout board can also be inserted

in order to drive multiple minicrates. The internal 400 MHz clock on each FEB is synchronised to the common detector clock (CLK). Tests show the FEB-to-FEB CLK (SYNC) delay difference to be 50 ps (70 ps) [8].

A 'Hold mask' scheme ensures the HG/LG read cycles of all CITIROCs on all FEBs start concurrently, by disabling analogue data sampling for a period at least as long as the full ADC read cycle, Fig. 4. At the end of the Hold mask, all FEBs are ready for a new analogue read cycle, and operate in self-triggering mode thereafter. The 8-bunch structure of the neutrino beam is clearly resolved by the readout system, Fig. 6 (right).

6. USB3 Data and Slow Control Flow

Readout is asynchronous and based on a 'data push' mode. Two data transfer mechanisms operate for the DAQ Data flow:

- FEB-to-DAQ PC transfer via USB3.0 at 3.2 Gbit/s max, but often limited to the DAQ hard disk capability ($\sim$ 2 Gbit/s on BabyMind).
- FEB-to-FEB transfer via MCR backplane. Max. 1 Gbit/s.

Several readout modes are possible. The standalone mode allocates the full USB bandwidth to the USB-connected FEB. For a chain of minicrate FEBs (6 FEBs maximum per backplane), the Time-division Multiplexing (TDM) mode is used whereby every FEB automatically sends its data through the backplane to the first FEB of the chain which is connected to USB. The USB bandwidth is shared by six FEBs and every FEB in the chain communicates on a dedicated time slot synchronized by the MCB Frame Synchronisation (FS) signal operating at 10 kHz.

The DAQ protocol is based on a modulo 32-bit words due to the USB microcontroller 32-bit interface connected to the FPGA. Every 32-bit word is built with the 4 MSB bits reserved for the word ID which defines the content for the remaining 28 LSB bits.

The CITIROC and FPGA slow control configuration is implemented entirely via the same USB link used for data transfer, DAQ and slow control using different USB endpoints i.e. USB logical links. For the FEB chain, 1 Mbit/s dedicated RX/TX NRZ LVDS lines following a RS-485 protocol are used on the backplane. Each board is accessed by the protocol through its single board ID built with the MCR address (3 MSB bits) and the FEB slot (3 LSB bits).

Raw binary data transfer rates average 500 MB per day of running at T2K for the full Baby MIND detector (all 8 MCRs).

7. Firmware and platform-independent readout software

The Baby Mind firmware and software uses the UniGe library to operate, see Fig. 7. The DAQ environment consists of the BabyMind application VHDL firmware in FPGA, the Unige VHDL firmware communication library in FPGA, the USB3 Cypress FX3 microcontroller, the UniGe FX3 firmware, the Windows/Linux cypress USB driver for FX3, the UniGe Windows/Linux C# library in the host PC and the BabyMind application C# software in the host PC.

The USB3.0 link is transparent from both sides, providing 1 bi-directional Slow control channel (1 IN and 1 OUT USB Endpoint) and 1 fast FPGA-to-PC readout channel (1 IN USB Endpoint). The BabyMind .NET application was developed on Windows 7. Once compiled it can also be operated on Linux (tested on CentOS 7).

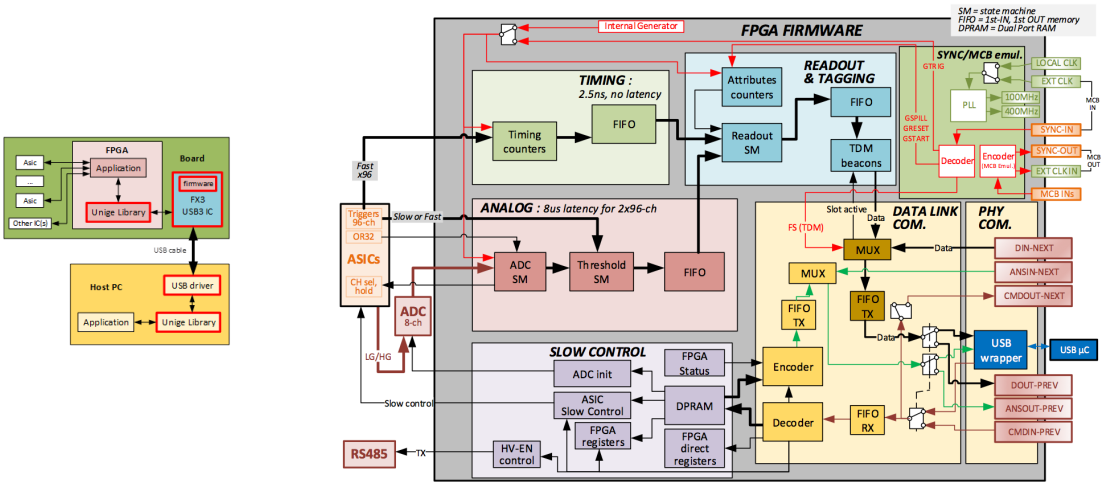

Fig. 7. Baby MIND software implementation and FEBv2 FPGA firmware architecture.

8. Summary and Outlook

A complete electronics readout front end has been developed for the Baby MIND detector instrumented with silicon photomultipliers. Its development benefited from extensive testing at beamlines at CERN-PS in 2016 and 2017. The detector was commissioned at J-PARC in 2018 with T2K beam and is due to operate for first physics runs in 2019.

The main features of this modular, versatile system such as deadtime free signal sampling and asynchronous USB3 readout can be applied to a broad range of applications. A readout scheme based on the Baby MIND architecture has recently been adopted for the SuperFGD, a new 3D fine grained scintillator detector with 60,000 MPPCs type S13360-025 planned for operation in 2021 by the T2K ND280 near detector upgrade project [9].

9. Acknowledgements

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