PROCEEDINGS OF SCIENCE

Commissioning High-speed Readout for the LHCb VELO Upgrade

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The new Vertex Locator for LHCb, comprising a new pixel detector and readout electronics, will be installed in 2020 for data-taking in Run 3 at the LHC. The electronics centres around the "VeloPix" ASIC at the front-end operating in a triggerless readout at 40 MHz. Custom serialisers send zero-suppressed data from the VeloPix at a line rate of 5.13 Gb/s. System tests of the complete electronic and optical chain, along with early results from high-speed link tests at CERN are presented.

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1. Introduction

This paper describes the high-speed electronics of the LHCb Vertex Locator (VELO)[1][2] currently being constructed and commissioned for operation for LHC Run 3 in 2021. The VELO is a silicon hybrid pixel detector operating in vacuum and very close to the LHC beams (5.1 mm), and therefore must cope with a very high radiation environment[1]. Furthermore, LHCb will have no hardware trigger, and so the ASICs must readout every bunch crossing at the full machine rate. A new front-end ASIC, VeloPix [3], was designed to meet these requirements. The VeloPix and its supporting readout electronics will be described. Some of the challenges to commission the full VELO high-speed readout system, and the solutions developed are presented.

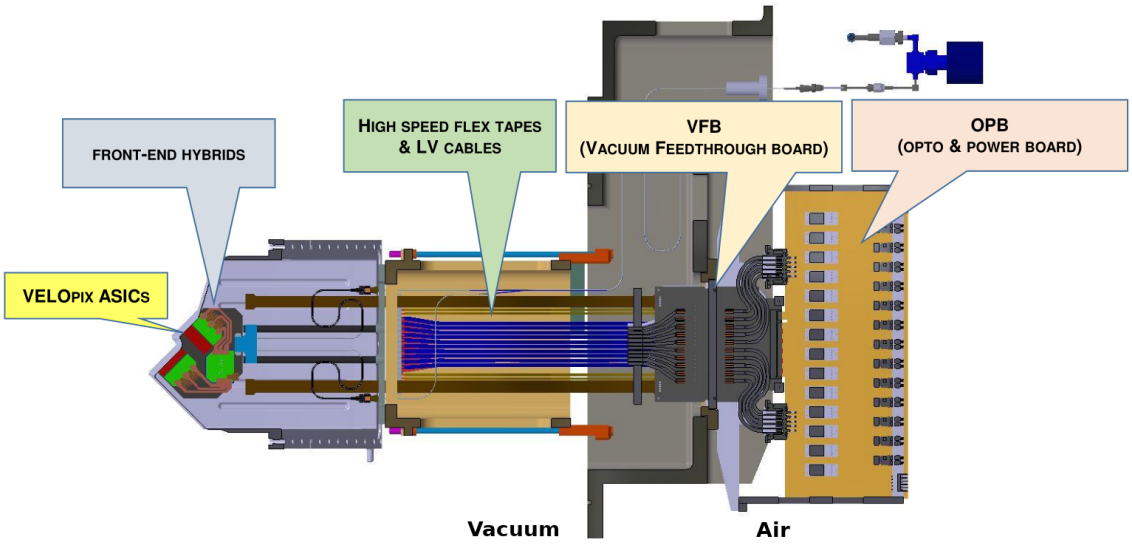
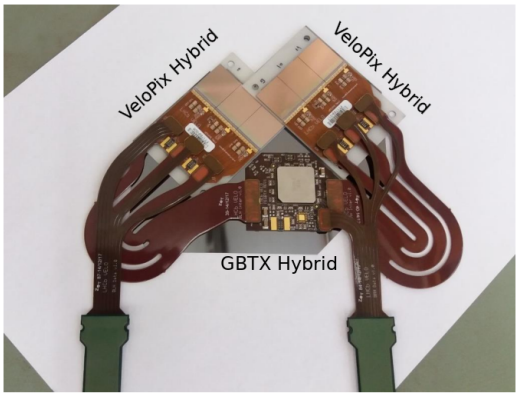


Figure 1: CAD drawing of a VELO module, with leftmost showing the VeloPix ASICs wire-bonded to the front-end hybrids. High-speed flex tapes connect the hybrids to the vacuum feedthrough board, bridging the vacuum-air boundary of the VELO vacuum tank. Opto-Power Boards sitting on the exterior of the tank route data to Versatile Links for conversion to optical transport.

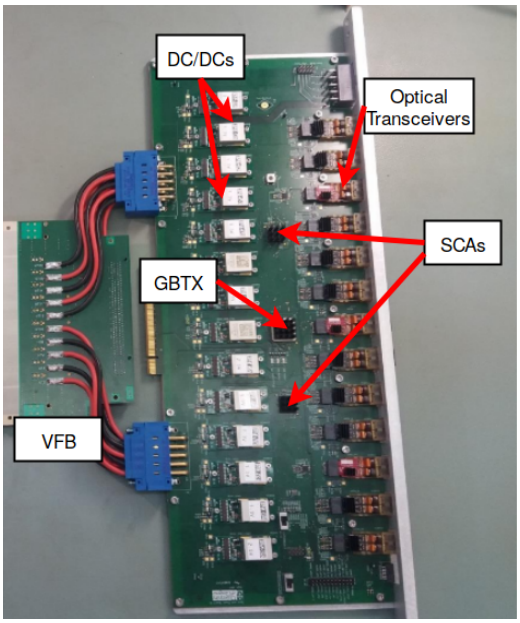
2. VELO Electronics

A slice of the VELO detector is shown in figure 1. The modules consist of four silicon sensor tiles (2 per module side). Each sensor is bump-bonded to three VeloPix ASICs. These VeloPix "triplets" are wire-bonded to hybrid circuitry which routes the I/O to and from the chips (see figure 2a). The GBTX chip [4] is used as the control/timing/monitoring interface for the VeloPix chips, and this has its own hybrid. The hybrids are mounted onto a silicon microchannel cooling substrate and communication between hybrids is facilitated via interconnect cables. The VELO is a moveable detector, with each VELO half retracting during LHC beam injection. Flexible data tapes between the base of the VELO hybrid and the vacuum feedthrough board are used to meet the motion requirement. The VELO electronics make extensive use of components from the CERN GBT and Versatile Link Projects [4, 5, 6].

[1] maximum fluence is expected to be $8 \times 10^{15} \cdot 1\text{MeV} \cdot \text{n}_{\text{eq}}/\text{cm}^2$



(a) VELO hybrid assembly



(b) Opto-Power Board

Figure 2: (a) Hybrid assembly of one side of a VELO module. Two VeloPix hybrids are shown with interconnect cables to the GBTX hybrid in the centre. Data/Control flex tapes are shown (in green) at the bottom of the figure. Sensors have not been bonded in this example and the bare VeloPix ASICs can be seen. (b) Opto-Power Board showing its connections to the VFB, DCDCs for powering, GBTX and SCA chip, and the Versatile Link Optical modules for data transmission and timing and control signalling.

2.1 VeloPix ASIC

The VeloPix front-end ASIC driving the design of the VELO control and data acquisition is part of the Medipix/Timepix family. It employs 130 nm CMOS technology and each chip has a 256×256 pixel matrix, each $55 \times 55 \mu m^2$ in size. VeloPix is designed for data-driven readout, with binary precision, meaning a "hit" is registered when a signal above a tunable threshold is detected. It is optimised for high speed readout at 40 MHz with a peak hit rate of 900 Mhits/s, corresponding to a maximum data rate of 19.2 Gb/s per ASIC. The chips are radiation hard to 400 MRad and SEU tolerant.

2.2 Front-end to Back-end electronics

A Vacuum Feedthrough Board (VFB) is installed in the VELO vacuum tank to provide signalling to the flex-tapes in the vacuum and the Opto-Power Board (OPB) connected on the outside of the tank. The OPB (shown in figure 2b) consists of a GBTX and two GBT-SCA chips [6]. GBLDs are also employed to drive the timing and control signals to and from the GBTX hybrids.

The back-end is provided by a common readout board for LHCb - the PCIe40 [7] card. As the name suggests, it is a PCIe (Gen-3 $\times 16$) card. Core to its design is the Intel *Arria10* FPGA (10AX115S4F45E3SG). It supports up to 48 duplex links at ~ 5 Gb/s each. The measured output

bandwidth is ~ 100 Gb/s over the PCIe bus. The function of the PCIe40 can be determined by its firmware - it can be used for timing, control, or data acquisition (or all three at once).

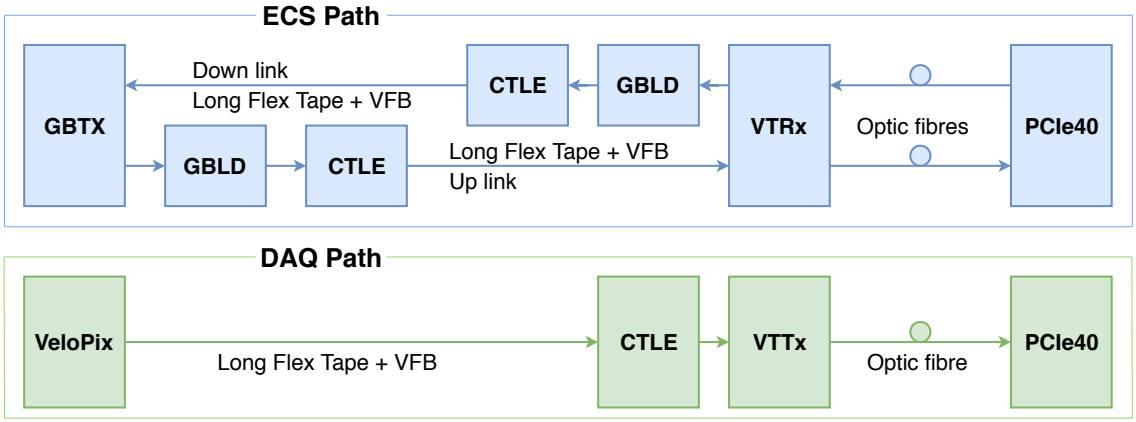


Figure 3: ECS and DAQ paths from front-end to back-end. The extra components on the duplex ECS path compared to the DAQ path are described in the text.

The complete set of signalling pathways can be encapsulated into two distinct groups of links[2] - ECS (Experiment Control System) and DAQ. The two paths have similar physical properties, but differ in terms of line-rate (4.8 Gb/s for ECS, 5.12 Gb/s for DAQ) and protocol. GBT is used for ECS, and GWT (a custom VeloPix protocol and associated serialiser) are used for DAQ. They share similar electrical transmission lines and therefore, similar performance is expected.

For the ECS links, a GBLD on the OPB is used to amplify and set some pre-emphasis to boost the signal quality. A passive Continuous Time Linear Equaliser (CTLE) circuit is added to attenuate low-frequency noise from the transmission lines, and subsequently reduce the overall jitter at the receiver. The VeloPix has some internal emphasis and a large signal amplitude (1V p-p), obviating the need for an extra GBLD.

3. Results

Here are described some of the more interesting findings from high-speed commissioning tests of a complete VELO slice.

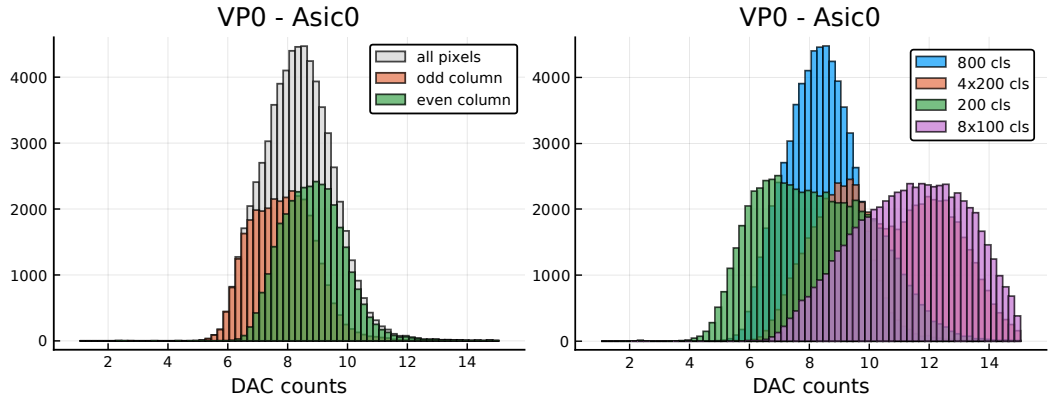
3.1 GBTX Testing in the cold

A problem with GBTX communication was discovered during the first cooling tests of completed VELO prototype modules. Despite performing without issue at ambient room temperatures, communication from the PCIe40 to the GBTX on the module was lost whilst cooling the module to its operational temperature of 30°C. A GBTX I^2C programming cable was used to monitor the internal state of the GBTX. At temperatures below -10°C, the GBTX was stuck in a "WaitDESLock" state, meaning that the clock and data recovery (CDR) circuit was having trouble recovering the incoming clock. To correctly receive the GBT serial data stream, both the frequency and phase of

[2]The term "link" is used to denote a single electrical and optical pathway.

the CDR clock much precisely match those of the incoming data. The CDR circuit performs frequency locking and phase alignment in separate steps to complete its locking sequence. The CDR PLL which performs the phase alignment was found to have more noise at lower temperatures. Increasing the CDR phase detection charge pump current from 1.5μA to 5.6μA compensated for the additional noise, restored the locking sequence so that the GBTX could complete initialisation, thus restoring its functionality. This solution was offered by the GBTX team at CERN, and approved for GBTX cold operation.

3.2 VeloPix Shutter Noise



(a) Noise Odd-Even

(b) Noise v. shutter lengths

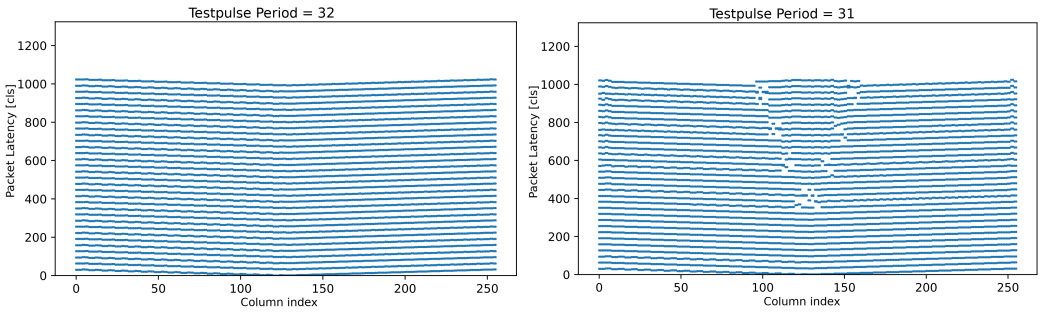
Figure 4: Measured noise in an example VeloPix. (a) A difference between the noise on odd (orange) and even (green) columns can be seen. (b) Varying the length of time the shutter is open and closed affects the noise. The four different patterns are described in the text.

Noise on the VELO pixels is measured by counting the number of hits over threshold in a given time window. This time window is controlled by opening a shutter inside the VeloPix. The shutter open time is adjustable. This data is acquired over the ECS path of the VeloPix. The noise shown in figure 4 is measured in DAC counts (15.4 e^-/DAC), with noise hits counted as a function of DAC value. A per-pixel fit of DAC counts is used to create the histograms.Examining the noise revealed a double peak structure rather than the typical Gaussian shape. This was determined to be a function of the column number of the VeloPix matrix. Even columns produced more noise than the odd columns, as can be seen in figure 4a. Further investigation revealed that the noise was strongly influenced by shutter time window. Figure 4b shows four distinct shutter patterns. The blue is 800 clock cycles (cls) long, orange is four sequential shutter open-close operations of 200 cls, green is 200 cls, and purple is eight sequences of 100 cls. From this, one can conclude that the act of opening the shutter introduces extra noise in the chip. A proposed solution is to take noise over the DAQ path, where the shutter is always open. This method will be used for threshold equalisation of the chip and should more accurately reflect noise during the VeloPix standard data taking configuration, where the shutter is always open.

3.3 Bandwidth saturation tests

Test-pulses (injected signals) were used to test the bandwidth of VeloPix, and the full link

chain. Data were received from the PCIe40 and reconstructed. Test-pulses were injected in the top row of the VeloPix matrix. These must traverse the full column to the end-of-column readout logic. By injecting test-pulses at the appropriate frequency, one can ensure the readout queue is always full and bandwidth is fully utilised. Using the top row puts the chip into its maximal power consumption state as both pixel and routing logic are active. Figure 5 shows we can fully saturate a VeloPix link without loss of packets. Loss occurs, as expected, above the bandwidth limit.



(a) At bandwidth capacity

(b) Above bandwidth capacity

Figure 5: Latency of packet arrival from VeloPix. Data arrival is regular at 100% bandwidth saturation and becomes irregular when bandwidth is oversaturated, indicating packet loss. The "V" shape is due to hits at the column edges taking longer to reach the output logic at the centre.

4. Summary

The Vertex Locator for LHCb is being extensively tested as it nears its commissioning phase. Following successful performance in beam tests at CERN SPS facility, a campaign was launched to test the high-speed DAQ and control chain to its limits. Some issues have been found and overcome in this process. The overall signal quality has been tested on several production level prototype modules and met the data taking requirements.

References

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[3] T. Poikela, et al. *VeloPix: the pixel ASIC for the LHCb upgrade*, JINST **10** (2015), no. 01, C01057

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