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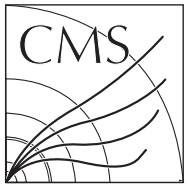

The Compact Muon Solenoid Experiment

Conference Report

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Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade

N. Rasevic, G. Blanchot, S. Baron, M. Kovacs, S. Kulis, D. Porret, A. Zografos

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PROCEEDINGS OF SCIENCE

Development of an Optical Readout Hybrid for the CMS Outer Tracker Upgrade

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Abstract

The pixel-strip modules for the CMS Tracker Phase-2 Upgrade for the HL-LHC integrate a readout hybrid (PS-ROH) for the control and data acquisition link. This hybrid is based on the new, low power and compact gigabit transceiver (LpGBT) and the versatile transceiver VTRx+ specifically designed for the upgrade. A characterization board was first designed to qualify the design rules and the achievable timing performance of the gigabit block. This design enabled the development of the PS-ROH for the CMS Tracker PS modules. A testing setup was also developed to verify the PS-ROH performance before its integration into the PS modules.

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1. Introduction

Two new front-end module types (2S and PS) are currently under development for the Compact Muon Solenoid (CMS) Tracker Phase-2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) [1]. The 2S modules are based on a double strip-strip (2S) sensor configuration. The PS modules (Fig. 1) contain a strip sensor and a macro-pixel sensor and two front-end hybrids interconnected with a power hybrid and with a PS readout hybrid (PS-ROH). The readout hybrid enables the optical transmission of data, clock and control signals at transmission speeds up to 10.24 Gbps in the cold and radiation environment of the tracker.

The optical readout hybrid interfaces two PS front-end hybrids with the new Low Power Gigabit Transceiver (LpGBT) [2]. This new ball grid array chip provides different transmission modes, high-speed differential ports (e-links), digital input and output control ports and eight analog to digital converter (ADC) inputs. It provides an enhanced clock distribution and phase alignment features, comparing with the GBTX chip.

A characterization board enabling all possible configurations was designed in a first step on a six layer rigid printed circuit board. It provides 100 Ω matched impedance tracks with test connectors for the LpGBT phase-shifted clocks, some of the e-links and with high data rate SMA connectors to interface with an external optical driver (VTRx+). The differential pair topologies were verified with signal integrity simulations. Two decoupling scheme configurations on the top and on the bottom layer were proposed and characterized by power integrity simulations.

The LpGBT was later on integrated into the PS-ROH, on a four layer flexible circuit. Suitable differential topologies were defined for an achievable impedance of 90 Ω for the e-links. A specific differential pair topology for the gigabit lines connecting to the VTRx+ was also defined. Here, the decoupling scheme is only possible on the top layer, and power integrity simulations allowed comparing the expected performance with respect to the characterization board implementation.

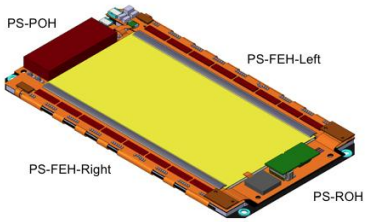

***Figure 1**: PS Module.*

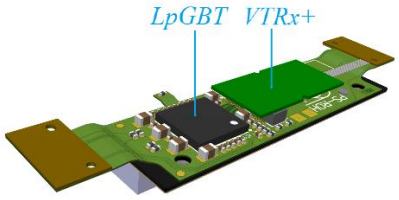

***Figure 2:** PS Read Out Hybrid.*

2. PS Readout Hybrid

The PS-ROH is interconnected with two front-end hybrids (FEH), using fine pitch Panasonic connectors. The readout hybrid (shown in Fig. 2) hosts an LpGBT and VTRx+ laser driver transceiver. This hybrid provides distribution of data and clocks to the FEHs and data from FEHs to the back-end FPGAs. Figure 3 shows the block diagram of the PS readout hybrid. The main component on the PS-ROH is the LpGBT, whose role is to accept high speed data from the VTRx+ module, to decode it and to send specific commands to the FEH ASICs. It also distributes clocks, serializes the data arriving from the FEHs and sending them back to the FPGA over the optical

link. The LpGBT ADC module and the GPIO ports allow monitoring the working parameters for an entire module, for example: supply voltages, power good lines, or sensor temperature.

The PS readout hybrid is built on a four layer flexible board, with a total thickness of maximum 200 µm. The copper thickness is 12 µm. For layer interconnection blind and buried microvias are used. Figure 4 shows the detailed stack-up structure of the PS-ROH.

The LpGBT input and output ports are designed as LVDS lines tuned for a terminated differential impedance of 100 Ω. Because of technology and design constraints which are used for fabrication of the PS-ROH board and all the front-end hybrids, that requirement is not achievable. The highest achievable differential impedance is 90 Ω [4]. The differential pair geometry used in this design is based on 50 µm wide traces and a 60 µm gap between the traces, with 25 µm spacing between the layers. The high speed VTRx+ lines, which are very short, are defined without ground plane on the first layer below the differential lines: this doubles the spacing between the differential pairs and the reference plane layer, enabling to achieve a 100 Ω differential impedance.

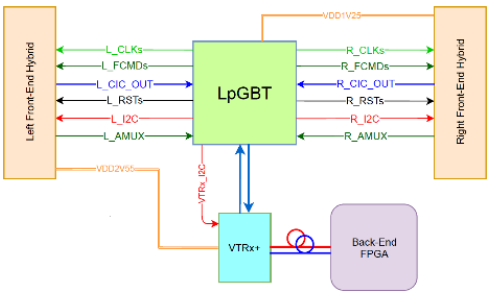

***Figure 3**: PS-ROH block diagram.*

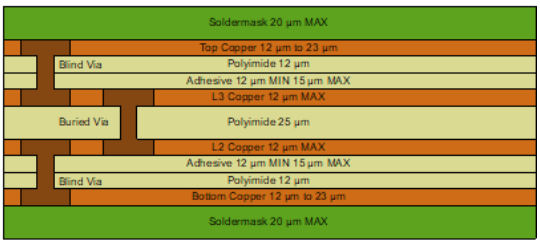

***Figure 4**: PS-ROH stack-up specifications.*

3. VL+ Characterization Board

This board is designed to characterize the LpGBT chip, to allow the testing of basic features and the chip functionality in a high radiation environment and to define a reference design for all the LpGBT based boards.

The characterization board shown in Fig. 5, is a six layer rigid board (Fig. 6), with dimensions of 170 mm x 160 mm. It hosts the LpGBT, which is the only active component on the board, and several connectors and switches.

The characterization board allows access to seven e-link data inputs, four e-link data outputs, four e-link clocks, four phase-shifting clocks, 40 MHz reference clock input, high-speed data transceiver, two master I2C lines and one slave I2C line. On-board DIP switches enable setting the chip address, the chip mode of operation, lockmode, I2C slow-control pin and optional I2C pull-ups. The mode configuration is also available through the I2C ten-pin header connector.

The power supply is provided from outside through two-pin power connectors, which enables complete independence from on-board power regulators and sources.

Most hybrids are designed to host components on just one side, which is also the case with the PS-ROH, which could be a potential problem in terms of chip power decoupling, because the LpGBT chip is designed with the requirement to have the decoupling below the chip (on the opposite side of the board). That is the reason why we designed the characterization board with two optional decoupling positions.

The differential pair geometry is calculated using an Altium Designer tool, obtaining a track width of 100 µm, a gap between the tracks of 100 µm and spacing between the differential pair and reference plane of 100 µm. The Rogers RO-4450F prepreg dielectric material is used, on a copper thickness of 35 µm in the middle layers and 50 µm on the outer layers. Differential lines are routed just on the top and bottom layers.

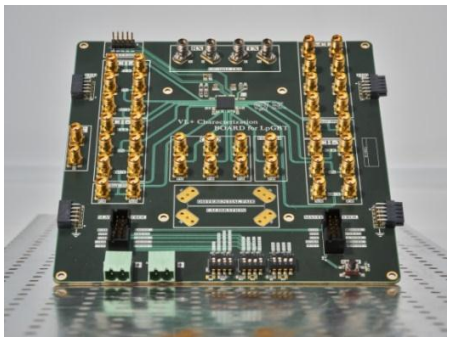

***Figure 5**: VL+ characterization board.*

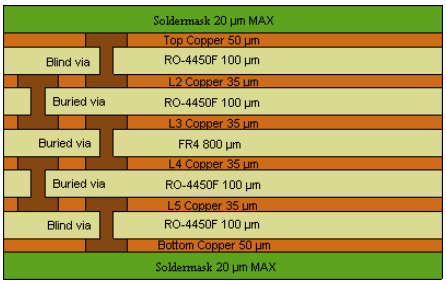

***Figure 6**: Characterization board stack-up.*

4. Simulations and Measurements

The PS readout hybrid flexible board is under fabrication at the moment of writing this publication, therefore our measurements are based mostly on the characterization board.

4.1 Power Integrity

The power integrity related characteristics were simulated with the HyperLynx tool from Mentor Graphics. The voltage drops and the frequency response of different decoupling schemes were characterized from 1 MHz to 150 MHz.

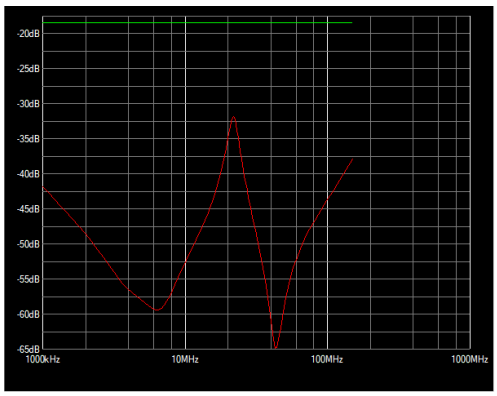

***Figure 7**: PS-ROH decoupling frequency response.*

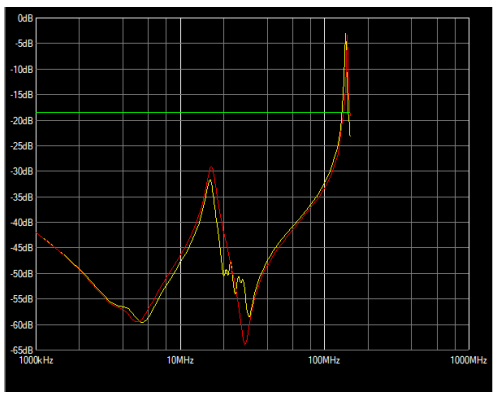

***Figure 8**: Characterization board decoupling frequency response.*

Figure 7 shows the frequency response for a decoupling capacitor scheme on the PS-ROH hybrid. Figure 8 shows the frequency response for two capacitive decoupling topologies on the characterization board, the red line representing the response for a decoupling on the top layer at the periphery of the LpGBT, and the yellow line representing the response for a decoupling topology on the bottom layer, under the LpGBT chip.

The results are acceptable, except for the frequency range between 15 MHz and 25 MHz. The increased impedance in this region is however not exceeding the target value of -18 dB (120 mΩ), which is calculated using the HyperLynx tool.

4.2 Signal Integrity

The differential impedance on the high-speed line of the characterization board is measured using a vector network analyzer, and the results are shown in Fig. 9. The impedance is near to 105 Ω in the section where the signal passes through the lines, with a rise of impedance to almost 120 Ω in the region where the signals enter the board and pass through the SMA connectors. In another section where the signals pass through the 4 levels of vias, the impedance falls to a value of around 60 Ω. These results are still satisfactory, because the impedance of 105 Ω is ±10 % of the nominal value, resulting from fabrication tolerance, and sections where greater impedance mismatch occurs are very short, and result from the usage of specific passive components. There is no change in impedance value related to different decoupling capacitor positions.

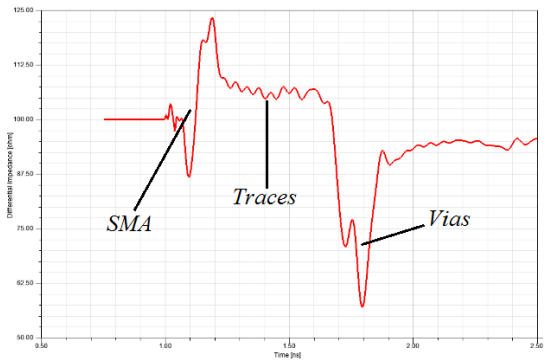

***Figure 9**: Characterization board high speed transmitter differential impedance.*

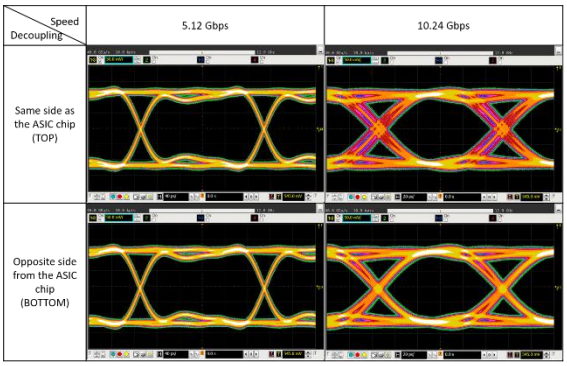

***Figure 10**: Characterization board eye diagrams by operating speeds and decoupling capacitor positions.*

The eye-diagram shows the characteristics of the real transmitted data. Figure 10 shows the eye-diagrams measured on the high speed transmission line of the characterization board. The eye-diagram characteristics, namely the eye opening and the rise and fall time, are as the chip designers predicted. Slight differences are observed for the higher transmission frequencies (10.24 Gbps), for the two different decoupling capacitor positions.

5. Conclusion

The computer simulation and measurement of S-parameters and eye-diagrams for different configurations on the characterization board suggest that the topology applied in the PS-ROH design will perform well. Testing of the features and characterization of the LpGBT is validated with the characterization board. The PS-ROH design rules were defined on the basis of the characterization board rules.

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