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Silicon Pixel Sensor R&D for the CLIC Tracking Detector

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Abstract

The physics aims at the proposed high-energy e^+e^- collider *CLIC* pose challenging demands on the performance of the detector system. Precise hit-time tagging, an excellent spatial resolutions, and a low mass are required for the vertex and tracking detectors. To meet these requirements, an all-silicon vertex and tracking detector system is foreseen, for which a broad R&D programme on a variety of novel silicon detector technologies is being pursued. For the ultra-low mass vertex detector, different hybrid technologies with innovative sensor concepts and interconnection techniques are explored. For the large-scale tracking detector, the focus of the R&D lies on monolithic HV-MAPS and HR-CMOS technologies. This contribution gives an overview of the ongoing activities with a focus on monolithic technologies for the CLIC tracking detector. Recent results from laboratory and test-beam measurement campaigns of the *ATLASpix_Simple* and the *CLICTD* sensor prototypes are presented.

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KEYWORDS: Solid state detectors, particle tracking detectors, electronic detector readout concepts (solid-state)

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1 Introduction

The *Compact Linear Collider* (CLIC) [1, 2] is a proposed high-energy electron-positron collider based at CERN in Geneva, Switzerland, for the era beyond the High-Luminosity Large Hadron Collider (HL-LHC) [3]. Its physics goals comprise top quark and Higgs boson measurements with unprecedented precision, as well as searches for Physics Beyond Standard Model (BSM). It is proposed to be constructed in three energy stages reaching a centre-of-mass energy of up to 3 TeV and a total length of 50 km at the final stage.

An innovative two-beam acceleration scheme is being developed for the CLIC accelerator [1]. A low-energy high-current drive beam transfers its energy to the main beam with high energy and low current in normal-conducting cavities, the so-called two-beam modules. This acceleration technique allows for gradients of more than 100 MV/m.

The proposed physics aims for CLIC [4] pose challenging demands on the performance of the detector system [5]. For pile-up rejection and to mitigate the impact of beam-induced background, a precise hit-time tagging with a resolution of ~ 5 ns is required for the vertex and tracking detectors. In addition, an ultra-low material budget of $\sim 0.2\%$ of a radiation length (X_0) per layer for the vertex detector and $\sim 1\%$ X_0 per layer for the tracking detector are required while achieving a single-plane spatial resolution of a few micrometers. The detector requirements are summarised in Table 1.

To meet the stringent detector requirements, an all-silicon vertex and tracking detector system is foreseen as the central part of the *CLIC detector model* (CLICdet) [6]. In order to identify suitable technologies, a broad R&D programme on a variety of novel silicon detector technologies is being pursued [5].

For the ultra-low mass vertex detector, different small pitch (25 μm) hybrid technologies with innovative sensor concepts are explored [7]. A dedicated readout chip called *CLICpix2* [8] has been developed in 65 nm CMOS technology and bump-bonded to thin planar active-edge sensors [9]. To overcome the challenges of the fine-pitch bump-bonding, alternative interconnection techniques

Table 1. Summary of the requirements for the CLIC vertex and tracking detectors [5].

	Vertex Detector	Tracking Detector
detector area	0.84 m ²	137 m ²
timing resolution	~5 ns	~5 ns
hit detection efficiency	99.7 – 99.9 %	99.7 – 99.9 %
maximum pixel size	(25 × 25) μm ²	30 – 50 μm × 1 – 10 mm
material budget per layer	~0.2 % X ₀	1 – 1.5 % X ₀
average power dissipation	<50 mW/cm ²	<150 mW/cm ²

such as capacitive coupling and anisotropic conductive films are explored [10]. In addition, Silicon-On-Insulator (SOI) test chips are also under investigation [11].

Monolithic CMOS technologies are promising for the large-area tracking detector due to their cost effectiveness and large-scale production capabilities. Different sensors with large and small collection electrodes are under investigation and recent results from the *ATLASpix_Simple* and the *CLICTD* test chips are presented in Section 2 of this paper.

In order to predict and further optimise the performance of the various prototype technologies, a fast and versatile simulation tool, *Allpix Squared* [12], has been developed. It allows for high statistics Geant4-based [13] Monte Carlo simulations, for which detailed electric field maps from TCAD finite-element simulations can be imported for a highly accurate description of the sensor properties.

To allow fast prototyping cycles, a versatile data acquisition system called *Caribou* [14], has been developed to be used in both laboratory measurements and test-beam campaigns. It reduces the effort of taking new pixel sensor prototypes into operation by maximizing the fraction of common hardware and software blocks of the system while keeping chip-specific components to a minimum.

In addition, the flexible and modular test-beam data reconstruction framework *Corryvreckan* [15] has been developed. It fulfils the requirements of a complex offline event building in data taking environments combining detector subsystems with different readout architectures.

2 Depleted monolithic CMOS Sensors for the CLIC Tracking Detector

For the tracking detector with its large area of ~140 m² fully monolithic CMOS technologies are considered the best choice due to their cost efficiency and large-scale production capabilities. In addition, they allow for a reduced material budget compared to hybrid technologies.

A high voltage CMOS sensor with a large collection diode, the *ATLASpix_Simple* [16], has been characterised both in laboratory and test-beam measurements and initial results have been presented in [5]. Recent results focussing on a comparison of different substrate resistivities are presented in Section 2.1.

3D TCAD simulations and previous test results have led to the development of innovative design concepts for CMOS sensors with a small collection electrode [17]. These have been implemented in various prototype chips targeting both CLIC and other future projects. The *CLICTD* chip [18] has recently been produced using a modified 180 nm CMOS imaging process implemented on a

high-resistivity epitaxial layer. The design includes an innovative sub-pixel segmentation scheme, and first results are presented in Section 2.2.

2.1 The ATLASp_{ix}_Simple HV-MAPS Prototype

The *ATLASp_{ix}_Simple* sensor is a High-Voltage Monolithic Active Pixel Sensor (HV-MAPS), which was designed as a candidate for the ATLAS ITk upgrade [16] but also targets the requirements of the CLIC tracking detector.

It was produced in a commercial 180 nm HV-CMOS process on wafers with substrate resistivities between 20 and 200 Ωcm and features an active matrix consisting of 25 columns and 400 rows of pixels with a pitch of 130 × 40 μm². A photograph is shown in Figure 1.

As depicted in Figure 2, each pixel consists of a large collection electrode, which is placed in a deep N-well on a p-substrate and houses the in-pixel electronics comprising charge-sensitive amplifier and comparator. After production, the sensors can be thinned down to 50 μm by removing undepleted bulk material from the backside. A high bias voltage of up to $O(100\text{ V})$ leads to a large depleted volume with a high electric field resulting in a fast charge collection via drift.

For each hit, the time-of-arrival (ToA) is recorded with 10 bit a precision and a binning of 16 ns. In addition, the signal charge is determined with a time-over-threshold (ToT) measurement with a 6 bit precision. The pixel matrix is read out in a data-driven column-drain scheme.

It has previously been shown that the measured spatial resolution of the *ATLASp_{ix}_Simple* in column and row direction is approximately the pixel pitch/ $\sqrt{12}$. This corresponds to a binary resolution and is in agreement with the fact that almost no charge is shared with neighbouring pixels [5].

2.1.1 Hit Detection Efficiency for Different Substrate Resistivities

The hit detection efficiency and its dependence on the detection threshold as well as the bias voltage have also been studied in DESY-II test-beam campaigns. The results are shown in Figure 3.

As can be seen in Figure 3a, the efficiency drops with an increasing detection threshold. Comparing the different substrate resistivities, it drops significantly slower for the 200 Ωcm sample than for the lower substrate resistivities. As a consequence, the 200 Ωcm sample can be operated for a much larger range of the threshold while maintaining a high detection efficiency.

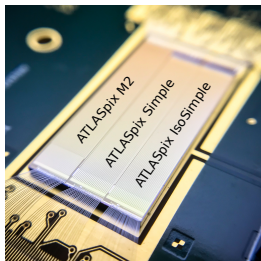


Figure 1. Photograph of an *ATLASp_{ix}* sensor with its three submatrices glued and wire-bonded to a printed circuit board.

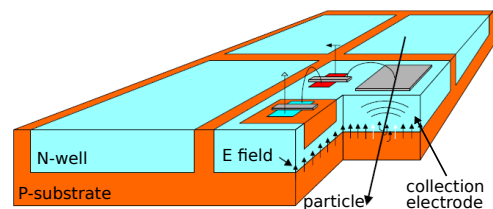
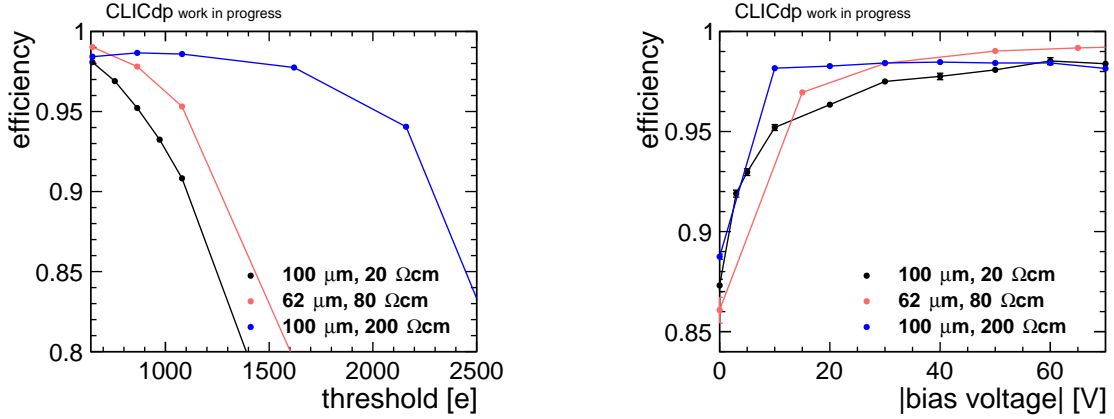


Figure 2. Schematic drawing of the HV-MAPS concept [19] (modified).



(a) Threshold dependence at a bias voltage of -50 V.

(b) Bias voltage dependence at a detection threshold of $650 e^-$.

Figure 3. Hit detection efficiency of *ATLASpix_Simple* samples with different substrate resistivities and thicknesses.

This behaviour is expected because a higher substrate resistivity leads to a larger depleted volume for a given bias voltage as described in Section 2.1.2. Consequently, the signal induced by the generated charge carriers of an incident particle is larger so that it can exceed the detection threshold for higher thresholds before becoming inefficient.

Figure 3b shows how the hit detection efficiency changes with the applied bias voltage. It can be observed that the efficiency rises with increasing bias voltage. For the lower resistivities, the efficiency saturates only slowly whereas it already reaches a stable plateau at a bias voltage around 10 V for the 200 Ωcm. Therefore, the 200 Ωcm sample becomes fully efficient at a much lower bias voltage.

Also this observation meets the expectation since a higher substrate resistivity leads to a larger depleted volume for a given bias voltage. In return, the 200 Ωcm sample reaches a given depleted volume, and therefore a given signal size, for a smaller applied bias voltage. Consequently, it becomes fully efficient at a lower bias voltage.

It should be noted that the sensor thickness is not expected to have an influence on the hit detection efficiency because by the thinning only undepleted bulk material is removed from the back of the sensor and the contribution to the charge collection from the undepleted bulk is insignificant.

2.1.2 Timing Performance for Different Substrate Resistivities

The timing performance for the different substrate resistivities of the *ATLASpix_Simple* has been determined in measurement campaigns at the DESY-II test-beam facility [20] using an EUDET-type beam telescope [21] and an additional Timepix3 plane [22] as a timing reference.

Figure 4 shows 2D histograms of the seed pixel ToT of a cluster on the *ATLASpix_Simple* plotted against the time residual of the reference track and the associated cluster on the *ATLASpix_Simple*. The reference track timestamp has been assigned by a Timepix3 plane [22] with a precision of 1.56 ns [23]. The seed pixel of a cluster is the one with the earliest timestamp, which is used to

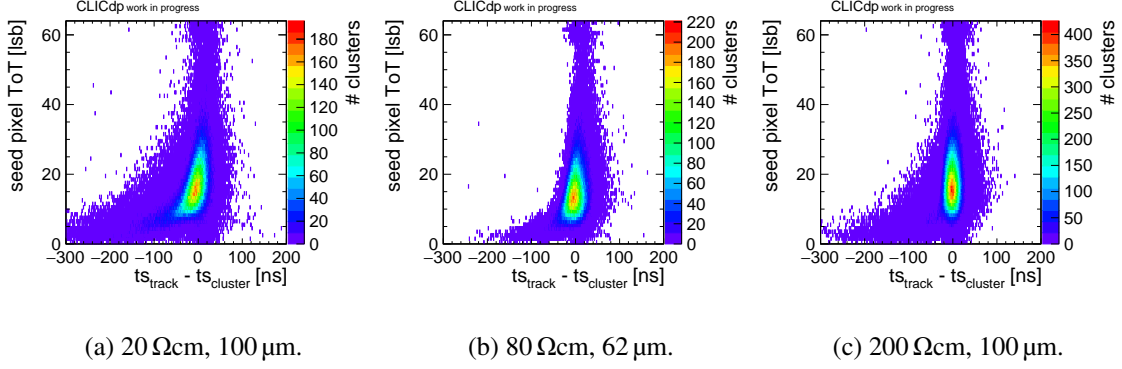


Figure 4. Track-cluster time residual versus the seed pixel ToT of ATLASp_{ix} samples for different resistivities and thicknesses at a detection threshold of $650 e^-$ and a bias voltage of $-50 V$ before applying any correction.

define the timestamp of the whole cluster. The ToT is a measure of the signal size, i.e. a large ToT corresponds to a large signal size. A clear dependence of the peak position of the time residual on the seed pixel ToT can be observed for the low substrate resistivity of $\sim 20 \Omega\text{cm}$ (see Figure 4a). This effect, referred to as timewalk, is strongly reduced with increasing substrate resistivity (see Figures 4b and 4c).

The dependence on the substrate resistivity can be explained as follows. A higher substrate resistivity leads to a larger depleted volume for a given bias voltage. As a consequence, more charge carriers can move freely and the induced signal is higher. This means that the crossing of the detection threshold is steeper and less affected by jitter. In addition, a larger electric field leads to a faster charge collection due to a shorter drift time of the charge carriers. Hence, the timewalk effect is expected to be less pronounced.

A correction for a row-dependent signal delay as well as a timewalk correction of the cluster timestamp have been applied offline. The resulting time residuals are shown in Figure 5 for the three investigated substrate resistivities at equal operating conditions with a threshold of around $650 e^-$

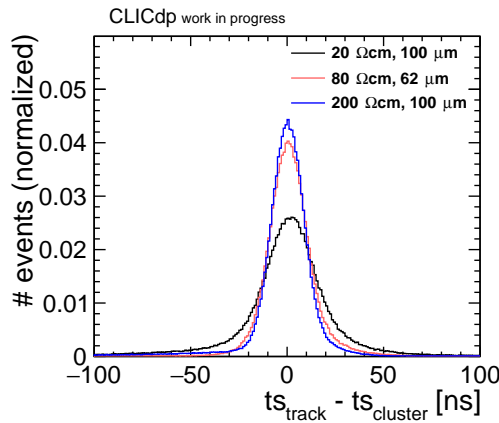


Figure 5. Comparison of the track-cluster time residual for ATLASp_{ix}_Simple sensors with different substrate resistivities and thicknesses after row-dependent and timewalk correction.

Table 2. Comparison of the time resolutions for *ATLASpix_Simple* samples with different substrate resistivities at a threshold of $\sim 650 e^-$ and a bias voltage of -50 V. The quoted uncertainties correspond to the errors on the fit.

substrate resistivity [Ωcm]	thickness [μm]	σ [ns]
20	100	13.3 ± 0.04
80	62	9.4 ± 0.03
200	100	8.3 ± 0.02

and a bias voltage of -50 V. Gaussian fits have been performed to determine the time resolution as the standard deviation σ of the fit function. The results are summarized in Table 2.

As in Figure 4, a clear dependence on the substrate resistivity is observed and can be explained in the same way. Hence, the timewalk effect is expected to be less pronounced and the timing resolution is better. The overall best result of $\sigma \sim 6.8$ ns was obtained with a $200 \Omega\text{cm}$ sample at a threshold of $480 e^-$ and a bias voltage of -50 V.

It should be noted that all measured time residuals contain a contribution of about 1.56 ns from the time resolution of the reference track timestamp.

2.2 The CLICTD HR-CMOS Prototype

The *CLICTD* sensor has been designed to meet the requirements of the *CLIC* tracking detector. It is fabricated in a modified CMOS imaging process, which has been optimised with the help of 3D TCAD studies [17]. The chip features a matrix of 128×128 pixels with a pitch of $37.5 \times 30 \mu\text{m}^2$. A photograph is shown in Figure 6. In an innovative readout segmentation scheme, 8×1 pixels each are combined into a single readout channel with a combined 8-bit ToA measurement with 10 ns binning and a 5-bit ToT measurement. This scheme allows to save space for digital circuitry while maintaining the small-collection electrode design at a low pixel pitch [18].

The sensor has been characterised both in laboratory and test-beam measurement campaigns.

2.2.1 Hit Detection Efficiency

Measurements at the DESY-II test-beam facility [20] show that the *CLICTD* sensor can be operated fully efficiently, i.e. with a hit detection efficiency above 99.8% for threshold values below $400 e^-$, as can be seen in Figures 7a and 7b. It has been measured down to a threshold of $150 e^-$, where the

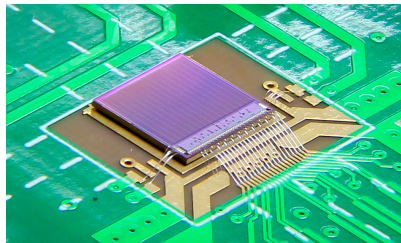
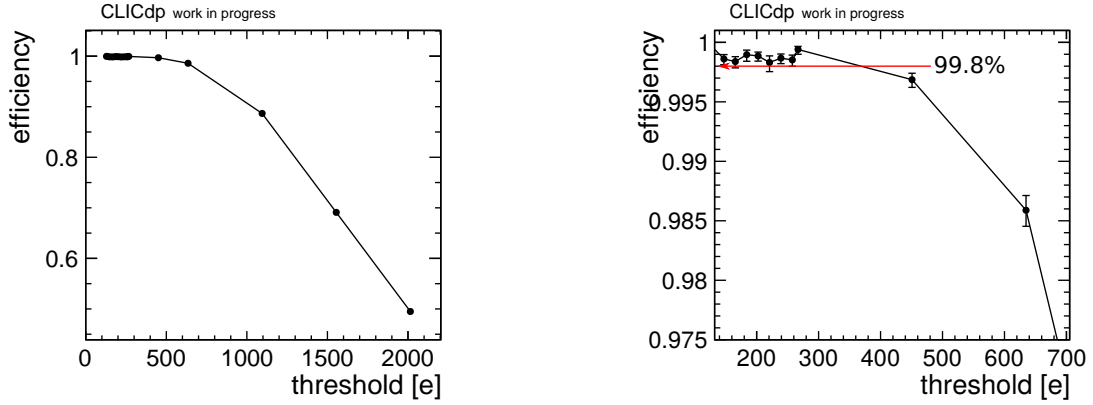


Figure 6. Photograph of a *CLICTD* sensor glued and wire-bonded to a printed circuit board.



(a) Hit detection efficiency for a threshold range from 150 to 2500 e^- .

(b) Hit detection efficiency for a threshold range from 150 to 700 e^- .

Figure 7. Hit detection efficiency measurements for a *CLICTD* sample.

sensor can be operated without noise hits. At thresholds above 400 e^- , the hit detection efficiency drops because the induced signal of the collected charge is less likely to cross the detection threshold.

As the in-pixel distribution of the hit detection efficiency in Figure 8 reveals, the efficiency remains high in the centre of a pixel and drops towards edges and especially the corners. This is explained by an increased amount of charge sharing into the neighbouring cells for particles incident close to the edges and corners of the sensor. As a consequence, the collected charge per pixel is smaller and the induced signal is less likely to cross the detection threshold.

2.2.2 Timing Performance

The time resolution of the *CLICTD* sensor can be deduced from the width of the time residual between the track timestamp and the *CLICTD* cluster timestamp, which is defined as the earliest pixel timestamp within the cluster.

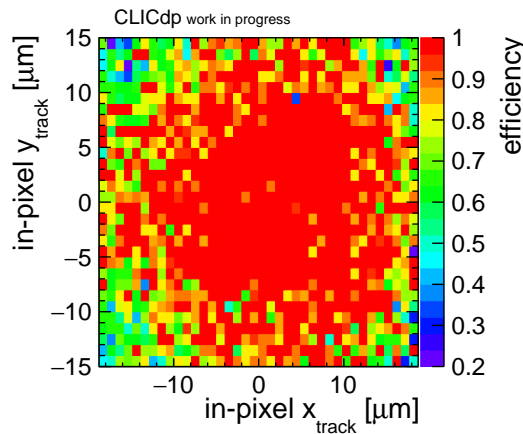
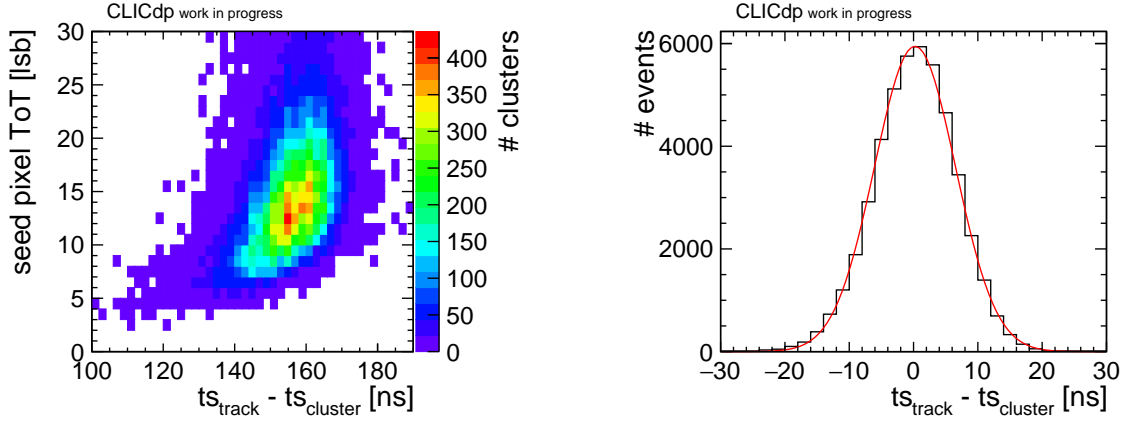


Figure 8. In-pixel hit detection efficiency of a *CLICTD* sample for a threshold of 1500 e^- .



(a) Track-cluster time residual vs. seed pixel ToT of the *CLICTD*.

(b) Track-cluster time residual after timewalk correction.

Figure 9. Timing performance measurements for the *CLICTD*.

Figure 9a, which shows the track-cluster time residual plotted against the seed pixel ToT of the cluster, reveals a clear timewalk effect. A timewalk correction can be applied offline to improve the time resolution. The result is shown in Figure 9b. A Gaussian fit to the time residuals results in a time resolution of $\sigma \sim 6.3$ ns.

3 Summary and Outlook

The experimental conditions at the proposed linear e^+e^- collider *CLIC* pose stringent requirements on the detector performance. To meet these requirements, an all-silicon vertex and tracking detector system is foreseen, for which a diverse R&D programme is being pursued in order to identify suitable technologies. As part of these efforts, hardware and software tools for simulation, data acquisition, as well as test-beam analysis have been developed within the CLICdp collaboration.

For the ultra-low mass vertex detector, different small pitch hybrid technologies with innovative interconnection techniques are under investigation. For the large-scale tracking detector, the focus of the R&D lies on depleted monolithic CMOS technologies. Various sensor prototypes, such as the *ATLASpix_Simple* and the *CLICTD*, are being characterized in laboratory and test-beam measurement campaigns.

Samples of the *ATLASpix_Simple* HV-MAPS test chip with different substrate resistivities have been compared in view of the timing performance as well as the hit detection efficiency. The *ATLASpix_Simple* reaches hit detection efficiencies above 99.8% and a timing resolution of ~ 6.8 ns. A high substrate resistivity is essential both for an excellent timing behaviour as well as a larger operating window maintaining a high hit detection efficiency.

The *CLICTD* HR-CMOS sensor prototype has been designed to explore a novel readout segmentation scheme. A hit detection efficiency above 99.8% and a time resolution as good as ~ 6.3 ns have been measured.

In summary, the presented results show that HV-MAPS and HR-CMOS are promising technologies and have a large potential to be used in the *CLIC* tracking detector. Most of the detector

requirements are fulfilled by the test sensors and further prototypes with newer process technologies and improved designs are planned to be fabricated and tested in the future.

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