

CLICTD: A monolithic HR-CMOS sensor chip for the CLIC silicon tracker

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The CLIC Tracker Detector (CLICTD) is a monolithic pixelated sensor chip produced in a 180 nm imaging CMOS process built on a high-resistivity epitaxial layer. The chip, designed in the context of the CLIC tracking detector study, comprises a matrix of 16×128 elongated pixels, each measuring $300 \times 30 \mu\text{m}^2$. To ensure prompt charge collection, every elongated pixel is segmented in eight sub-pixels, each containing a collection diode and a separate analog front-end. A simultaneous 8-bit time measurement with 10 ns time bins and 5-bit energy measurement with programmable range is performed in the on-pixel digital logic. The main design aspects as well as the first results from laboratory measurements with the CLICTD chip are presented.

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1. Introduction

A novel monolithic pixel sensor chip, the CLIC Tracker Detector (CLICTD), is presented. The CLICTD chip features a matrix of 128 rows and 16 columns with pixels of $300 \times 30 \mu\text{m}^2$. The chip was designed according to the requirements for the silicon tracker at the future Compact Linear Collider (CLIC) [1]. These requirements include a Time of Arrival (ToA) measurement with 10 ns time bins, and a 5-bit Time over Threshold (ToT) measurement for time walk correction. Moreover, the 5-bit ToT measurement (which has a programmable range from 0.6 to 4.8 μs) enables a precise hit position interpolation that is needed to reach a single point resolution of $7 \mu\text{m}$ along the transverse plane with the pitch of $30 \mu\text{m}$. Other requirements include a total material budget of $1 - 1.5\% X_0$ per detection layer (allowing for $\sim 200 \mu\text{m}$ for the silicon layers) and an average power consumption below $150 \text{ mW}/\text{cm}^2$. In order to minimise the average analog power consumption, the analog front-end can be set to a standby power mode in the 20 ms gaps between subsequent colliding bunch trains (power pulsing), taking advantage of the low duty cycle of the CLIC beam [2]. The digital power consumption is minimised by means of clock gating. Details on the CLICTD chip design have been presented in [3].

2. Process description

The design was implemented in a 180 nm High-Resistivity (HR) CMOS imaging process, where a deep P-well is used in order to shield the on-pixel electronics from the collection electrode. The signal is collected with a small area N-well on top of a P-type high resistivity epitaxial layer. This results in a small capacitance (a few fF) for the collection electrode and helps to minimise the analog power consumption and the noise in the front-end. Full depletion of the epitaxial layer is achieved by including an additional deep N-type implant. Two different pixel layouts were implemented and manufactured through a process split on different wafers. As illustrated in Figure 1, the first pixel layout is with a continuous deep N-type implant, and the second with a segmented deep N-type implant to increase the lateral field and thereby reduce the charge collection time [4]. In addition, reduced charge sharing is expected because of the gap in the N-implant. The gap is introduced only along the long dimension of the pixel, as the short pixel dimension corresponds to the transverse detector plane, where charge sharing can be beneficial for improving the position resolution through hit position interpolation.

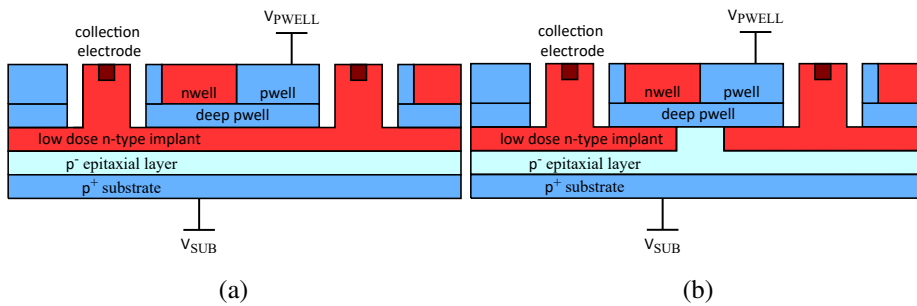


Figure 1: The two process splits: (a) continuous N-implant, and (b) gap in N-implant (not to scale).

3. The CLICTD prototype chip

The CLICTD matrix comprises 16×128 elongated pixels of $300 \times 30 \mu\text{m}^2$. Each pixel is segmented in eight sub-pixels, each with its individual collection diode and analog front-end, to

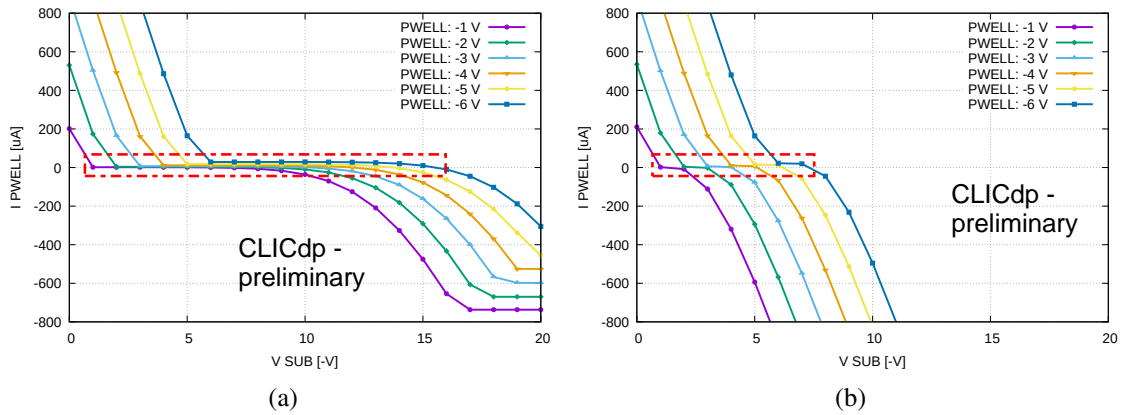


Figure 2: Leakage current measured at the P-wells in the CLICTD matrix as a function of the substrate bias, for different values of the P-well bias. CLICTD sample from (a) the first process option - continuous N-implant, and (b) the second process option - gap in N-implant.

ensure prompt charge collection. The diodes are therefore spaced by $37.5 \mu\text{m}$ along the long pixel direction. Every front-end includes level shifter, voltage amplifier, discriminator and a 3-bit local threshold tuning DAC. The level shifter acts as a unity gain buffer and is placed as close to the collection electrode as possible to minimise the input capacitance. One bit indicating whether the front-end detected a particle is stored for each sub-pixel, while the simultaneous 8-bit ToA and 5-bit ToT measurement is performed in the on-pixel digital logic for the combined output (by means of an "OR" gate) of all eight discriminator outputs. Thus, the time-stamp of the first hit and the integral ToT of all hits within the same frame are read out for each pixel. A serial readout at 40 MHz is employed. To reduce the amount of data shifted out of the chip, a compression algorithm is applied. The data acquired during the frame are shifted out only for pixels that detected a particle. For pixels that did not detect a particle, only one bit is shifted out.

4. Measurement results

Once fabricated, the CLICTD chip was characterised using the CaRIBOu readout system [5].

4.1 I-V characteristic

The sensor bias operation range was determined by measuring its I-V characteristics. The leakage current at the P-wells in the pixel area (biased at V_{PWELL} in Figure 1) was measured, while scanning the substrate bias voltage, and for given values of the P-well bias ranging from -1 to -6 V. The region where the leakage current remains stable and relatively low ($< 20 \mu\text{A}$ for the full chip) is the region where the sensor can be operated (marked in red in Figure 2). For the first pixel layout in Figure 1a, the continuous deep N-type implant offers a better isolation between the P-wells and the substrate. Therefore, the substrate can be biased to a higher (in absolute value) voltage, as shown in Figure 2a. Due to the reduced isolation originating from the gap in the deep N-type implant in the second pixel layout, the sensor can be operated only when the two nodes are biased at a similar voltage level (Figure 2b), a result which is in agreement with simulations [4].

4.2 Noise measurements and equalisation

During the threshold equalisation for the CLICTD pixel matrix, the baseline for each sub-pixel is extracted as the mean value of the curve produced after scanning the threshold and counting the number of noise hits for each threshold. In order to equalise the matrix on a sub-pixel basis, the

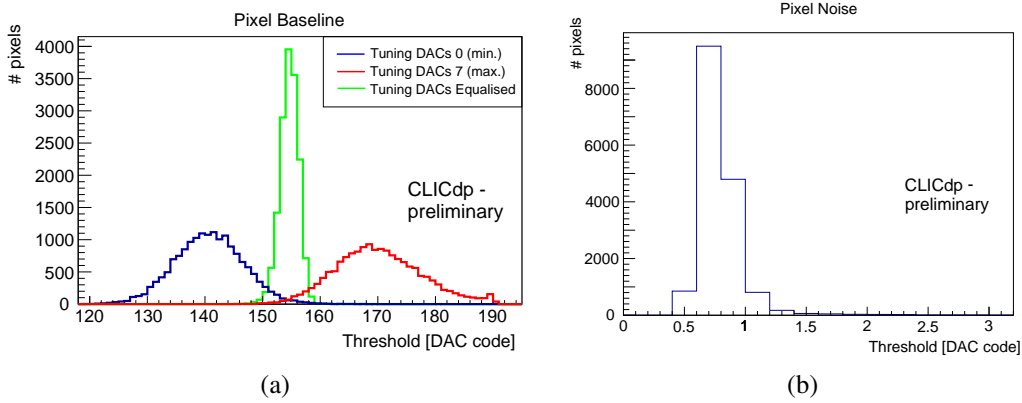


Figure 3: (a) Distribution of pixel baselines obtained from threshold scans before (blue, red) and after (green) equalisation. (b) Histogram of noise RMS per sub-pixel, in threshold DAC codes.

scan was performed for each of the eight sub-pixels in the pixel, while the rest of the sub-pixels were masked. The threshold scans were performed for the lowest and highest code of the 3-bit threshold tuning DAC in the front-end. A linear interpolation was applied in order to select the DAC codes for which the threshold dispersion over the matrix is minimised. Figure 3a presents the threshold scan for lowest (blue curve), highest (red curve) and equalised (green curve) DAC code. A histogram of the noise RMS per sub-pixel, extracted in threshold DAC codes as the RMS value of the curve resulting from the threshold scan for each sub-pixel, is plotted in Figure 3b. Based on the threshold DAC step to electrons conversion extracted in Section 4.3, the threshold dispersion for the equalised CLICTD matrix is about $25 e^-$ and the mean value of the noise RMS is $13 e^-$. The above results are from a CLICTD sample with gap in the n-layer, with both the P-wells and the substrate biased to $-2 V$.

4.3 Measurements with radiation sources

Figure 4a presents the fluorescence spectra from an iron (red curve) and a copper (blue curve) target, measured with the CLICTD chip using an X-ray beam. The CLICTD threshold was scanned during this measurement and the number of detected photons was stored in each pixel and read out for every threshold. The produced occupancy curve gives the number of counts above threshold, for each applied threshold step. For a given beam intensity and frame duration, this number depends on the fluorescence emission spectrum of the target. A differentiation of the occupancy curve gives the measured energy spectrum.

From the mean values of the Gaussian fits for the K_α peaks for iron (6.4 keV) and copper (8.04 keV), and with an electron-hole pair creation energy in silicon of 3.62 eV, the LSB of the threshold DAC has been extracted to correspond to $\sim 16 e^-$. The minimum detectable charge for the chip settings applied for this measurement is estimated to be $\sim 300 e^-$.

Using the same setup, an X-ray image of a small item (screw) was taken with the CLICTD chip. The image presented in Figure 4b was produced with 1000 acquisitions of 4 ms shutter length, with equalised matrix. The number of frames when a hit was detected is plotted for each sub-pixel.

For the above measurements, a CLICTD sample with continuous N-implant was used, while the reverse bias was set to $-2 V$ at the P-wells and to $-4 V$ at the substrate. The sensor capacitance (and consequently the front-end performance) strongly depends on the sensor bias [6]. The

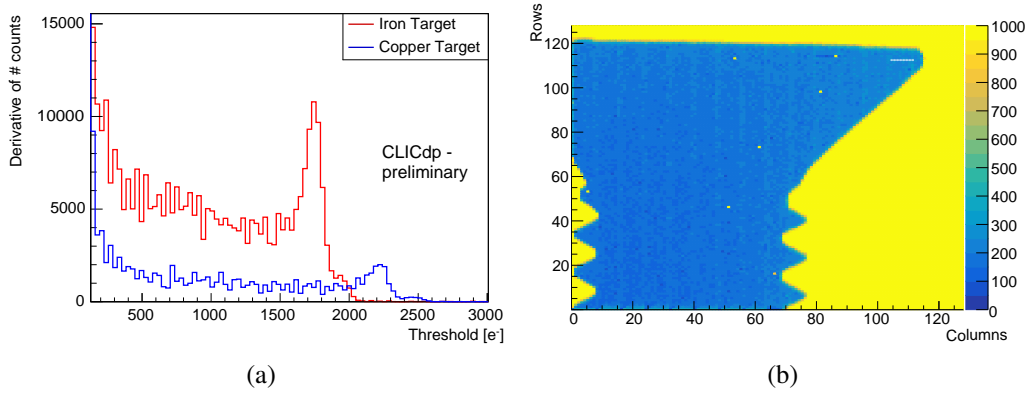


Figure 4: (a) Fluorescence spectra using iron (red) and copper (blue) targets, measured with the CLICTD chip. (b) X-ray image of a screw, recorded with the CLICTD chip.

front-end was biased at its default values after chip reset and the operation parameters were not yet tuned for signal-to-noise performance. Under these bias conditions, the analog part of the matrix consumes ~ 170 mW/cm², while the on-pixel digital logic consumes another 240 mW/cm². The expected average power consumption of the CLICTD matrix over the cycle of the CLIC accelerator, as extrapolated from static power measurements and simulated values, is ~ 5 mW/cm², after applying the power pulsing scheme introduced in Section 1. In addition, 43 mW are consumed by the analog and digital periphery electronics.

5. Summary

A monolithic sensor chip, the CLIC Tracker Detector (CLICTD), designed in the framework of the CLIC silicon tracker study, has been presented. The chip was produced in a modified CMOS imaging process and features a novel architecture with segmented pixels. Preliminary results show a threshold dispersion of 25 e⁻ and a mean noise RMS of 13 e⁻ over the CLICTD matrix, after threshold equalisation. The average power consumption over the CLIC beam cycle is estimated to be ~ 5 mW/cm² for the pixel matrix, plus 43 mW for the periphery electronics.

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