**The Compact Muon Solenoid Experiment**
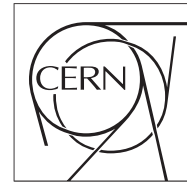
# Conference Report

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# Performance study of HGCROC-V2: the front-end electronics for the CMS High Granularity Calorimeter

Damien Thienpont for the CMS Collaboration

**Abstract**

The High Granularity Calorimeter (HGCAL), presently being designed by the Compact Muon Solenoid collaboration (CMS) to replace the existing endcap calorimeters for the High Luminosity phase of the LHC, will feature unprecedented transverse and longitudinal readout and triggering segmentation for both electromagnetic and hadronic sections. The requirements for the front-end electronics are extremely challenging, including high dynamic range (0-10 pC), low noise ( 2000 electrons), high-precision timing information in order to mitigate the pileup effect (25 ps binning) and low power consumption ( 15 mW/channel). The front-end electronics will face a harsh radiation environment which will reach 200 Mrad at the end of life. It will work at a controlled temperature of 240 K. HGCROV-V2 is the second prototype of the front-end ASIC. It has 72 channels of the full analog chain: low noise and high gain preamplifier and shapers, and a 10-bit 40 MHz SAR-ADC, which provides the charge measurement over the linear range of the preamplifier. In the saturation range of the preamplifier, a discriminator and TDC provide the charge information from TOT (Time Over Threshold) over 200 ns dynamic range using 50 ps binning. A fast discriminator and TDC provide timing information to 25 ps accuracy. Both charge and timing information are kept in a DRAM memory waiting for a Level 1-trigger decision (L1A). At a bunch crossing rate of 40 MHz, compressed charge data are sent out to participate in the generation of the L1-trigger primitives. We report on the performances of the chip in terms of signal-to-noise ratio, charge and timing, as well as results from radiation qualification with total ionizing dose (TID).

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# Performance study of HGCROC-v2: the front-end electronics for the CMS High Granularity Calorimeter

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ABSTRACT: The High Granularity Calorimeter (HGCAL), presently being designed by the Compact Muon Solenoid collaboration (CMS) to replace the existing endcap calorimeters for the High Luminosity phase of the LHC, will feature unprecedented transverse and longitudinal readout and triggering segmentation for both electromagnetic and hadronic sections. The requirements for the front-end electronics are extremely challenging, including high dynamic range (0-10 pC), low noise (~2000 electrons), high-precision timing information in order to mitigate the pileup effect (25 ps binning) and low power consumption (~15 mW/channel). The front-end electronics will face a harsh radiation environment which will reach 200 Mrad at the end of life. It will work at a controlled temperature of 240 K.

HGCROV-V2 is the second prototype of the front-end ASIC. It has 72 channels of the full analog chain: low noise and high gain preamplifier and shapers, and a 10-bit 40 MHz SAR-ADC, which provides the charge measurement over the linear range of the preamplifier. In the saturation range of the preamplifier, a discriminator and TDC provide the charge information from TOT (Time Over Threshold) over 200 ns dynamic range using 50 ps binning. A fast discriminator and TDC provide timing information to 25 ps accuracy. Both charge and timing information are kept in a DRAM memory waiting for a Level 1-trigger decision (L1A). At a bunch crossing rate of 40 MHz, compressed charge data are sent out to participate in the generation of the L1-trigger primitives.

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## Contents

## 1. Introduction

As described in [1], the entire electromagnetic section and part of the hadronic section of the HGCAL consist of hexagonal silicon sensors while the rest of the hadronic section in the lower radiation region will be made of SiPM-on-scintillator tiles. The SiPM-readout chip is made by only adding a current conveyor and adapting the preamplifier of the silicon version. This paper focuses on the architecture and performance of the latter.

## 2. Architectural overview

The HGCROC-V2 chip is made of: 72 channels of the full analog chain achieving charge and timing information; 4 common mode channels for subtracting coherent noise; 2 calibration channels for the MIP calibration. Four 1.28 Gbps links are devoted to send out an image of the deposited charge of each bunch crossing event by summing and compressing data over 4 (or 9) channels. These data will contribute to the L1 trigger generation. Two more 1.28 Gbps links are dedicated to send out the full event information (charge and time) of selected bunch crossings after a L1 trigger request.

The I2C protocol is used to set or read the more than 7900 parameters of the chip. This part is triplicated to resist to the Single Event Effect (SEE). The chip is controlled by the Fast Command block which receives a clock and a command link at 320 MHz. This allows to configure the operating mode of the system: link synchronization, reset, calibration, L1 request, etc. The 40 MHz clock, in phase with the LHC clock, is extracted from the 320 MHz fast command link and provides the clock to the digital part of the ASIC (digital processing, I2C) and to the PLL which generates the others clocks needed to operate the chip: the 640 MHz clock for the 1.28 Gbps links,

the phase adjustable 40 MHz clock for the ADCs, the phase adjustable 160 MHz clock for the TDCs. Indeed it is needed to be able to adjust the phase of the conversion blocks (ADC and TDC) to the phase of the physical signals which depend on the rapidity angle.
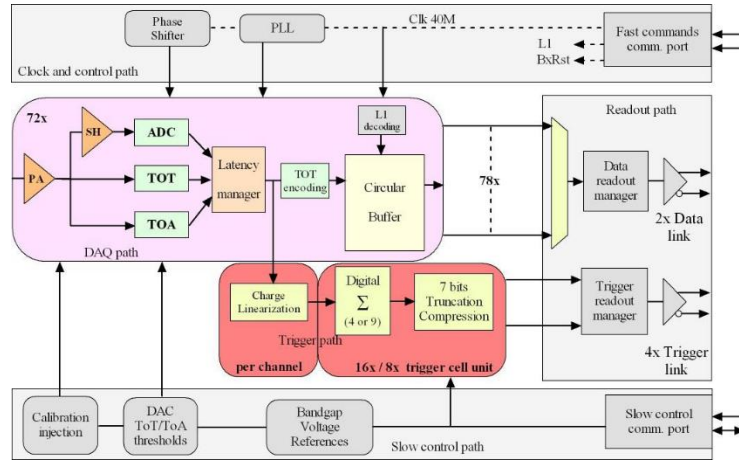


Figure 1: architectural overview of HGCROC-V2

The analog front-end is made of three distinct sub-parts:
- The low-noise preamplifier which converts the input charge from the silicon diode into an output voltage. As the value of the MIP depends on the sensor thickness and on the irradiation, the preamplifier gain is programmable so that the ADC range covers an energy range corresponding to 100 times the energy deposited by a minimum ionizing particle (MIP). A specific requirement is also not to have more than 20% of the signal in the next bunch crossing in order to mitigate the pile-up effect: this is achieved by the preamplifier constant time feedback.
- The shaper is made of three stages: a first gain-2 Sallen-Key shaper; a gain-3 RC² shaper; a unity gain buffer to drive the signal to the ADC.
- A discriminator provides the charge measurement when the preamplifier saturates by using the Time Over Threshold (TOT) technique. Another one provides the timing information by measuring the Time Of Arrival (TOA).

The charge information is given by the 10-bit SAR ADC (see [2]) in the linear range of the preamplifier. A dedicated 10-bits TDC measures the time of the TOA discriminator. Another 12-bits TDC measures the time of the second edge of the TOT discriminator which gives the charge information when the preamplifier saturates by subtracting the TOT time and the TOA time.

## 3. Performance study

A first characterization board has been developed where the chip is flipped on a mezzanine; all the power supplies remain separated (7 analog and 4 digital). This version makes it possible to check the performance of the circuit in an optimistic framework since the possible couplings via the power supplies are reduced. With this board, no coupling of the digital part appears on the signals converted by the ADCs as shown in Figure 2. The noise measured on the pedestals is around 1 ADC unit.

Another board has been developed to validate the operation of the circuit in a BGA. Here, the power supplies are all combined to leave only two global power supplies: one for the analog

domain and another for the digital domain. We now observe a coupling of the digital clock on the waveforms. The effective noise is only slightly higher (1.25 ADC unit), which is normal since the ADCs sample the signal at constant phase compared to that of the digital domain. It is the reason why this coupling does not disturb the charge measurement of the ADCs. But this is not the case for the TOA and TOT measurements since the edges of the discriminators will arrive asynchronously with respect to the global clock.

The difference found is attributed to the grounding of the BGA lead frame, which will be corrected in the future.
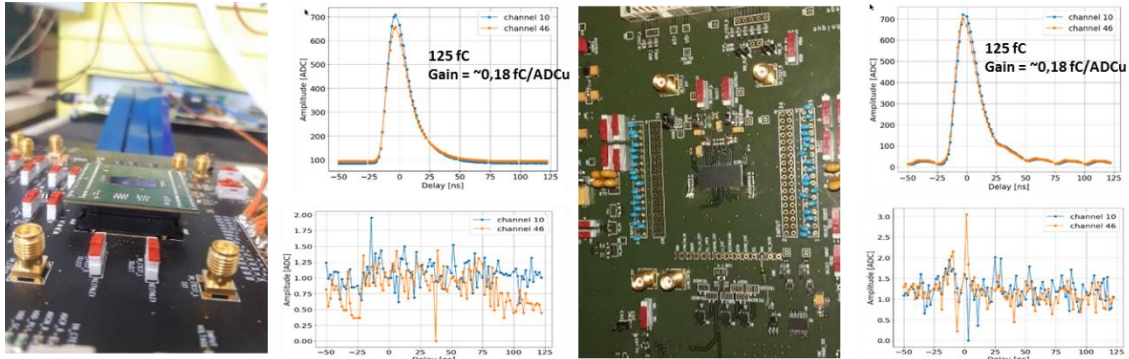


Figure 2: on the left hand side, the "FlipChip" board, waveforms and noise; on the right hand side, the "BGA" board, waveforms and noise.

## 3.1 General performance

A calibration pulser, based on an 11-bit DAC, has been integrated into the chip to emulate a charge injection (up to 8 pC). The measured performance shows a good linearity of +/- 0.1% of the full dynamic range. But with an unexpected offset of around 30 mV, limiting the minimum charge to be injected to ~ 15 fC (5 – 10 MIPs) whilst 0 fC was expected. This is due to the fact that the calibration DAC ground has been tied to the reference voltage grounding rather than the preamplifier ground: this will be easily corrected in the future.

## 3.1.1 Noise performance

An important parameter is the noise performance of the chip. The series noise whose main contributor is the input transistor of the preamplifier depends on the detector capacitance value. The measurements show a series noise of 0.7 nV/√Hz and a preamplifier input capacitance of 6 pF in accordance with the simulations and the specifications.

In the final system, the high voltage, needed to bias the silicon sensor, could be an important coherent noise source. It is so required to keep as low as possible all sources of coherent noise of the chip itself. By comparing direct ($DS = \sum ch[i]$) and alternate ($AS = \sum (-1^i) ch[i]$) sums of the 72 channels, the incoherent ($IN = rms(AS)/\sqrt{n}$) and coherent ($CN = \sqrt{[var(DS)-var(AS)]/n}$) noises may be extracted. We find 5% of coherent noise for the flipchip board and 10% for the BGA board.
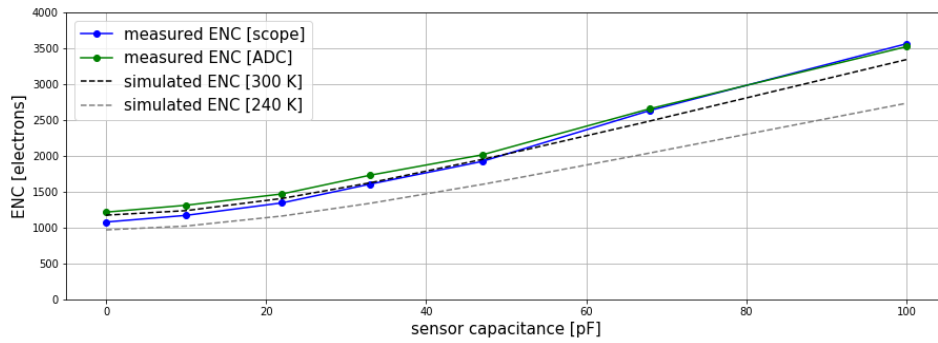
Figure 3: Equivalent Noise Charge as a function of the sensor capacitance.

### 3.1.2 Charge measurement performance

The ADC range achieves a linearity within +/- 0.5 % as shown in the figure 4. Because of the calibration DAC offset, the lowest injected charge is around 20 fC and not 0 fC: the first point is given by measuring the pedestal.

From and beyond the preamplifier saturation, the TOT provides the charge measurement. The residuals measurement show that the linearity remains below +/- 0.5 %. The 40 MHz digital coupling is clearly visible with the BGA version: this effect will be hopefully removed by reproducing the power and grounding policy of the FlipChip into the BGA. As expected by calculation, the TOT achieves a better linearity with a sensor capacitance, as shown in the figure 6. The Standard Deviation measurement show excellent overall resolution around the LSB (50 ps). Whether some spikes due to the TDC Differential Non-Linearity (DNL) appear, they can be reduced by global adjustment of the Master TDC: for instance the channel 2 of the figure 5 had twice higher spikes before this adjustment. Dedicated TDC characterization have shown that it is possible to further improve the DNL, and so the spikes in the resolution curve, by applying channel-wise adjustment. The result of this work shall be reported in a subsequent paper.
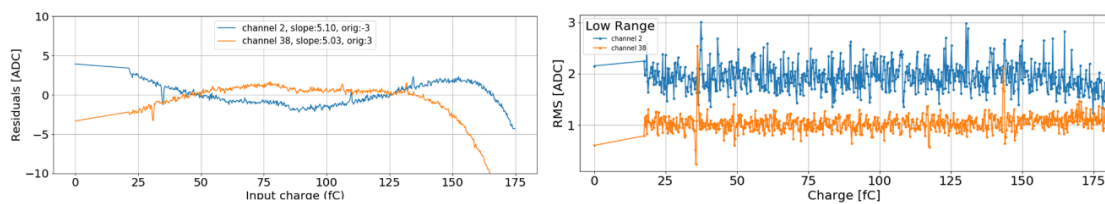


Figure 4: Charge residuals (left) and rms (right) in the "ADC range". 47 pF sensor capacitance on channel 2; no sensor capacitance on channel 38.
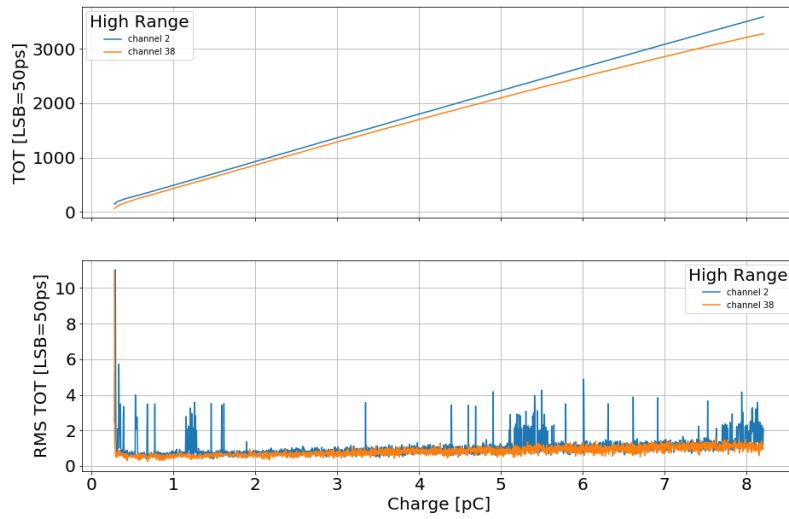
Figure 5: Charge linearity (top) and jitter (bottom) in the "TOT range". 47 pF sensor capacitance on channel 2, no sensor capacitance on channel 38: the spikes on the blue curve are not due to the sensor capacitance but to a poor DNL caused by random mismatch in the TDC of the channel 2.
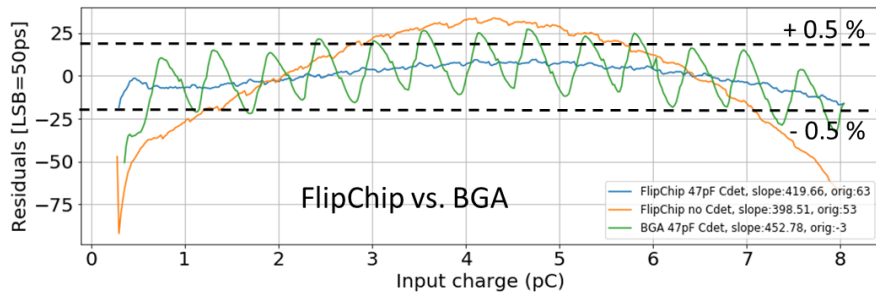


Figure 6: Residuals of the TOT as a function of the charge. Blue: FlipChip and 47 pF sensor capacitance. Orange: FlipChip and no sensor capacitance. Green: BGA and 47 pF, the 40 MHz coupling is clearly visible.
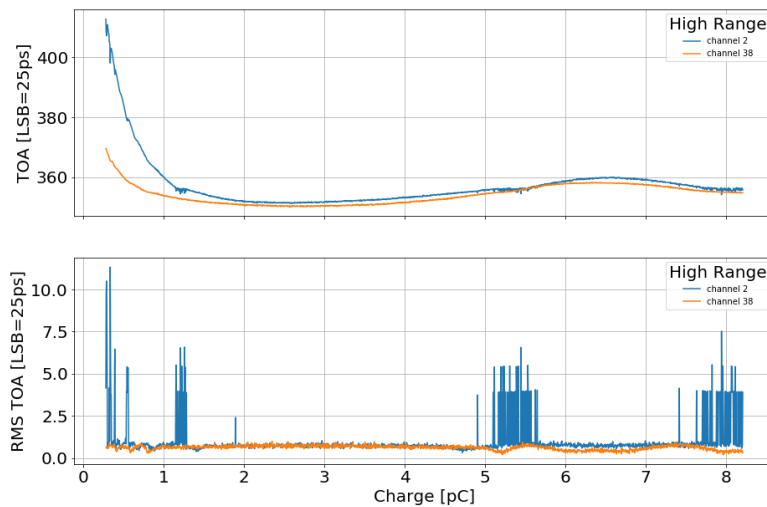


Figure 7: Time Walk (top) and jitter (bottom) as a function of the charge.

### 3.1.3 Time measurement performance

In order to mitigate the proton collisions pile-up effect, an accurate timing information – "the 5$^{th}$-dimension measurement" – is needed. The extremely challenging specification of 100 ps at 10 MIPs (15 – 30 fC) and a jitter floor below 25 ps are specified. The first promising measurements show a jitter floor around 25 ps, and around 200 ps at 20 fC as shown in figure 7.

Beyond the jitter requirement, the Time-Walk (TW) must be stable and well reproducible as it will be corrected off-line. The first measurements show a TW with 50 pF around 7 ns in accordance with the simulation. A bump appears at high charge which can be reproduced in simulation and should be removed in the next iteration of the chip. Further measurements are needed to validate the reliability of the TW.

### 3.2 Specific performance

### 3.2.1 Temperature sensitivity

Most of the previous measurements have been reproduced at cold temperature, down to minus 40°C. The shift of the pedestals is of 0.4 ADCU/°C around -30 °C which be made possible by compensating the temperature effects: it would be around 5 ADCU/°C otherwise. No obvious effect has been seen regarding the ADC gain, as well as the TOT and TOA performances.

### 3.2.2 TID results

The chip has been irradiated up to 310 Mrad in an X-Ray machine at room temperature. The ADC and TDC start to misbehave around 100 Mrad, but normal operation was recovered after 2-days annealing at room temperature. A second TID campaign is planned to better reproduce the real environment: a lower dose rate which should be less aggressive as the annealing operates at the same time; but also at low temperature as it is known the annealing is less efficient at cold. No obvious effect have been seen regarding the pure analog part. Expected shifts of power consumption and bias have been observed.

## 4. Conclusion

The first results of HGCROCv2 are very promising and a big step has been taken to reach the HGCAL's requirements. So far, the measurements of pedestals, noise, charge and time performance are within or close to the expected ones, at warm or cold temperature. The TID results are encouraging but need to be confirmed in cold conditions. Still a lot of things have to be checked such as the channel-wise adjustments for TDC tuning, the reliability of the ADC/TOT transition, and the reliability of the TW. The trigger path needs to be fully studied as well. All these measurements must be reproduced for the SiPM-version of the chip.

## References

[1] CMS Collaboration, *The Phase-2 Upgrade of the CMS Endcap Calorimeter*, *CERN-LHCC-2017-023,* 2017

[2] M. Firlej *et al.*, *A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors*, JINST 10 P11012, 2015