

Review

Introducing Timepix2, a frame-based pixel detector readout ASIC measuring energy deposition and arrival time

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ARTICLE INFO

Keywords:

particle energy deposition
Arrival time
Adaptive gain
Frame readout

ABSTRACT

The Timepix2 ASIC (application-specific integrated circuit) is the upgraded successor to the Timepix [1] hybrid pixel detector readout chip. Like the original, Timepix2 contains a matrix of 65k square pixels of 55 μm pitch that can be coupled to a similarly segmented semiconductor sensor, or integrated in an ionising gas detector. The pixels are programmable, with several operation modes and selectable counter depths (up to 18 bits for time-of-arrival, ToA, and up to 14 bits for time-over-threshold, ToT). In ToT and ToA mode, each pixel records the arrival time and energy deposited by particles interacting with the corresponding sensor segment, with an optional separation of timing resolution for ToT and ToA: down to 10 ns each. The gain of the frontend circuit can be programmed to adapt to the quantity of energy deposited in the sensor, yielding a large dynamic range of 0.38 ke^- to 950 ke^- . The frontend noise in adaptive gain mode is 380 e^- rms. The design also introduces some power optimisation features to the Timepix portfolio, such as power masking on selectable parts of the pixel matrix. With all pixels powered on, using 100 MHz for both ToT and ToA clock frequencies, and assuming a sparse particle interaction with the pixels, the matrix is estimated to consume less than 900 mW based on simulation.

1. Introduction

The Timepix family of chips (Llopert et al., 2007; Poikela et al., 2014) is a spinoff of the Medipix hybrid pixel detector development. Whereas the Medipix (Llopert et al., 2002; Campbell et al., 2018) chipset targets medical imaging and other photon (or particle) counting applications, the Timepix chips are intended for particle detection, in applications such as the characterisation of radiation in space. The original Timepix (Llopert et al., 2007) application-specific integrated circuit (ASIC), released in 2006 by the Medipix2 Collaboration (Llopert et al., 2002), contains 256 columns by 256 rows of square pixels of 55 μm pixel pitch that can be programmed to either record the time-of-arrival (ToA) or the energy deposition (time-over-threshold, ToT) of a particle

interaction in the sensor. Data from the chip is formatted in frames of uncompressed data from all 65k pixels, including pixels that did not record any particle interactions during the open shutter period. A readout deadtime results from the pausing of measurement during the readout of each frame. Following the successful use of Timepix in a variety of applications (Ballabriga et al., 2011), the Medipix3 Collaboration (Campbell et al., 2018) released the Timepix3² ASIC in 2014 (Poikela et al., 2014). Unlike Timepix, where readout is frame-based, data from Timepix3 is data-driven, whereby data is pushed off-chip as soon as a measurement is completed in each pixel. The Timepix3 data format includes the pixel address and both the ToA and ToT of the same particle interaction in the associated pixel sensor segment. The data-driven method permits long open shutter periods (because the pixel

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² Chronologically, Timepix3 predates Timepix2. The naming convention refers to the fact that the Timepix3 chip was developed by the Medipix3 Collaboration, whereas both Timepix and Timepix2 are from the Medipix2 Collaboration.

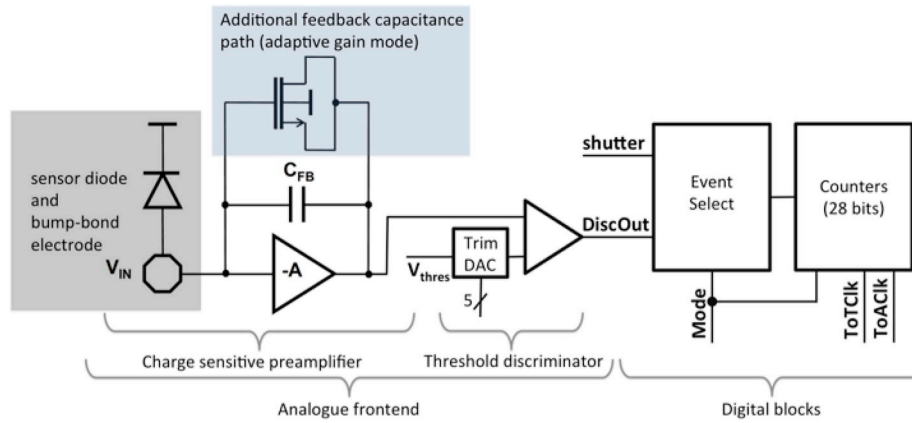


Fig. 1. Main pixel circuit blocks in regular operation.

storage elements are emptied and ready to characterise the next particle interaction almost immediately) and avoids the reading out of empty pixels. However, the data-driven file format also necessitates extra effort to sort and reformat the data off-chip. This work introduces the Timepix2 chip, developed by the Medipix2 Collaboration, which is intended to be a frame-based successor of the original Timepix.

The Timepix2 chip was developed in a commercial 130 nm deep sub-micron technology process. It contains 256 columns by 256 rows of square pixels of 55 μm pixel pitch. Data from the pixel matrix is typically output in full frames via either a 100 Mbps serial port or a 3.2 Gbps parallel bus. As a compromise between full-frame and data-driven readout schemes, an optional zero-column-suppression readout mode suppresses the readout of empty pixel columns when data is output from the serial port. Multiple chips integrated in a common system can be daisy-chained for readout and programming. Individual pixel power masking optimises power consumption to permit region of interest measurements, or to power down unused pixel electronics in hybrid pixel detectors where only a subset of pixels in the ASIC are bump-bonded to a sensor with an increased pixel pitch (e.g. of 110 μm). An optional matrix occupancy monitor flags the moment when the number of pixel columns with recorded hits has surpassed a programmed threshold of occupied columns. A set of digital pixels that contain the same digital functionality as regular pixels but without the analogue frontend, can be used to process discriminated signals from off-chip, allowing for coincidence measurements with external instruments. The wirebond pads at the bottom of the chip periphery are compatible with through-silicon-via chip-to-board interconnect technologies.

Each pixel in the regular matrix consists of an analogue frontend with an adaptive-gain preamplifier whose output is digitised by an energy-threshold discriminator. The digital half of the pixel circuitry contains state machines that select detected events, and counters that record ToT, ToA and/or the tally of particle hits. Although Timepix2 is a highly programmable, general-purpose detector chip, many of the design choices target the requirements of operation in mixed radiation fields with highly energetic particles, such as in space (Kroupa et al., 2015; Gohl et al., 2016). The feature upgrades of the Timepix2 pixels include simultaneous ToA and ToT measurement, separate ToA and ToT clock frequencies, monotonic behaviour in ToT even for high input charges, low minimum detectable energy due to low threshold dispersion, increased overall dynamic range (both analogue and digital), high energy resolution due to low frontend noise, fast clearing of data memory on the matrix, per pixel power masking, the ability to both program and read back individual pixel configuration settings, and separated analogue and digital calibration options with programmable test charge injection for the analogue frontend and digital test pulses for the digital state machines.

2. The pixel matrix

The Timepix2 ASIC architecture consists of a main matrix of 256 columns of 256 rows of 55 μm -pitch square pixels, and a chip periphery section containing global chip programming blocks, digital to analogue bias circuits, and readout blocks. The main matrix is the active area of the detector, where the pixel electronics are designed to be bump-bonded to a semiconductor sensor, such as a silicon pn junction diode segmented into pixels. All pixels in the matrix feature identical functions. The block diagram of Fig. 1 shows that a pixel consists of an analogue frontend followed by digital circuits that digitise and store the particle measurement for readout. An electronic shutter signal determines the period of measurement.

Energy deposited in a sensor segment from a charged particle induces a signal in the corresponding frontend input on the ASIC. The discriminator outputs a voltage pulse whose width is proportional to the energy deposition. Thus a measurement of the ToT provides a digital measurement of the energy absorbed in the sensor segment. Given that the Timepix2 pixel side-length is only 55 μm , a highly energetic charged particle, such as a heavy ion in space, will likely interact with multiple pixels, depositing energy in a cluster of pixels. In a mixed radiation field, the radiation species of the detected particle can be classified through the morphology and energy deposited in the pixel cluster (Kroupa et al., 2015; Gohl et al., 2016). As clusters from multiple particles can sometimes overlap pixels, recording the ToA to complement the ToT energy measurement would permit the correct association of data with different detected particle interactions.

2.1. Adaptive-gain analogue frontend

The analogue frontend consists of a Krummenacher-type (Krummenacher, 1991) charge sensitive preamplifier (CSA) with adaptive gain, followed by a threshold voltage discriminator. The CSA compensates for leakage current from the sensor and can be programmed to process either positive or negative polarity signals from the sensor material. Each pixel also has a 5-bit digital to analogue converter that trims the local threshold of the discriminator. A programmable control charge can be injected to the input of the preamplifier during test and calibration of the analogue frontend.

Whereas the gain of the CSA, which is inversely proportional to the feedback capacitance, was a fixed value in previous Medipix and Timepix ASICs, the Timepix2 frontend includes an adaptive gain scheme based on a design which was originally developed for free electron laser instrumentation (Manghisoni et al., 2015). Fig. 1 shows the parallel paths for the feedback capacitance in the CSA: one path consisting of a fixed capacitance between metal plates and a second path consisting of a metal-oxide-semiconductor (MOS) capacitance. When the MOS capacitor path is disabled, the CSA feedback capacitance, C_{FB} , is based on the

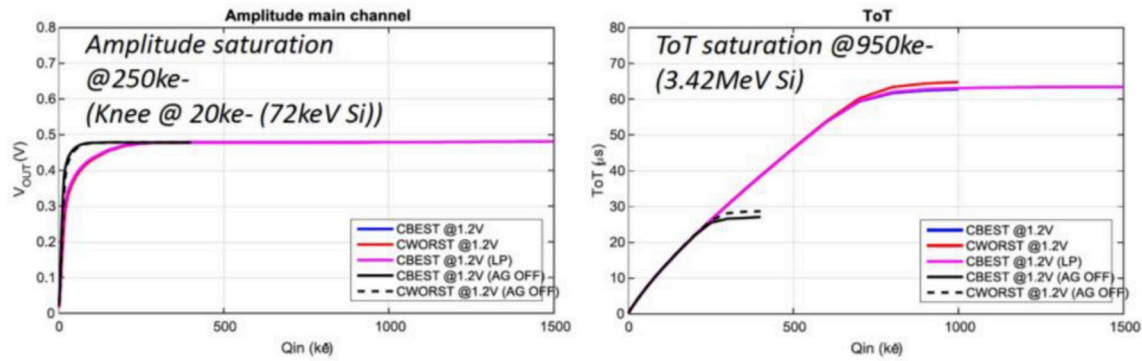


Fig. 2. Simulations of the frontend behaviour in hole collection mode.

Table 1

Parameters of the analogue frontend (values based on simulation).

Parameter	Fixed Gain Mode	Adaptive Gain Mode (hole collection only)
Minimum threshold	400 e ⁻	380 e ⁻
Noise	60 e ⁻ rms	50 e ⁻ rms
Gain	25 mV/ke ⁻	19 mV/ke ⁻ (for low input charges)
Power consumption	5 μ A/frontend @1.2 V	

metal plate capacitance and the CSA gain is constant for all input charge values. When the MOS capacitor is enabled, C_{FB} is the combination of the metal plate and the MOS capacitance, which is biased by the CSA input. In adaptive gain mode, the gain is high with low input charges and low with high input charges. Even when the input charge versus pulse height relationship becomes logarithmic, simulations show that the ToT of the discriminator output pulse increases monotonically with input charge up to 950 ke⁻; the ToT is expected to plateau at a maximum value beyond this point. Fig. 2 shows simulations of the frontend behaviour with and without adaptive gain (AG). Best case (CBEST) and worst case (CWORST) refer to minimum and maximum extracted C_{FB} values, and LP denotes the use of low power (i.e. high threshold voltage) transistors. The ToT values on these plots are derived from transient simulations of the CSA output prior to threshold discrimination; the “threshold” used here is an ideal threshold voltage. Due to the preamplifier topology, the adaptive gain mode is only compatible with sensors that provide positive polarity signals. Table 1 lists the design parameters of the Timepix2 analogue frontend based on simulation.

2.2. Digital modes

The digital part of the pixel processes the threshold-discriminated output from the analogue frontend. Each pixel contains a total of 28 bits that can be chained together to form 4-bit, 10-bit, 14-bit, or 18-bit counters that record ToT, ToA or number of particle hits. Table 2 lists the various operation modes. In the simultaneous ToT and ToA modes (Modes 1–2), the counter chains count concurrently and the pixels pause measurement during readout (i.e. the reading and writing operations are sequential). In the continuous read/write modes (Modes 3–8), the two counter chains are identical in depth and alternate between counting and reading modes, such that there is no readout deadtime. Existing data in the counters can be quickly discarded with a fast clear command without the need to read out the counters. A programmable digital test pulse can be sent to selected pixels for digital test and calibration independent of the analogue frontend. In addition to the eight operation modes of Table 2, Table 3 lists the modes for programming and digital diagnostics of pixel memory.

A set of digital pixels in the chip periphery also operate in the modes

of Table 2. The digital pixels do not have an analogue frontend and are not connected to the sensor; they are intended to process threshold-discriminated inputs from external instruments.

2.3. Event selection

In the operation modes that measure ToT (Modes 1–4 of Table 2), the selection of events that contribute to the measurement is handled differently by Timepix2 compared to its predecessor. In the original Timepix, ToT is processed for all portions of discriminator output pulses that occur within the open shutter period. Timepix2, on the other hand, has the option to process just the first hit, or to integrate the ToT of all hits that start within the open shutter period. In order to correctly measure the charge deposited in high linear energy transfer (LET) events, if a valid discriminator output pulse is still active by the time the shutter closes, the ToT count continues until the end of the event, or until the counter saturates. Fig. 3 depicts the selection of events for processing in the main operation modes. Separate clocks are used for ToT and ToA counting. In the simultaneous ToT and ToA modes (Modes 1–2), the open shutter period is defined as the period during which the shutter is low. In the continuous read/write modes (Modes 3–8), the shutter signal becomes a counter select.

2.4. Pixel power optimisation

Although all pixels are functionally identical, they were grouped in “superpixels” of 2×16 pixels during synthesis, place and route, in order to optimise the sharing of resources. Clock trees are generated and gated at the superpixel level to reduce digital power consumption if no hits are detected within the local superpixel. This type of power optimisation targets particle detection applications with sparse data in the pixel matrix. Operating in the simultaneous ToT and ToA mode, with both ToT and ToA clocks running at the maximum 100 MHz frequency, and assuming sparse hits, the pixel matrix is estimated to consume <500 mW digitally. Combined with the current consumption of the analogue frontend, the estimated total power consumption in the full pixel matrix is < 900 mW, based on simulation reports.

2.5. Power masking

While all Medipix and Timepix ASICs include the capability to mask the digital functionality of individual pixels, the pixel circuits in the Timepix2 chip are also powered down when masked. On the digital side, the measurement reference clock is gated with the pixel mask bit to turn off dynamic power consumption. On the analogue side, the discriminator is powered down completely, while the preamplifier is supplied with a minimal current (a few nA versus the nominal several μ A) to maintain sensor leakage current compensation. This scheme permits partial activation of regions of interest in the matrix without

Table 2
Digital operation modes.

Mode	Description	Counter1	Counter2	Counter3	Counter4
Mode1	Simultaneous ToT & 1st hit ToA^a (sequential read/write) User-defined options:	10-bit ToT	18-bit ToA	n/a	n/a
Mode2		14-bit ToT	14-bit ToA	n/a	n/a
Mode3	1) 1st hit or integral ToT 2) ToT clock frequency 3) ToA clock frequency 4) Wraparound of ToA counter Continuous read/write ToT with optional event counting User-defined options:	10-bit ToT	10-bit ToT	4-bit #events (paired with Counter1)	4-bit #events (paired with Counter2)
Mode4	1) 1st hit or integral ToT 2) ToT clock frequency Continuous read/write ToT User-defined options:	14-bit ToT	14-bit ToT	n/a	n/a
Mode5	1) 1st hit or integral ToT 2) ToT clock frequency Continuous read/write ToA User-defined option:	10-bit ToA	10-bit ToA	n/a	n/a
Mode6		14-bit ToA	14-bit ToA	n/a	n/a
Mode7	ToA clock frequency Continuous read/write	10-bit #events	10-bit #events	n/a	n/a
Mode8	event counting User-defined option:	14-bit #events	14-bit #events	n/a	n/a
	Reference clock frequency				

^a Since the ToA counter of a pixel can only store the timestamp of one event, it records the arrival time of the first event to occur within the open shutter period, regardless of whether the ToT option is programmed to evaluate 1st hit ToT or integral ToT.

unnecessarily consuming power in the unused regions. The time to power down or re-activate pixels in the matrix is the time it takes to reprogram the configuration bits: 2.6 ms.

3. Framerates

Data from the pixel matrix can be read out from a serial port or a 32-bit parallel bus. Both serial and parallel ports operate at up to 100 MHz. In regular full frame readout mode, data from all 65k pixels are output from the chip, including data from empty pixels. An optional zero-column-suppression (ZCS) readout mode minimises the readout of empty columns during output from the serial port. In ZCS mode, a 256-bit column hit map register is first output, followed by data from the columns enabled in the hit map. The architecture of the ZCS mode requires that a minimum of 16 columns be output (even if they are empty). Table 4 lists the time to read a frame from the Timepix2 chip, using the maximum data clock frequency of 100 MHz. In the simultaneous ToT and ToA operation mode, the minimum readout deadtime corresponds to t_{read} of 28 bits. In the continuous read/write modes, there is no readout deadtime, but the minimum counting period is defined by t_{read} .

4. Measurements

In this work, we report some preliminary measurements to demonstrate the most quickly testable features of the Timepix2 ASIC.

Table 3
Digital programming and diagnostics modes.

Mode	Description
Mode9	Set individual pixel configuration settings
Mode10	Get individual pixel configuration settings
Mode11	Set individual pixel threshold trim codes
Mode12	Get individual pixel threshold trim codes

4.1. Data acquisition system

The measurements presented here were obtained with a Timepix2 hybrid pixel detector (Fig. 4a), mounted on a custom Timepix2 chip-board (Fig. 4b), connected to an AdvaDAQ data acquisition system and controlled by PiXet software (Turecek et al., 2016). The chipboard can be cut to permit the tiling of Timepix2 detectors mounted on separate cards.³ It contains industry standard connectors, voltage regulators, a power measurement chip, multiple test points, and a backside pulse processing (BPP) circuit to correlate events in the pixel matrix with events detected through the backside pulse in the sensor. The BPP circuit comprises a charge sensitive preamplifier followed by a bandpass filter. With the addition of a threshold discriminator to digitise the signal, the BPP output can be fed back to a digital pixel on the Timepix2 ASIC for ToT and ToA measurement. Since the BPP uses discrete components, the dynamic range can be customised for a particular application. For example, the choice of a CSA feedback capacitance of 1 pF would permit the charge integration of up to 100 MeV, while a 10 pF feedback capacitance would process up to 1 GeV in a silicon sensor.

4.2. Basic diagnostics tests

Digital diagnostics tests of the Timepix2 ASIC pass. We can write data into, and read back from, global chip programming registers in the chip periphery. We can also write and read back random patterns into all storage elements in the pixel matrix, including individual pixel configuration and trim latches, and the data counters. ToT, ToA and event counting using both analogue and digital test pulses function correctly.

³ Multiple Timepix2 detectors can be tiled to create a larger combined active area. The detectors can be abutted along three edges with $\sim 60 \mu\text{m}$ dead area between chips.

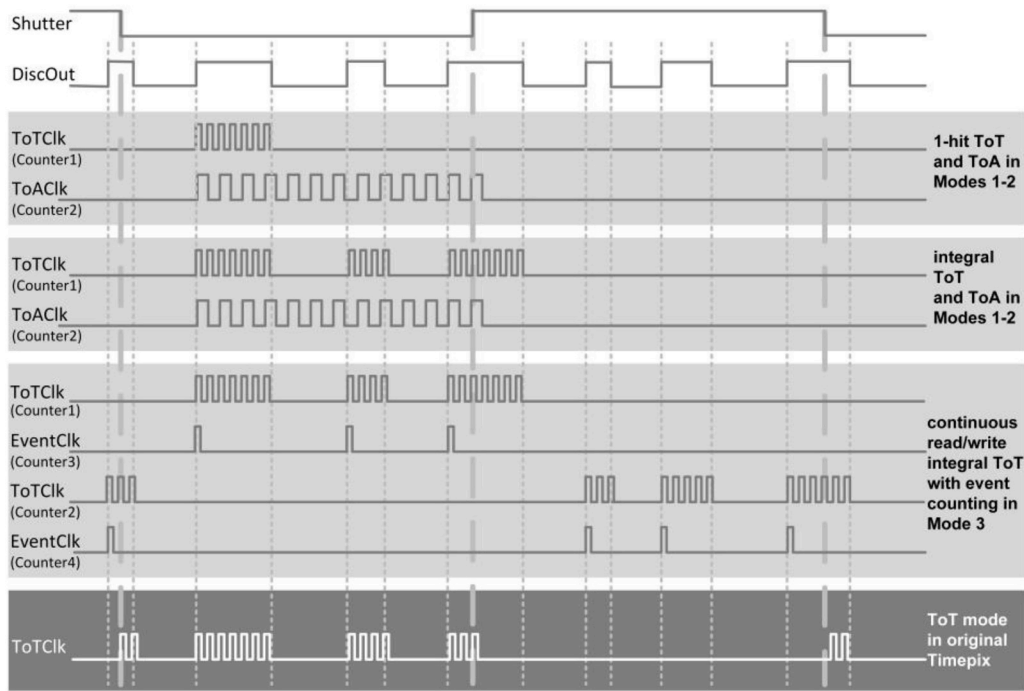


Fig. 3. Event selection with respect to the shutter state.

Table 4

Time to output frames in Timepix2, assuming 100 MHz clock.

# bits/pixel	Full frame, serial port		Full frame, parallel port		ZCS ^a , serial port	
	t _{read} [ms]	framerate [fps]	t _{read} [ms]	framerate [fps]	t _{read} [ms]	framerate [fps]
4	2.62	381	0.08	12207	0.16	6104
10	6.55	153	0.20	4883	0.41	2441
14	9.18	109	0.29	3488	0.57	1744
28	18.35	54	0.57	1744	1.15	872

^a The readout time and framerate in ZCS mode depends on the number of columns that contain data. The values shown in Table 4 are based on 16 columns, which is the minimum number of columns that must be read out in ZCS mode.

4.3. DAC scans

Fig. 5 shows input parameter sweeps of the digital to analogue converters (DAC) that are located in the chip periphery and provide programmable biasing of the analogue circuits. The DAC outputs agree with expected values.

4.4. Preamplifier response to test charge injection

For testing purposes, the output of the CSAs in the bottom row of the pixel matrix can be buffered and monitored by a test point on the chipboard. Fig. 6 shows screen captures of an oscilloscope monitoring the CSA output of a sample pixel stimulated by the injection of a test charge. The quantity of test charge is estimated based on the test capacitance value, C_{test}, which is extracted to be 5.8 fF by circuit simulation tools. In fixed gain mode (images on the left), the CSA output pulse height increases linearly with input charge quantity until the CSA output pulse height saturates. In adaptive gain mode (images on the right), the frontend gain is at a maximum for low quantities of input charge, and decreases as higher input charges turn on the MOS capacitor (Fig. 6c). The gains labelled on Fig. 6 are approximations based on the CSA output pulse height estimated from the oscilloscope screen shot. A precise gain calculation would require more detailed measurements. Nevertheless, the gains obtained from these preliminary tests indicate that the actual gain of the circuit agrees reasonably well with the value expected from simulation, listed in Table 1.

4.5. ToT measurement of analogue test charge

Fig. 7 shows ToT measurements of controlled test charges injected into the analogue frontend. Each data point represents the ToT counter

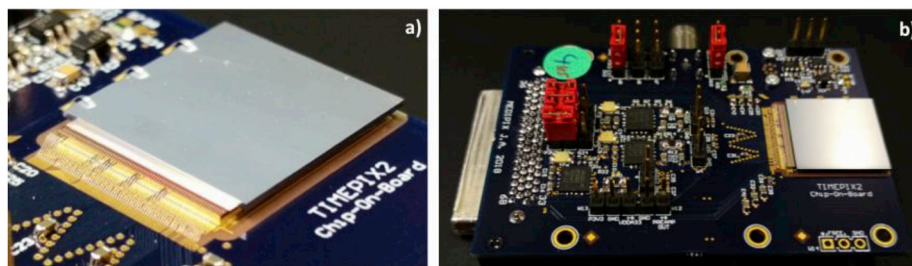


Fig. 4. Timepix2 with silicon sensor mounted on the chipboard. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

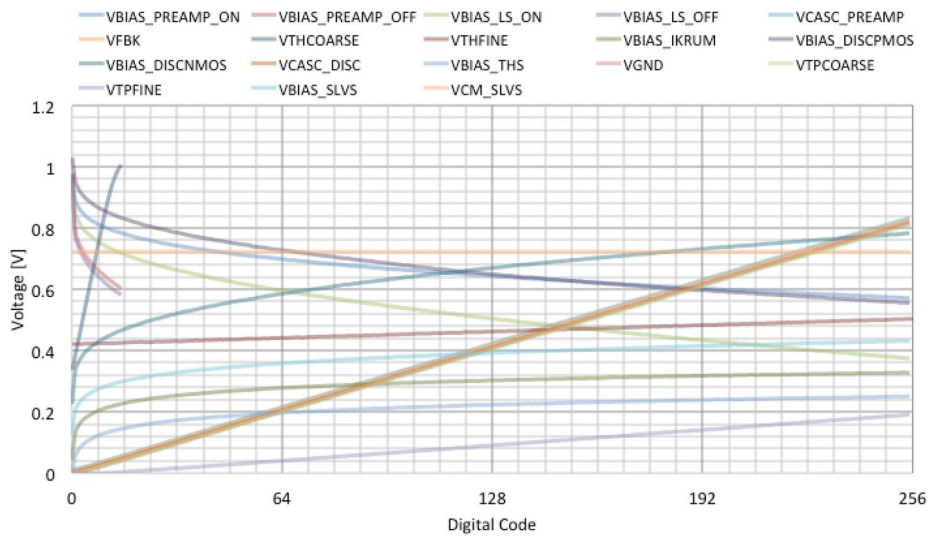


Fig. 5. DAC scans.

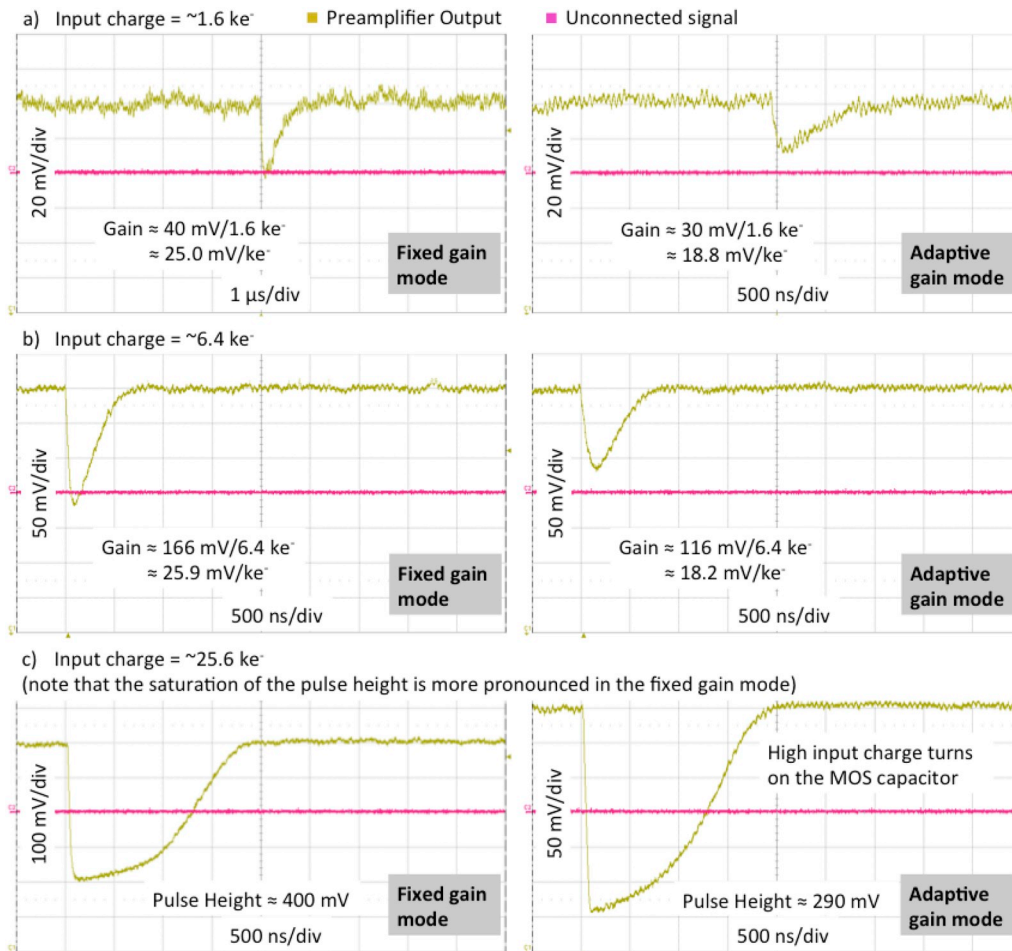


Fig. 6. Test charge injection to CSA, in fixed and adaptive gain modes.

value in a single pixel after ten consecutive analogue test pulses during the open shutter period. In Fig. 7a, a linear fit of the two curves in the region between 5 ke^- to 30 ke^- shows that the slope of the integral ToT (iToT) counts is 9.97 times the slope of the 1st hit ToT counts. Allowing for frontend noise and ToT quantisation error, this preliminary result suggests that the pixel correctly processes the ToT of only one out of ten

test pulses in 1st hit ToT mode, and measures the cumulative ToT of all ten test pulses in iToT mode. Fig. 7b shows the 1st hit ToT measurement with and without adaptive gain (AG) in the analogue frontend. Turning on AG does not seem to introduce any obvious non-linear effects to the ToT versus input charge relationship. The offset in the minimum detected input charge between these two uncalibrated measurements is

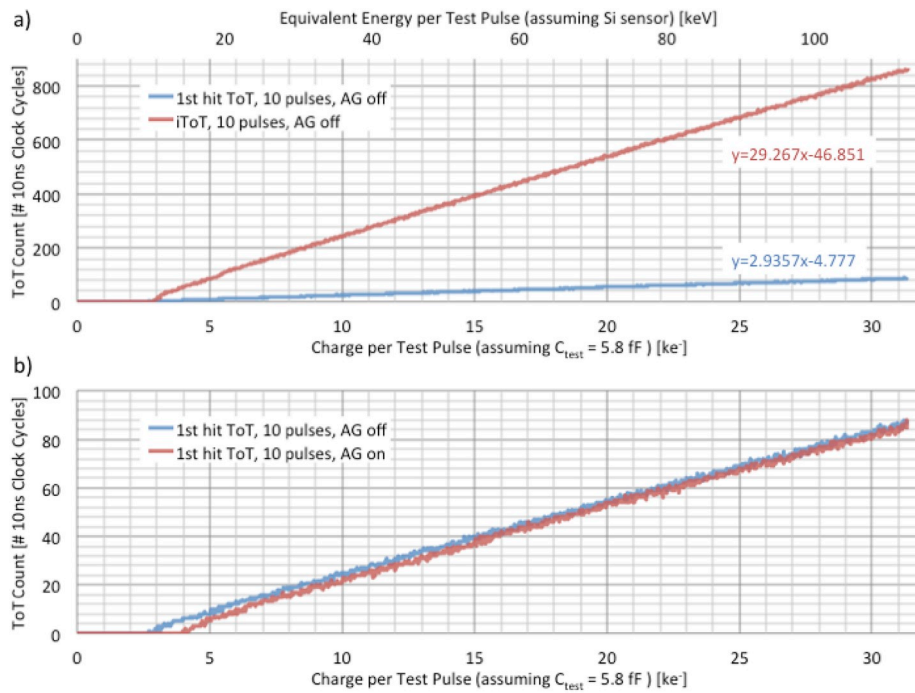


Fig. 7. Measurements of test charge injected at the input of the preamplifier.

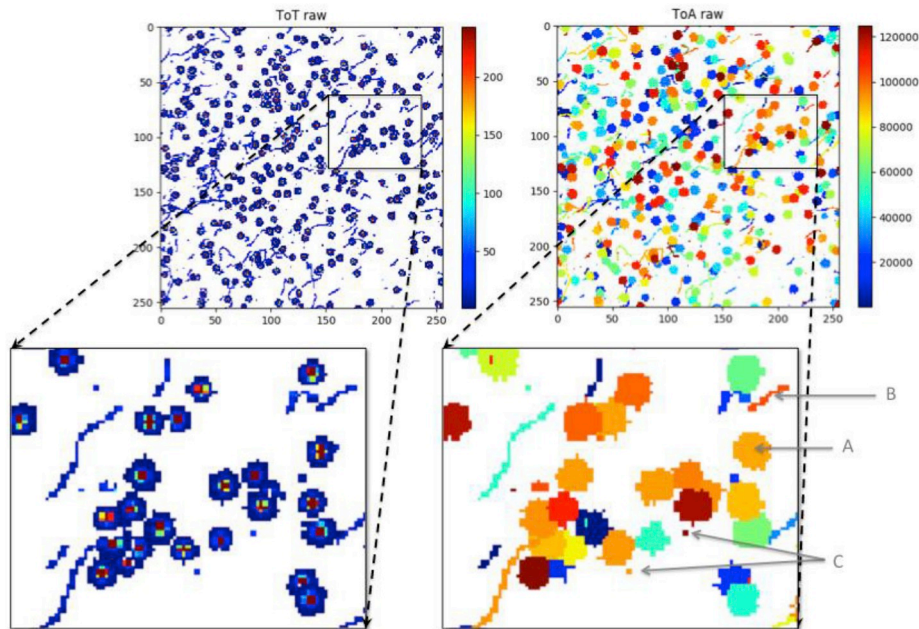


Fig. 8. Simultaneous ToT and ToA measurement in a mixed radiation field.

due to the difference in frontend gain in the two modes (see Table 1).

4.6. Simultaneous ToT and ToA measurements with radiation sources

Fig. 8 shows a frame output from a Timepix2 ASIC bump-bonded to a 500 μm p-on-n silicon sensor, displaying the energy and timestamp simultaneously measured within the same open shutter period. The chip was programmed to operate in the simultaneous ToT and ToA mode, with a 10-bit ToT counter and an 18-bit ToA counter per pixel. The Timepix hybrid pixel detector was exposed to a mixed field of beta electrons from a Sr90 source, alpha particles from an Am241 source, and gamma photons from the same Am241 source. Typically alphas deposit

energy in a cluster of pixels in a “blob” shape (e.g. Fig. 8, shape A), beta electrons interact with a cluster of pixels in a snake-like “squiggle” (e.g. Fig. 8, shape B), and gammas interact with single (or a very small cluster of two to four) pixels (e.g. Fig. 8, shapes C). The ToA timestamp helps to identify clusters resulting from the same radiation interaction, and to distinguish between spatially overlapping clusters.

It should be noted that the data in Fig. 8 were taken with an uncalibrated detector for demonstration purposes. A proper characterisation of the radiation field would require data from a calibrated detector. A calibration technique to map ToT counts to energy deposited in each pixel is described in detail in (Jakubek, 2011).

5. Conclusions and future work

In this work, we have presented the Timepix2 hybrid pixel detector readout ASIC. Timepix2 is a programmable detector intended for particle physics applications requiring a compact, high-resolution detector with high dynamic range. Several feature upgrades have been added compared to its predecessor, including a selectable adaptive gain front-end, event selection based on the shutter state, simultaneous ToT and ToA counting, separate ToT and ToA timing resolutions, continuous read/write modes, pixel power masking, and matrix occupancy monitoring. A custom chipboard has been designed and an AdvDAQ data acquisition system has been modified to read out the Timepix2 detector for initial tests. Preliminary results indicate that all tested chip functions perform correctly and agree well with expectations from simulations.

The results reported here were only preliminary tests obtained within the first few weeks since the reception of the ASIC from the foundry. A more comprehensive characterisation of the Timepix2 hybrid pixel detector with various sensor types will follow. The development of other data acquisition systems is also planned. The Timepix2 design realises the many features requested by the members and partners of the Medipix2 Collaboration, and we look forward to seeing the Timepix2 detector used in a variety of applications.

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