UNIVERSITY OF TEXAS ARLINGTON

Upgraded electronics of the ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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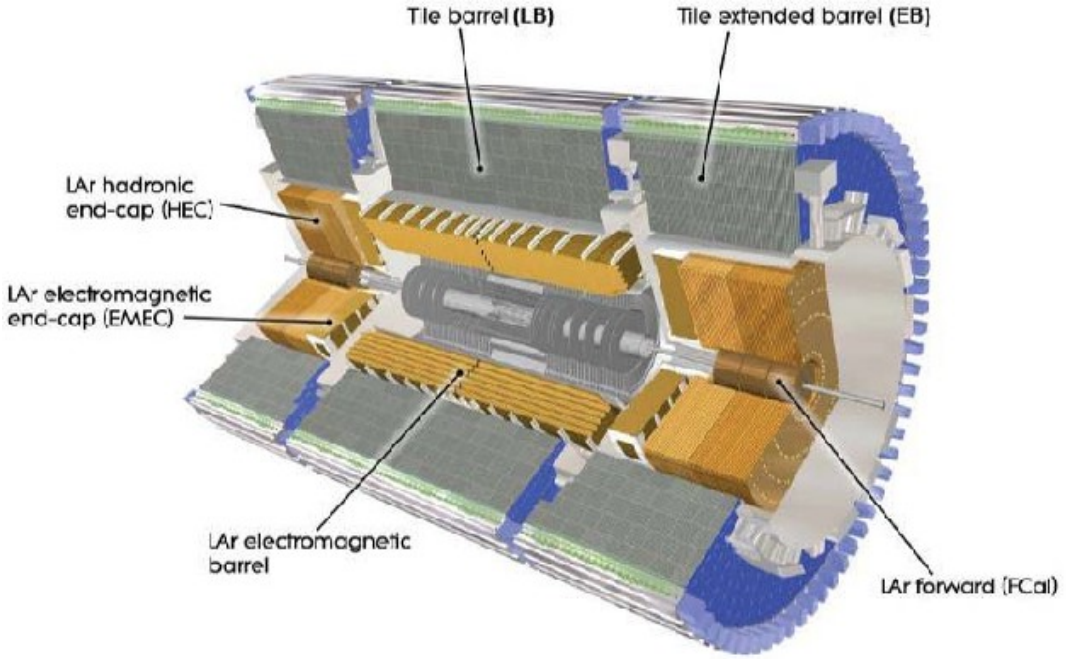
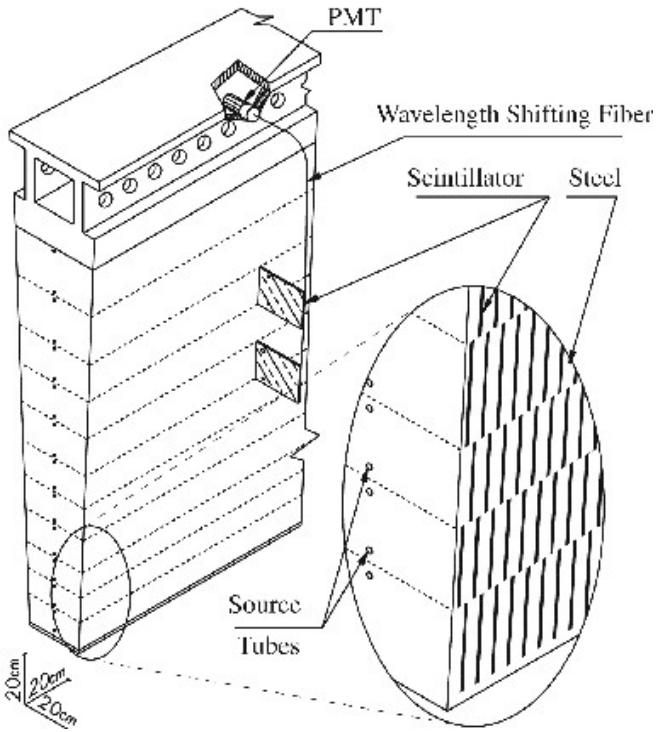
On behalf of the Tile Calorimeter Upgrade Team

November 28th 2019

Tile ATLAS Tile Calorimeter



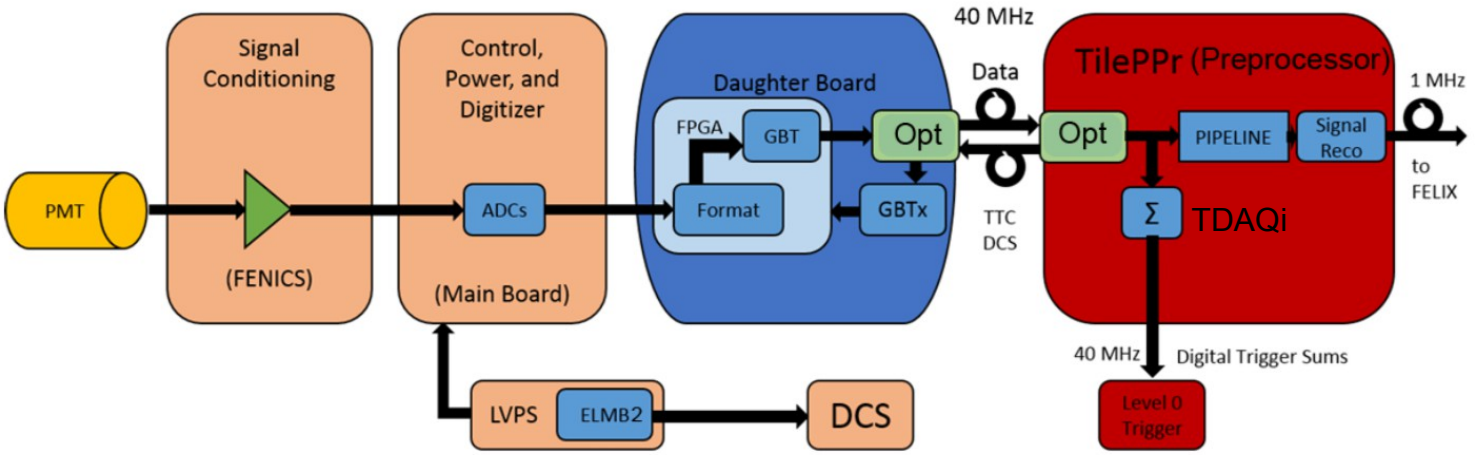


- Measures hadronic energy and missing ET.
- Segmented calorimeter of steel plates and plastic scintillators tiles
- 2 WLS fibers per tile
- 2 PMTs per cell
- Granularity 0.1 x 0.1 (eta,phi)

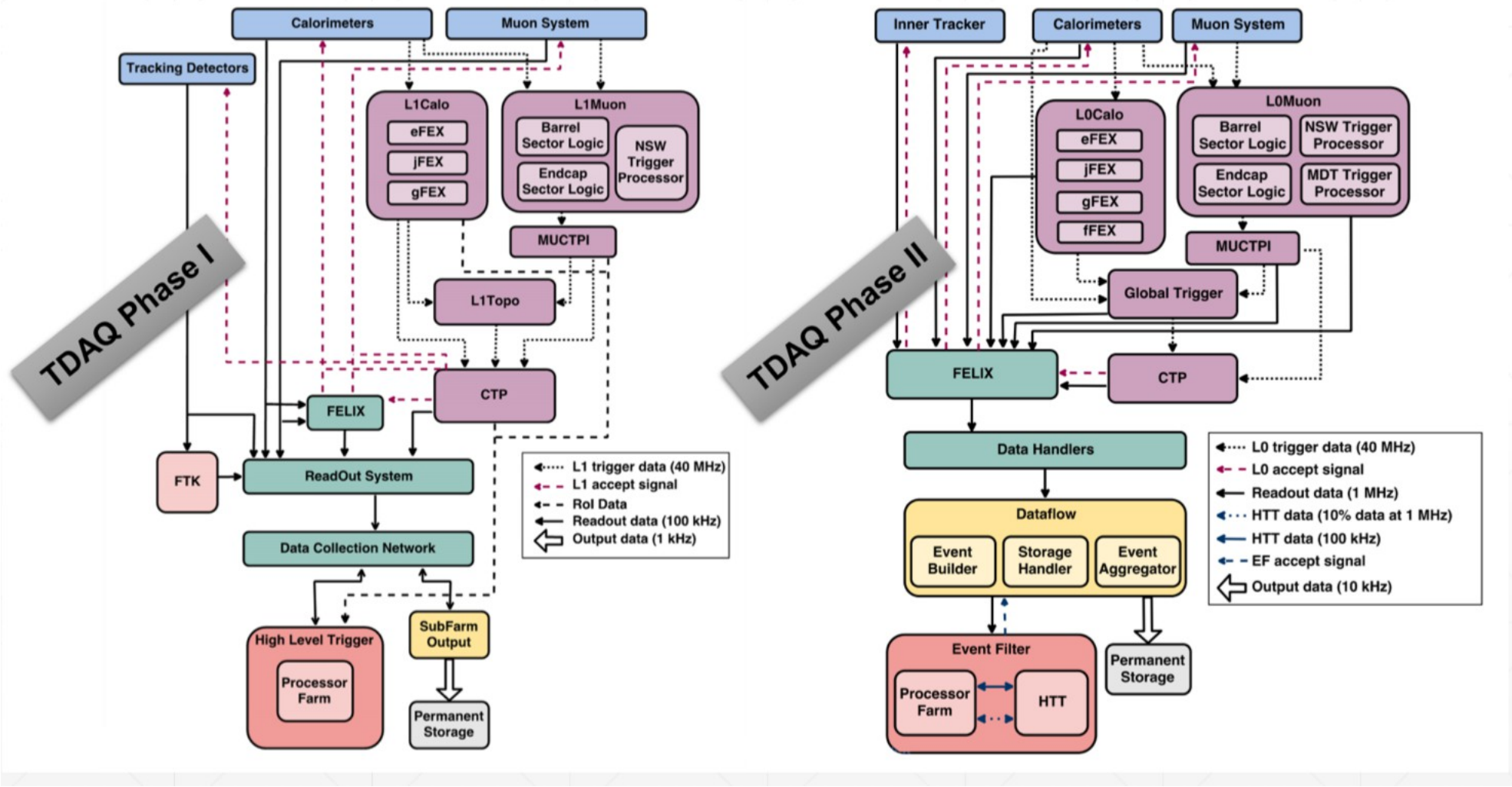
- Coverage: |eta| < 1.0 (LB)
  0.8 < |eta| < 1.7 (EB)
- Resolution $\frac{\sigma}{E} = 50\%/\sqrt{E} \oplus 3\%$
- 4 readout partitions
- Each partition has 64 modules
- About 10k readout channels

Tile Phase-II Upgrade for HL-LHC

- Complete replacement of on-detector and off-detector electronics.
  - To be compatible with full digital TDAQ and trigger processing at 40 MHz (L0) and to fulfill Phase-II radiation requirements.
  - And due to radiation and time aging (20x higher than legacy).
  - Moreover redundancy in data links and powering will be granted
- PMTs drawing the highest currents need to be replaced (10% of about 10k)
- Upgrade of LVPS system to reduce single point failure: one DC/DC converter powers 1/8 of a Tile module.
- High Voltage to be distributed remotely from off-detector.

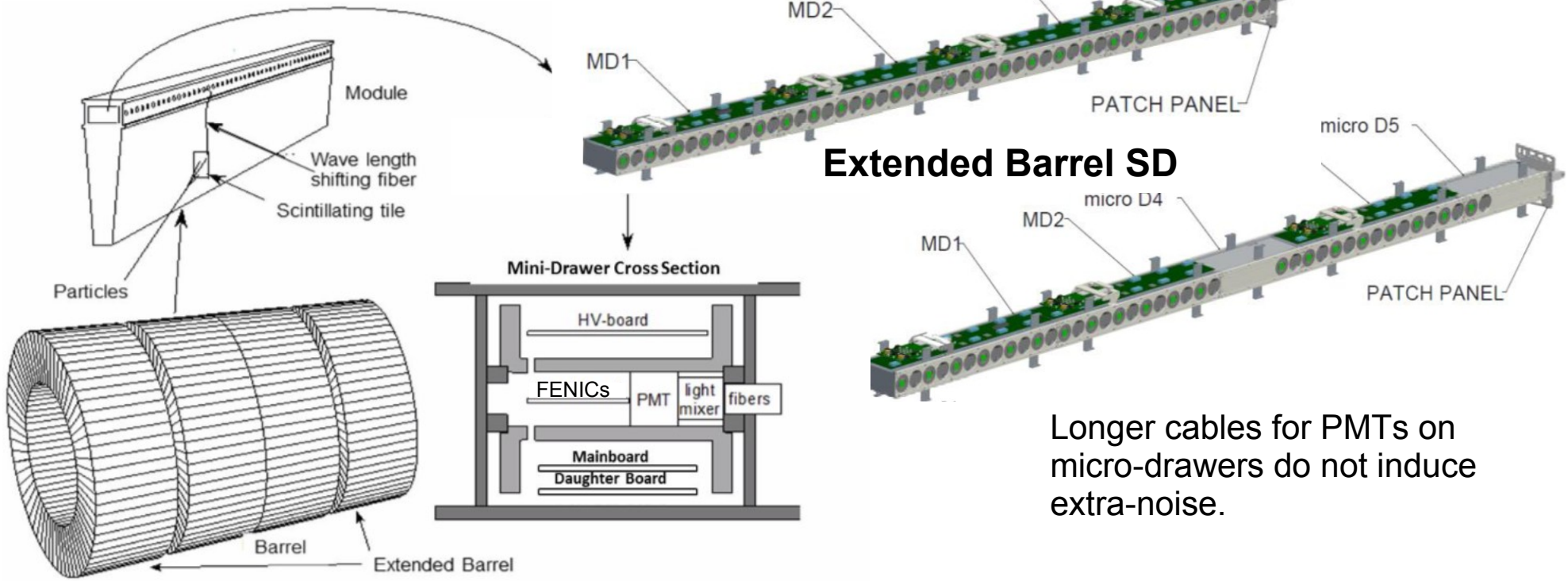


TDAQ architecture upgrade



Mechanics: “Mini-Drawers”

- 4 independent Mini-Drawers (hosting up to 12 PMTs each) for Long Barrel and 3 Mini-Drawers + 2 micro-drawers for Extended Barrel. Designed in Cluj and validated in Nov. 2018 testbeam.
- Easier maintenance and better robustness and modularity

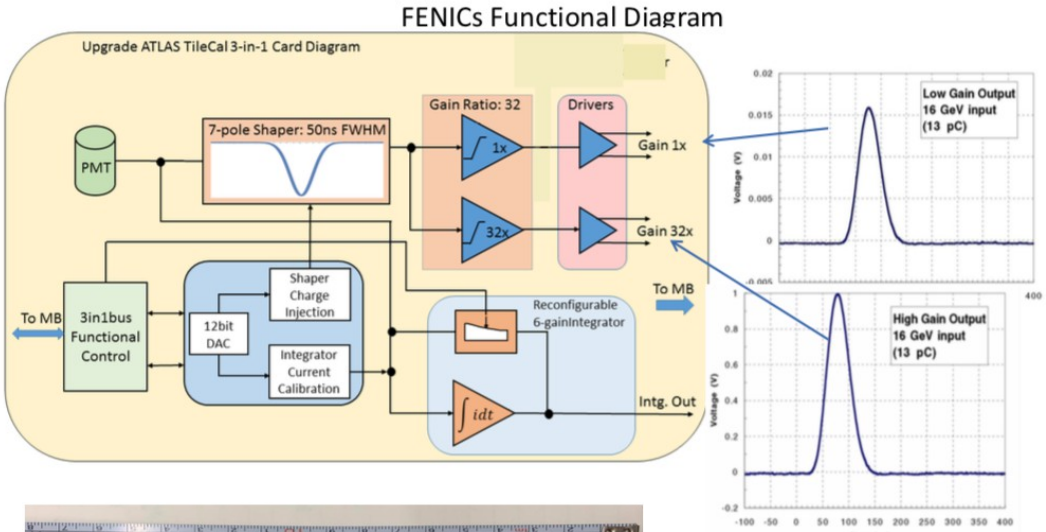


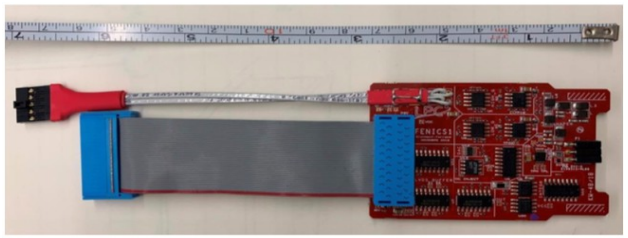
Longer cables for PMTs on micro-drawers do not induce extra-noise.

Front-End boards

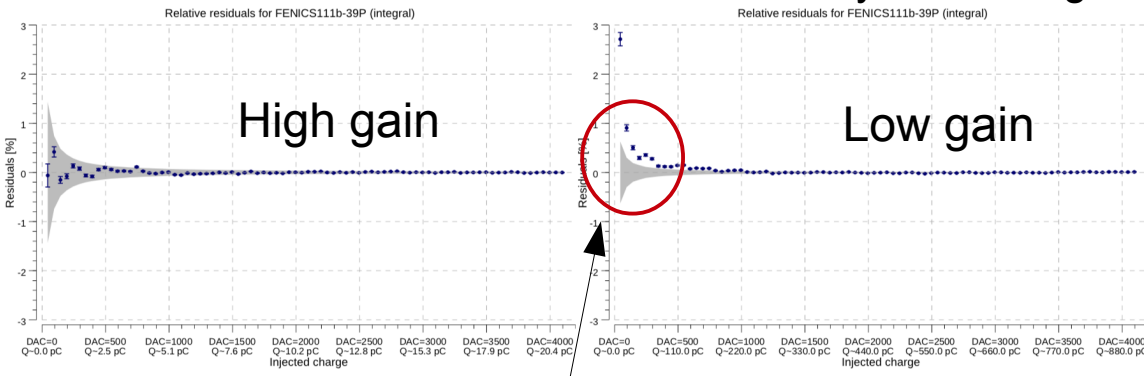
Evolution of the present FE 3in1 cards (U. Chicago)

- Radiation hard components
- PMT pulse shaping, 2 gains output and high precision slow integrator for Cesium calibration and luminosity measurement.
- Tuning the dynamic range by up to 20% to account for the higher PMT gain with new active dividers.



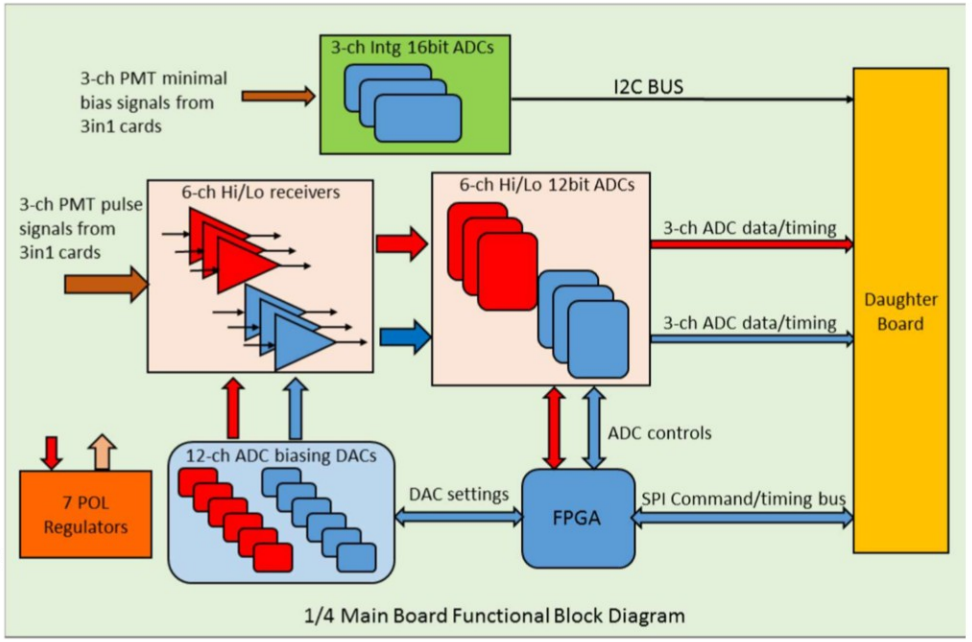


Latest FENICS version with increased dynamic range



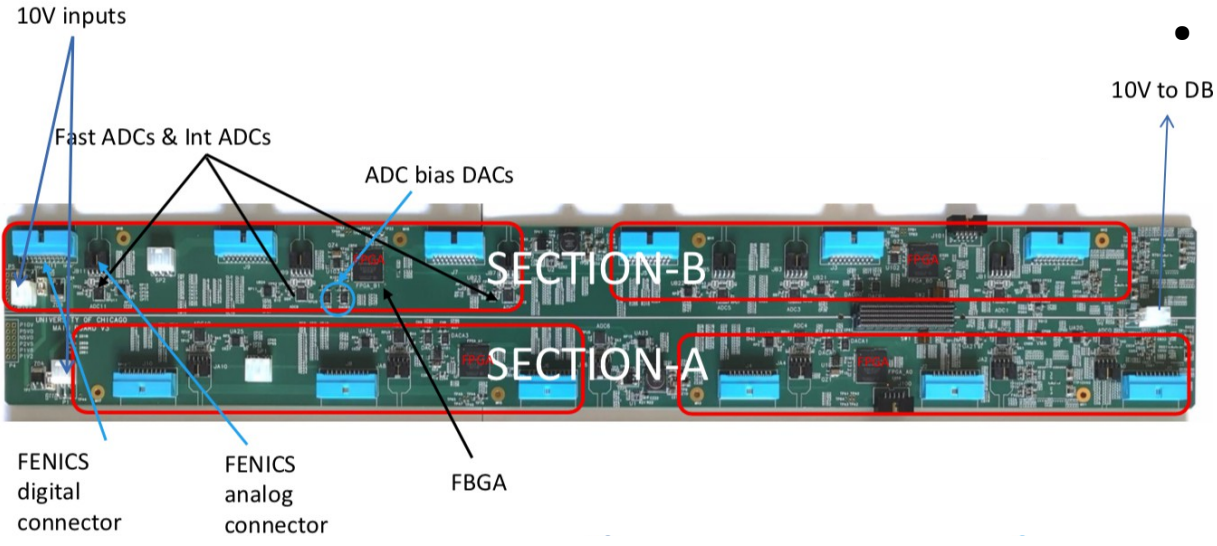
Up to 1% none linearity but covered by HG with much better linearity

MainBoard



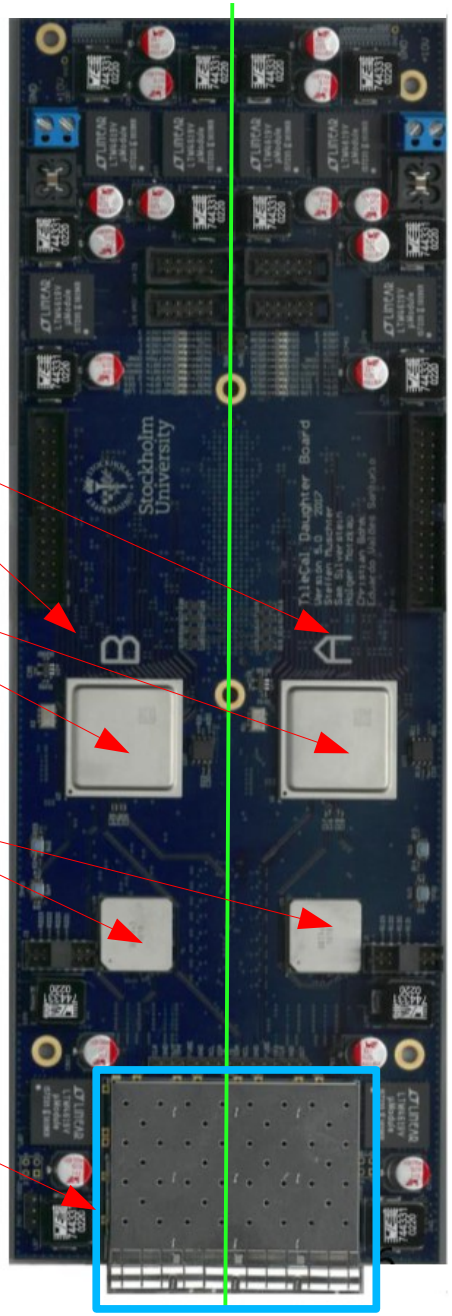
Control, power and digitizer interface between 12 FEBs and the DaughterBoard

- 4 sections with an FPGA in each.
- 3 PMTs controlled by 1 section: 6 chs of 40 Msps 12-bit ADCs (high and low gain), 3 chs 50kHz 16 bits ADCs for slow readout.
- The board is divided into 2 independent parts with powering from LVPS bricks.



DaughterBoard

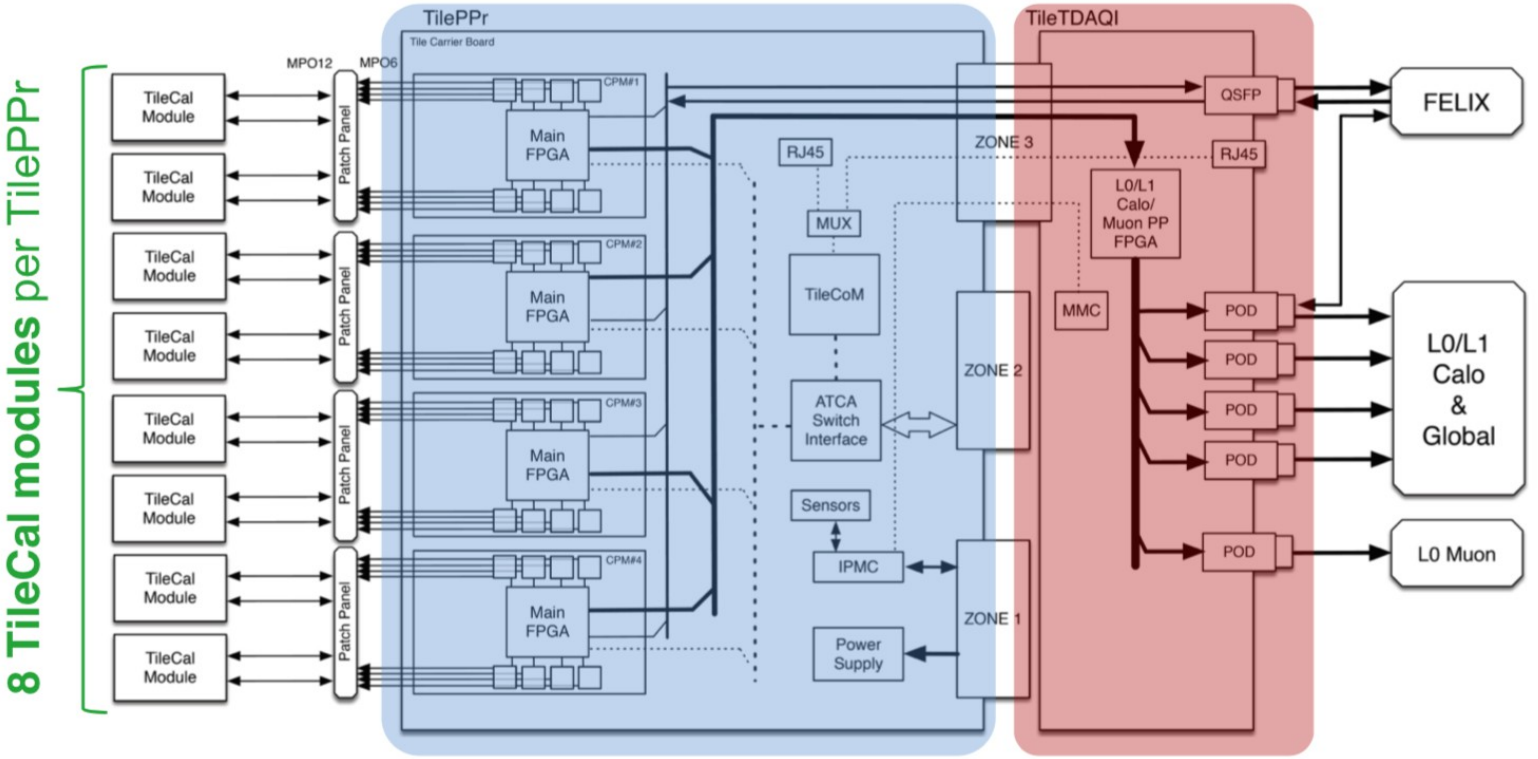
Stockholm University



- High-speed links with the off-detector electronics.
  - Data collection, formatting & transmission to the back-end
  - Clock & command distribution to the front-end
  - Double-redundancy
  - Communication with MB through 400 pin PMC connector.
- Latest DB version V5:
  - Kintex Ultrascale+ FPGA & 4 SFPs
  - During radiation tests SEL occurred with Kintex Ultrascale+
  - Replacing with plain Ultrascale and adding protection circuit in DBv6.

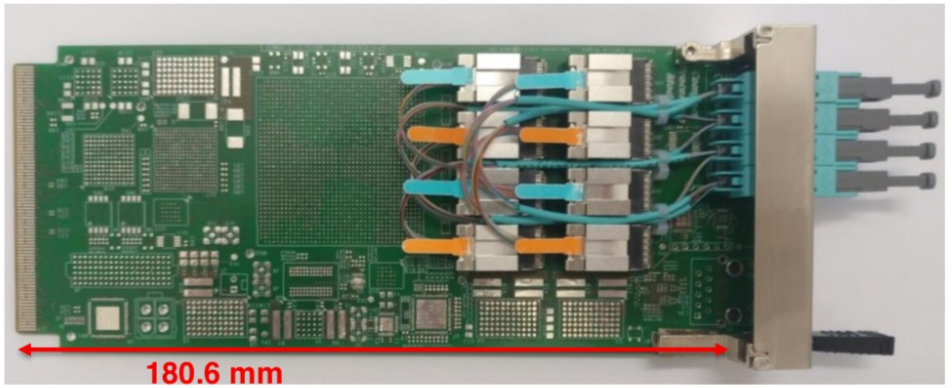
Overview of off-detector electronics

- Tile PreProcessor and TDAQi
  - Processing and handling of data from on-detector electronics
  - Distribution/ of LHC clock to TileCal modules
  - Interface with ATLAS trigger and ATLAS readout system



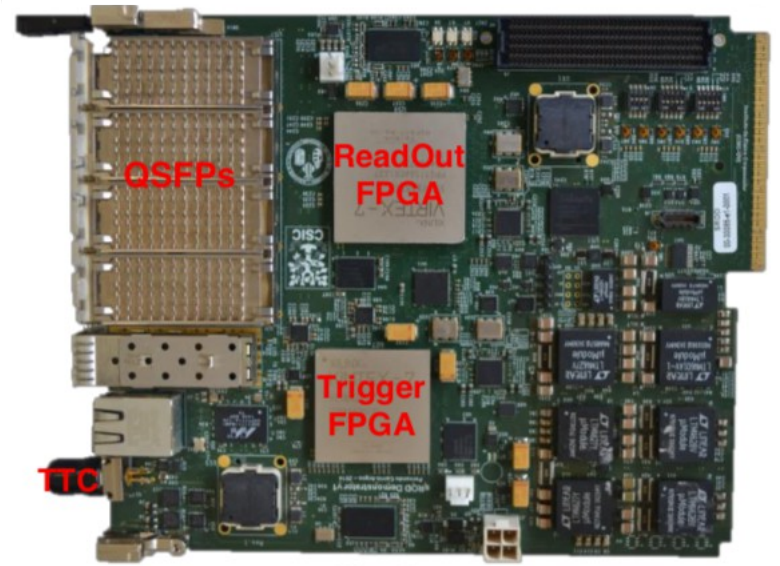
- 32 TilePPr boards in ATCA crate: carrier + 4 Compact Processing Module
- 32 TDAQi RTM: Interface with L0Calo, Global, L0Muon and FELIX

CPM and PPr Demo



Mechanical mockup of the Compact Processing Module

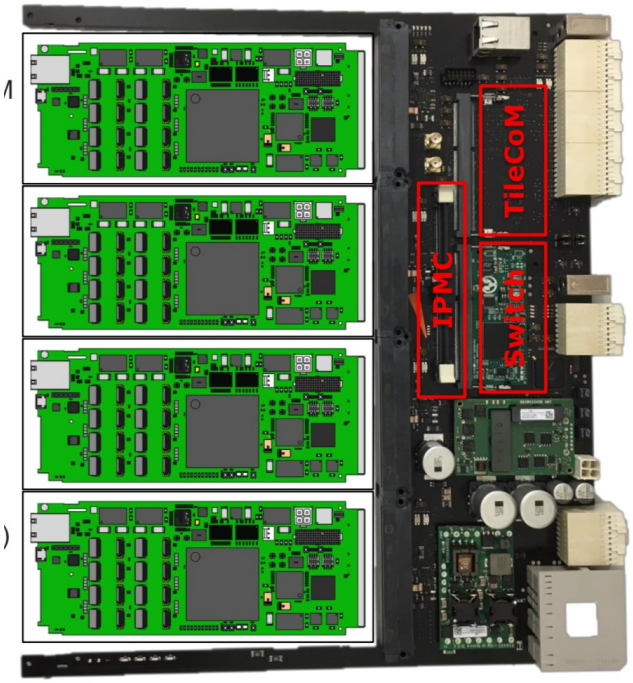
- Compact Processing Module
  - 14 layers PCB, 1.6 mm thick
  - Read-out of up to 8 mini-drawers
  - Energy reconstruction per PMT at the LHC frequency
  - First prototype available soon



PPr Demonstrator

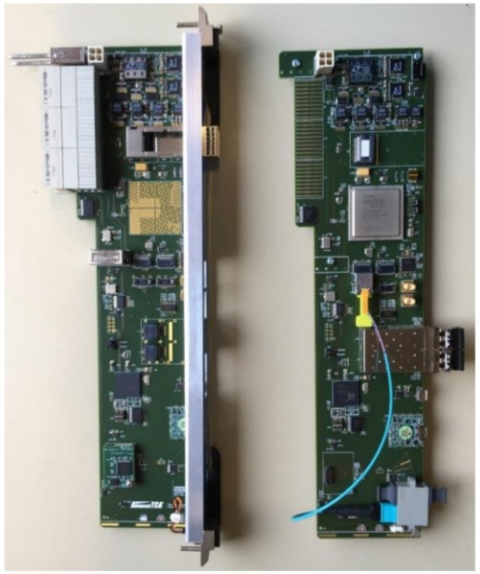
- Tile PPr Demonstrator
  - High speed interface with DB for data processing and handling
  - Clock distribution and configuration of the modules
  - Read-out of up to 4 mini-drawers
  - Used at test beam with backward compatibility, TTC and RODs

ATCA Carrier and TDAQi



Full size carrier board made and tested in Valencia (IFIC).

- Receives 4 CPMs and one TDAQi RTM (Rear Transition Module)
- Interface between the CPMs and the TDAQi.
- Interface with the FELIX (Front-End LInk eXchange)
- Transmits readout data of triggered events to FELIX through the TDAQi



TDAQi v1

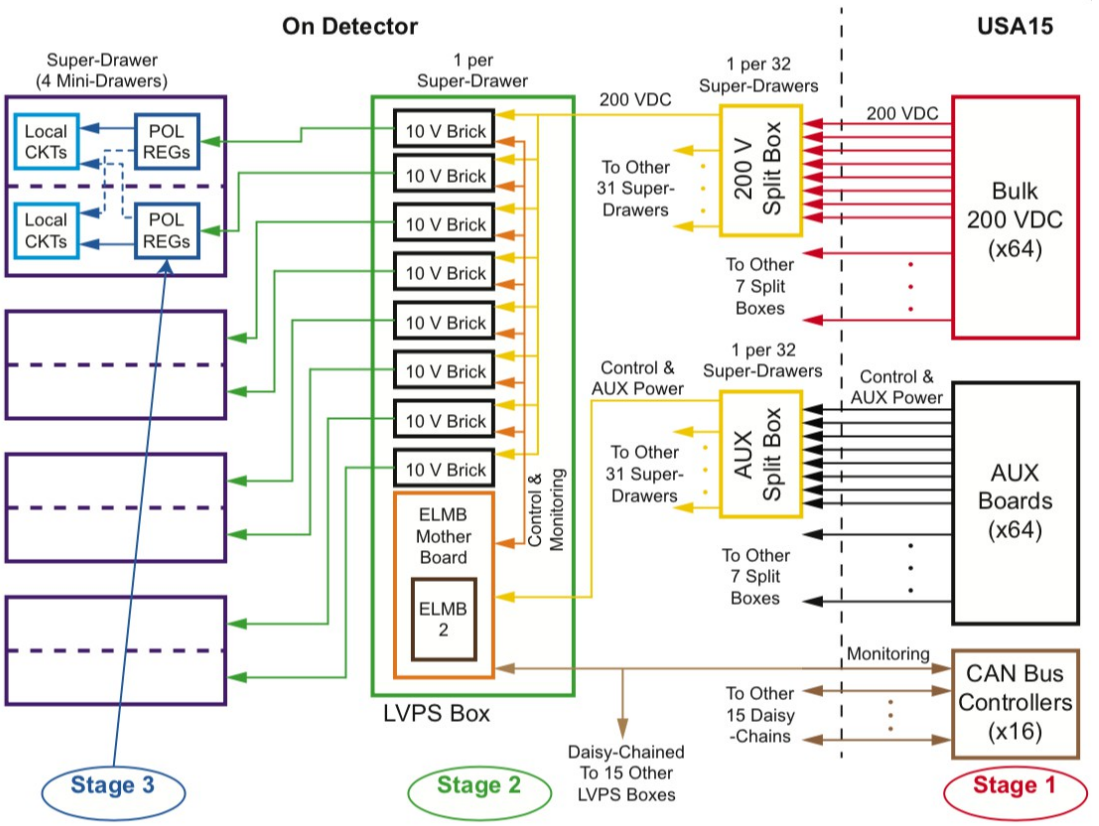
TDAQi v1 made and tested in Heidelberg

- Preprocesses trigger data (cell energy) and calculates trigger objects (towers or group of cells) → ATLAS Trigger system

LV system

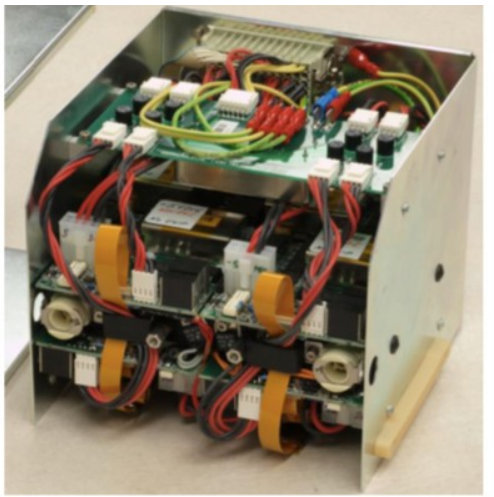
A three stage power system based on current LVPS

- Design with better reliability, lower noise and improved radiation tolerance
- One DC level brick with +10V
- Redundant power distribution: 2 individual bricks per Mini-Drawer. 8 bricks in a Tile Box.
- Control through ATLAS slow control system ELMB2.
- Long campaign of 6 irradiation tests and iteration to make the design radiation hard



Dose type	Max Dose (no safety factor)
TID	$80Gy$
NIEL	$3.5 \times 10^{12} n/cm^2$
SEE	$6.7 \times 10^{11} p/cm^2$

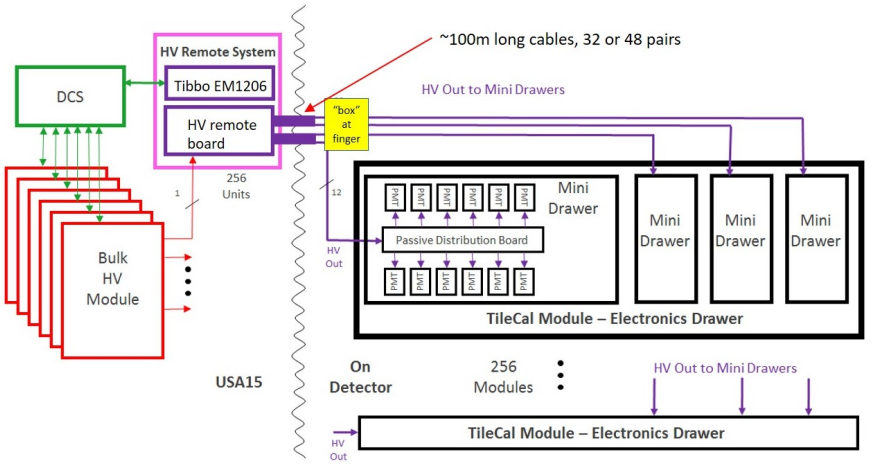
UTA, Prague



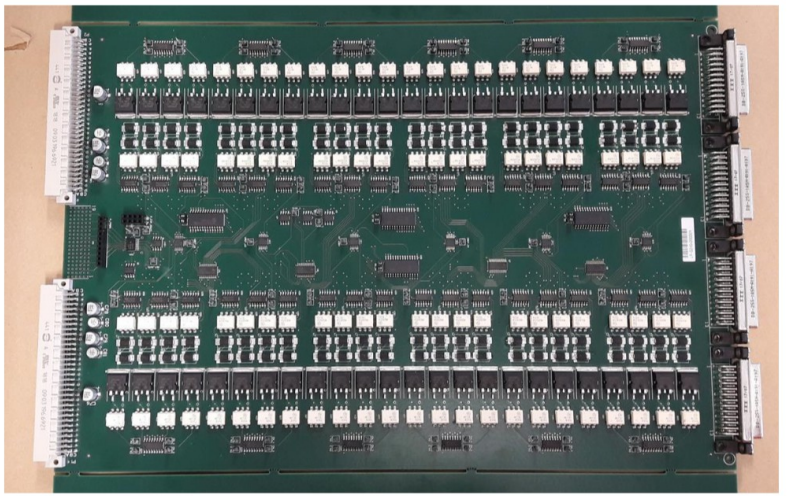
LVPS

High Voltage system

- Off detector HV distribution and regulation (HV remote) installed in ATLAS service cavern (USA15).
  - No radiation issues. Always accessible for maintenance.
  - Up to 48 pairs of wires per module in 100m long HV cable. 256 cables needed.
  - A 12 channels prototype used at test beam.
  - Full size 48 channels prototype under tests
  - Progress on the design of the HV bulk supply
  - Big challenge into routing and fitting all the wires in HV connectors.



HV remote system



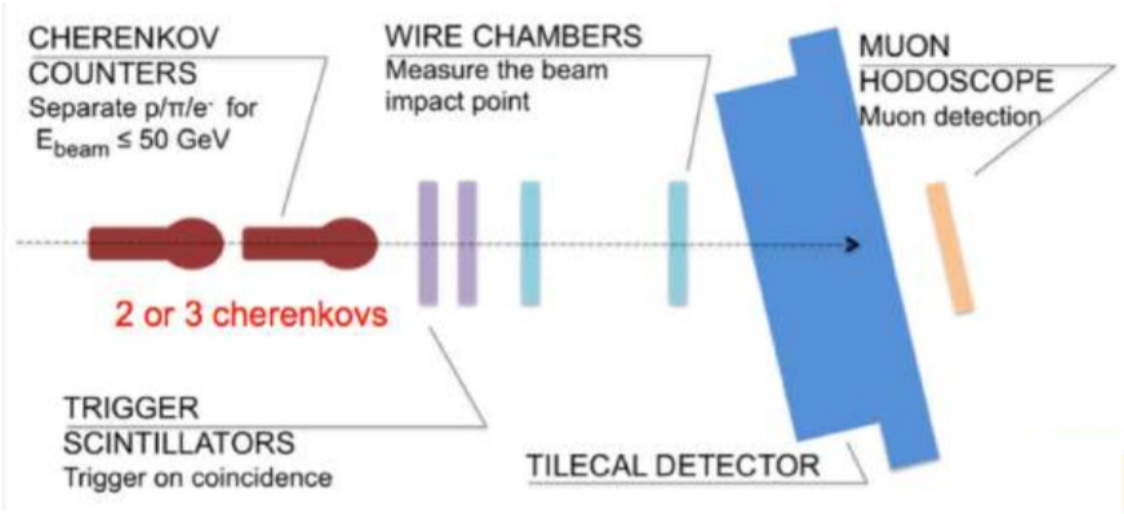
48 ch HV remote board

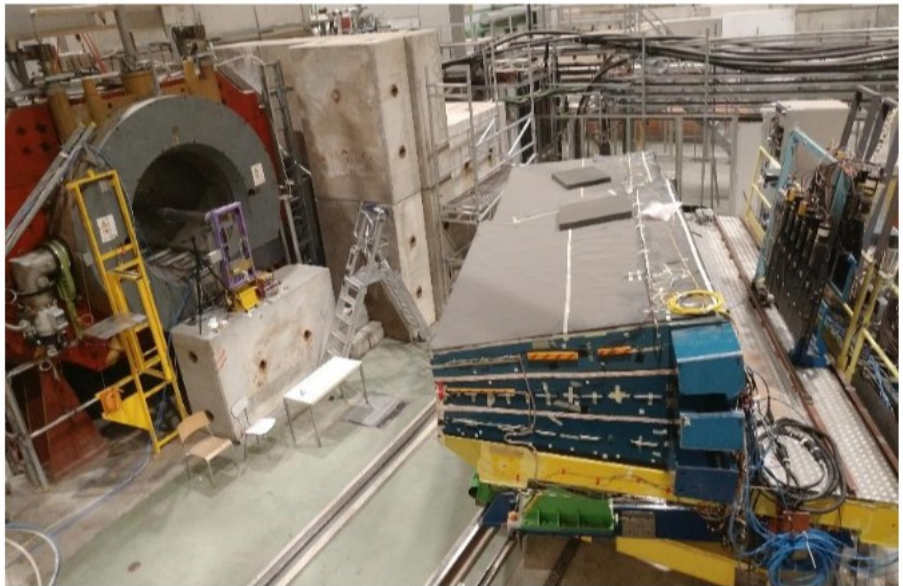
Test beam setup

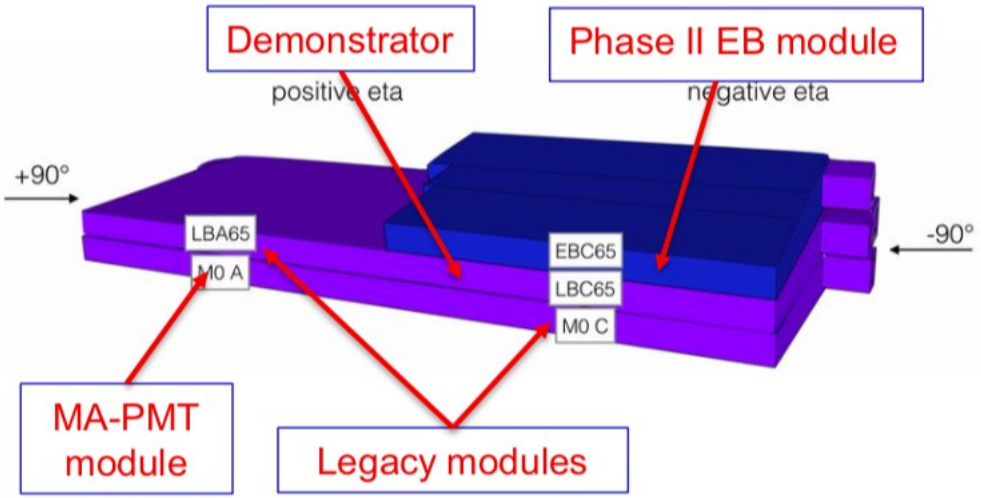
Three Tile modules stacked on a movable table:

- Ext. Barrel with FENICS card and Phase-II mini and micro drawers
- Tile Demonstrator in ½ of the Long Barrel module
- Drawer with Multi-Anode PMTs
- 2 legacy drawers

H8 beam facility at CERN SPS North Area



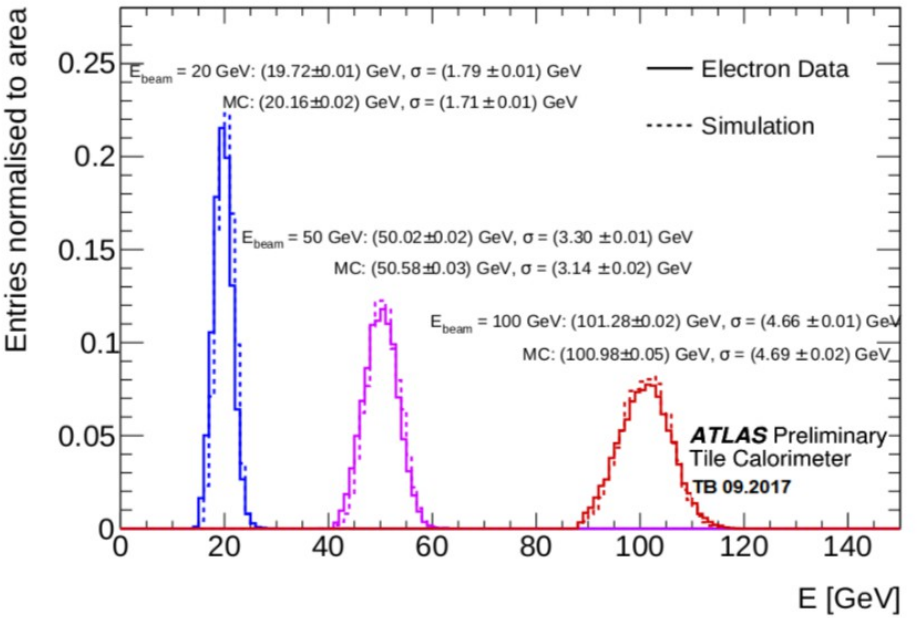


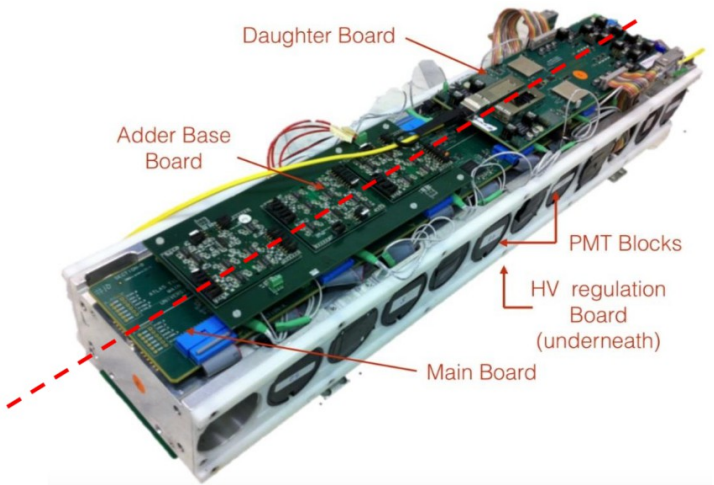


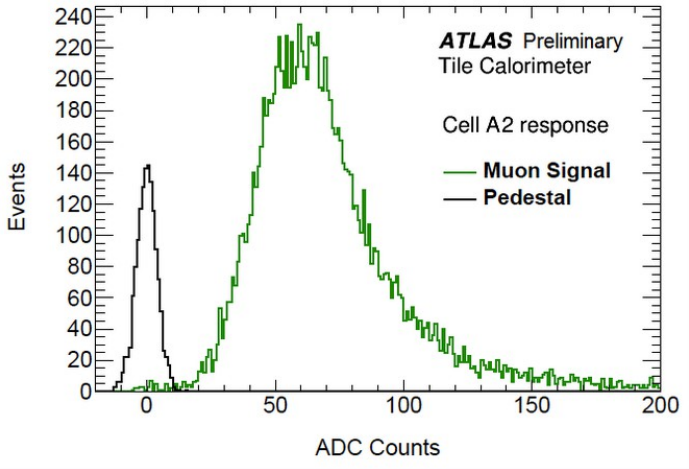
Tile Demonstrator in test beam

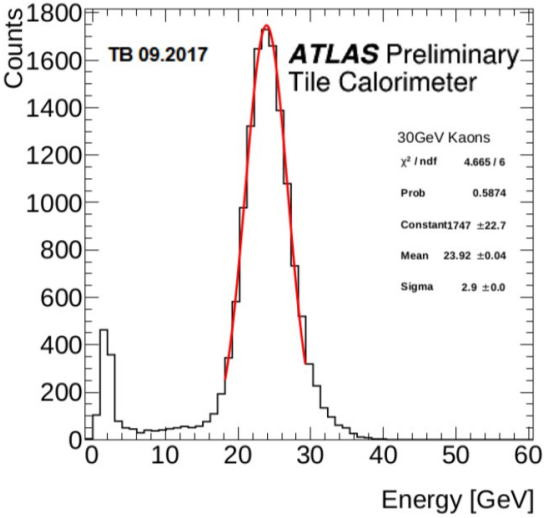
Integrated with the ATLAS TDAQ software and DCS for HV and LV

- FE configuration through PPr
- Physics and calibration data readout though FELIX and ROD
- Good performance and calibration through the different test beam campaigns









Tile Demonstrator @ ATLAS

The demonstrator project intends to operate a backwards compatible drawer in ATLAS during LS2 and possibly Run-3

- It was inserted in LBA14 in July.

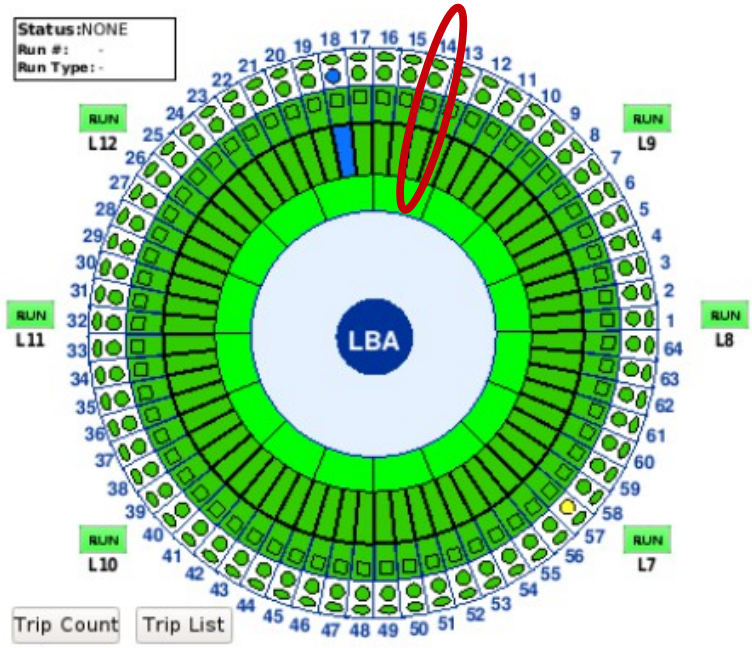
- Discovered some mechanical interference with mini-drawers which lead to small modifications.

- Powered (LV, HV) and monitored from DCS and calibrated using the TDAQ.

- Stable performance, low noise and good CIS and laser signals

- First tests with L1Calo → observed laser pulses in most trigger towers.

- Should meet some requirements in order to stay in ATLAS for Run-3



Inserting the demonstrator

Summary

- Wide R&D program to redesign the on-detector and off-detector electronics for HL-LHC

- Very good progress in all elements of the full readout chain.

- Most of the sensitive components have been radiation certified.

- Test beam campaigns from 2015 to 2018 proved the good performance of the prototypes of new electronics

- Full integration of the Tile demonstrator in the current system. Evaluation for Run-3.

- Good progress of the project which is in very mature state. Pre-production expected next year for several sub-systems.

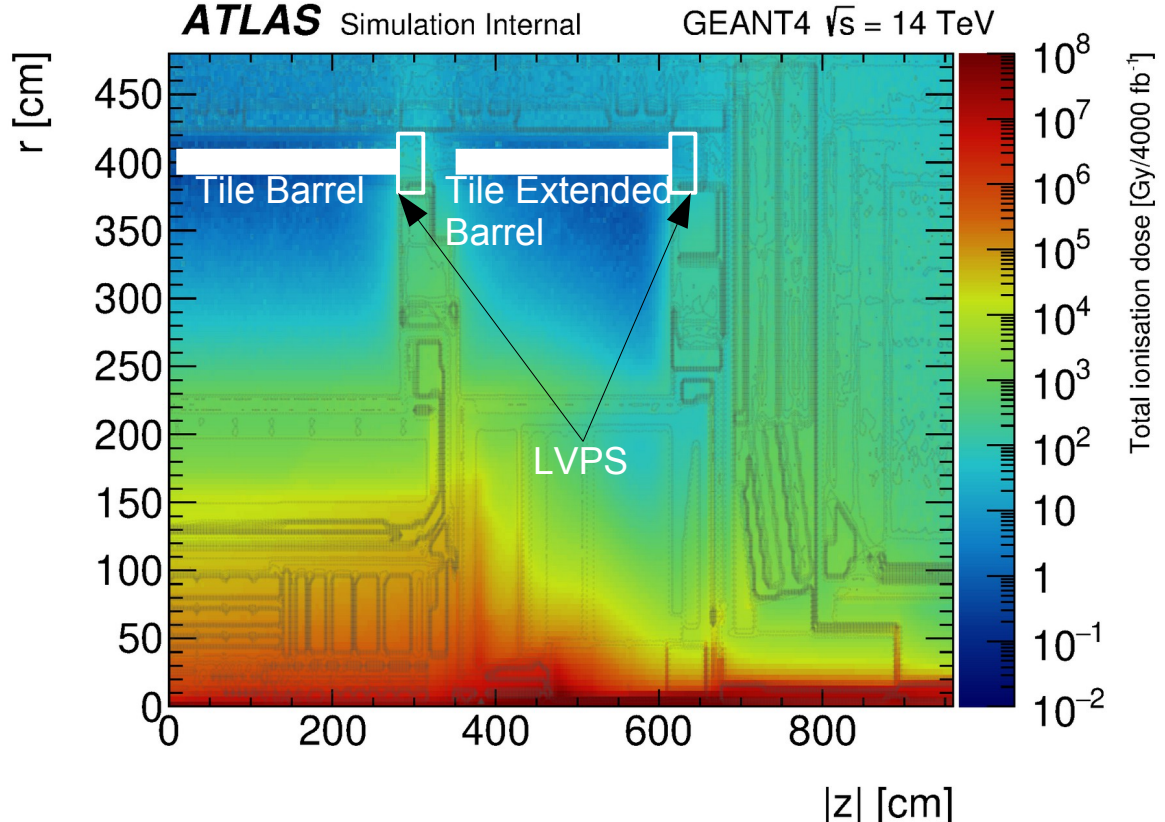
Backup

Tile Radiation Map

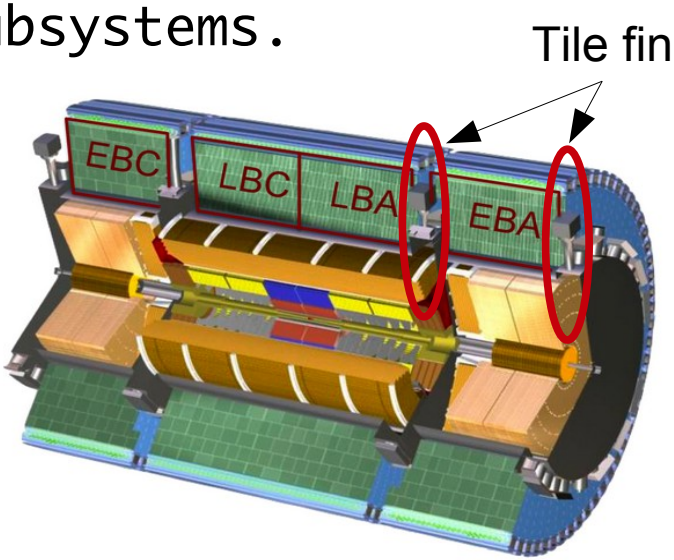
- Provided by the Radiation Estimation Task Force with Geant4

https://twiki.cern.ch/twiki/bin/view/Atlas/RadiationMapsGeant4

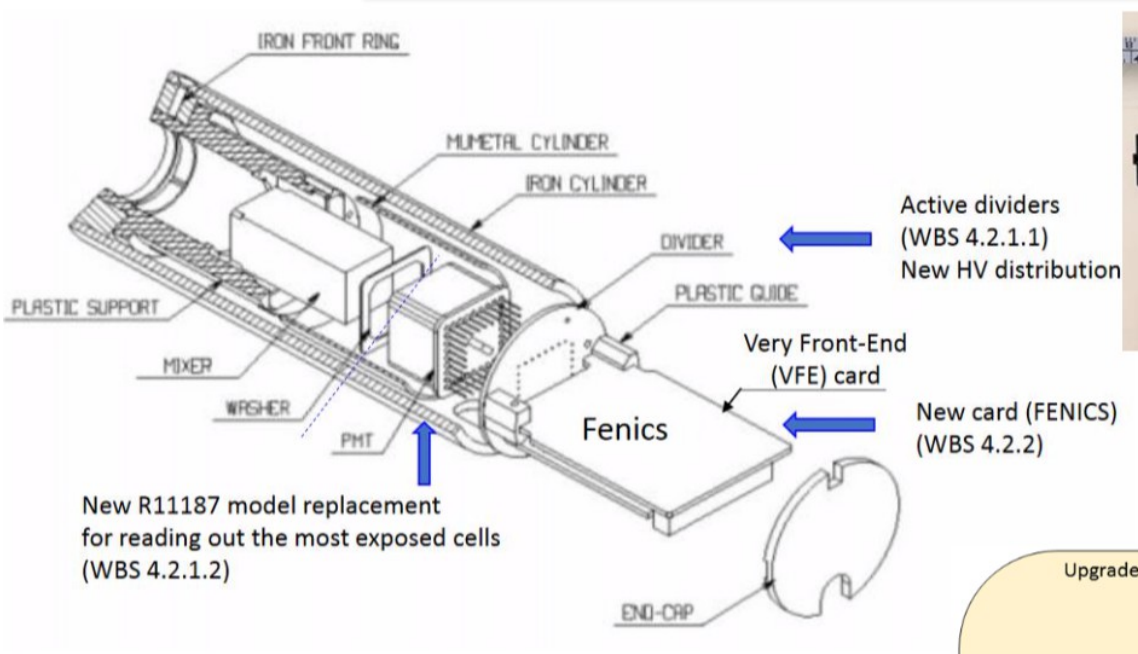
- Front-End electronics are relatively well shielded. Highest exposure in the LB-EB service gap region. For 4000 fb^{-1}:
  - About 80 Gy/15 Gy at barrel/extended fingers

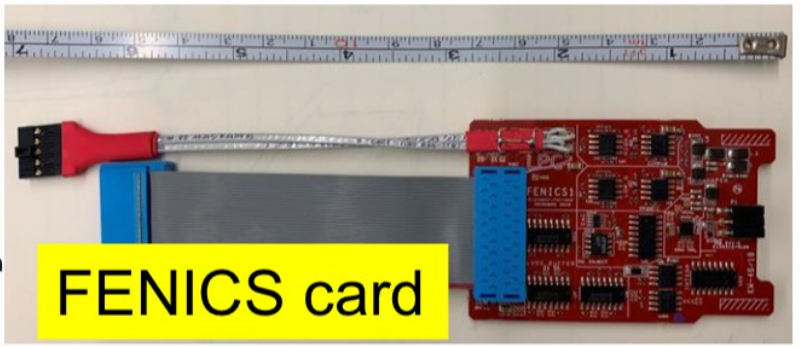


Barrel LVPS boxes including ELMB2 and Daughter Boards are mostly affected subsystems.



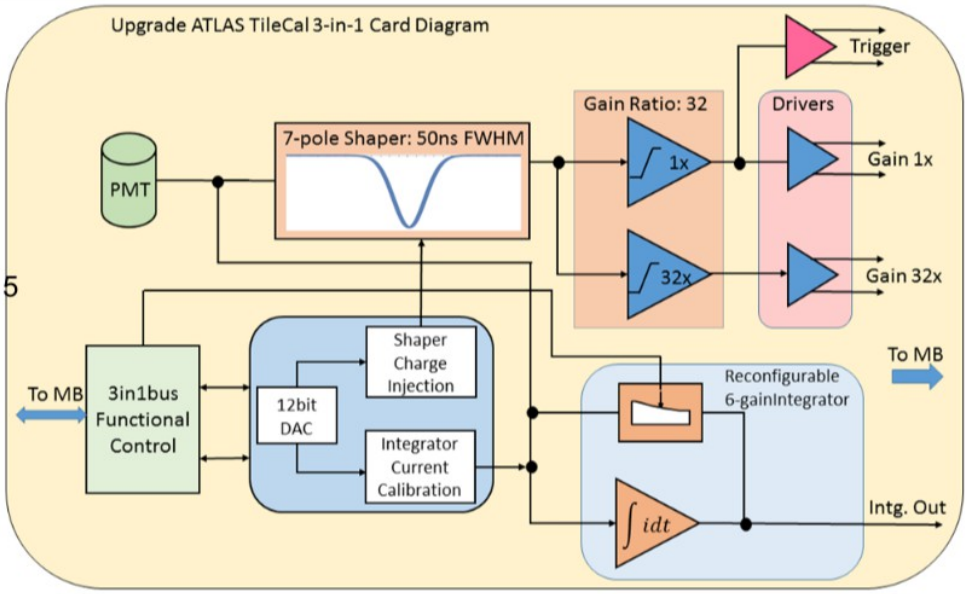
PMT Block and FENICS FEB





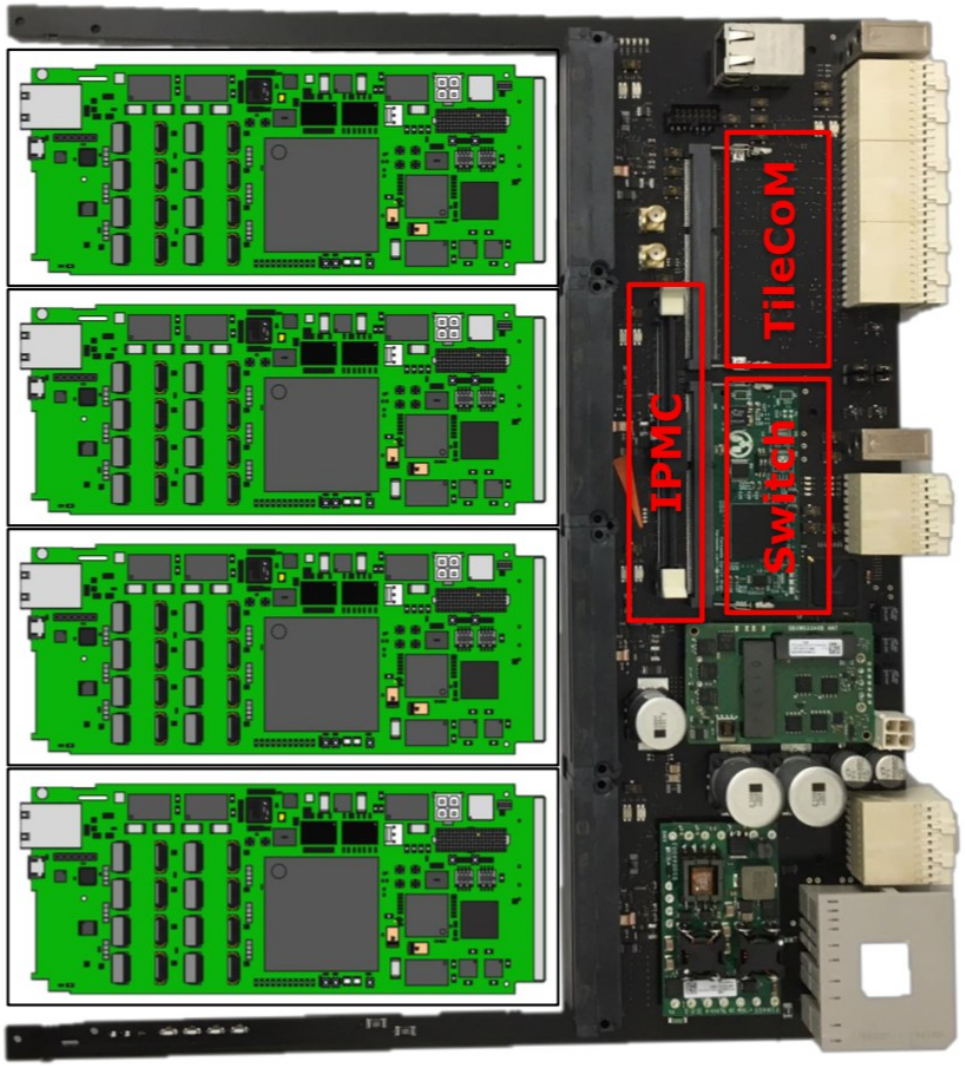
Differences between current 3in1 cards and FENICS cards.

- no trigger output
  legacy system -> an analog sum
  upgrade -> trigger based on calibrated signal digital sums in USA15
- no EPLD (lvds lines from MainBoard control analog switches)
  (the MainBoard FPGAs are in a lower radiation environment)
- improved charge injection switch
  (leakage pulse greatly reduced)
- only 2 voltages needed (instead of 3)
- lower noise and better linearity
- additional (low gain) integrator setting (Luminosity)



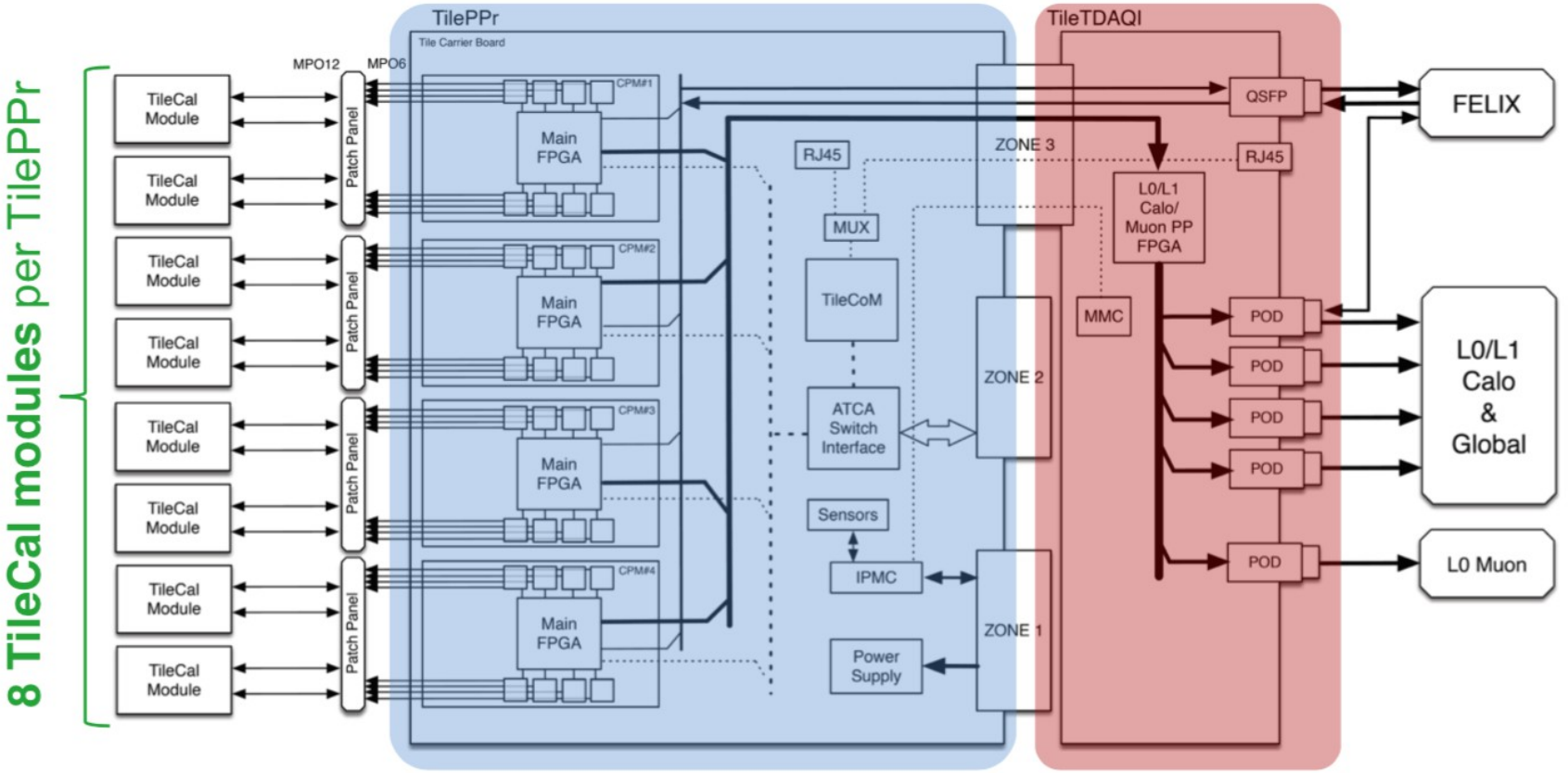
ATCA Carrier Base Board

- **ATCA cutaway carrier** form factor
  - Allows higher components – cooling
  - Provides **up to 400W** for AMCs and RTM
- Three on-board **mezzanines**
  - CERN **IPMC** board
  - **TileCoM** Zynq-based board
    - FPGA remote programming
    - Interface with DCS system
  - **16 GbE port switch** SODIMM
- **First prototypes being tested**
  - Operation inside ATCA shelf **validated**
  - Working on the communication between TDAQi and CPMs
  - **Measured higher diff impedance** than expected (130 Ω wrt 100 Ω on long lines)
  - **Reduce manufacturing** tolerances from 20% to 10% or use the controlled impedance service
  - **Positive** feedbacks from review panel
- **PDR successfully passed on September 17th, 2019**



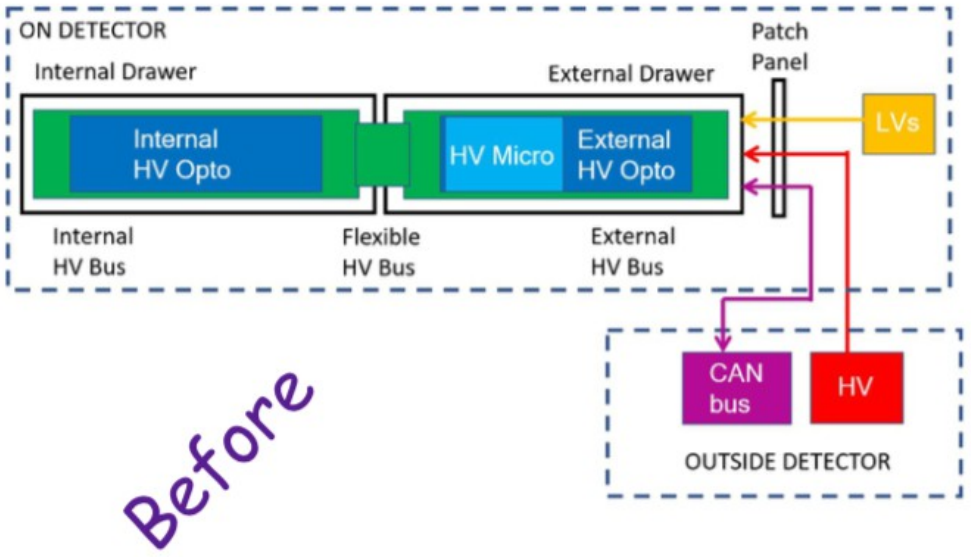
Tile PPr and TDAQi

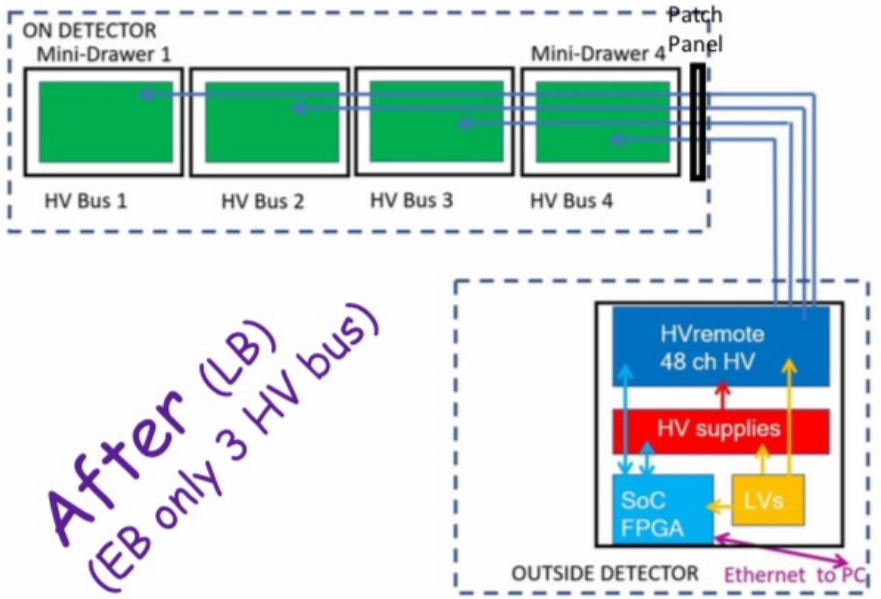
- **Tile off-detector electronics: TilePPr + TDAQi**
  - Data processing and handling from on-detector electronics
  - LHC clock recovery and distribution to the TileCal modules
  - Interface with the ATLAS trigger and ATLAS readout systems (FELIX)



- **32 TilePPr** boards in ATCA format**:** ATCA carrier + 4 Compact Processing Modules
- **32 TDAQi** RTM**:** Interfaces with L0Calo, Global, L0Muon and FELIX system

HV upgrade

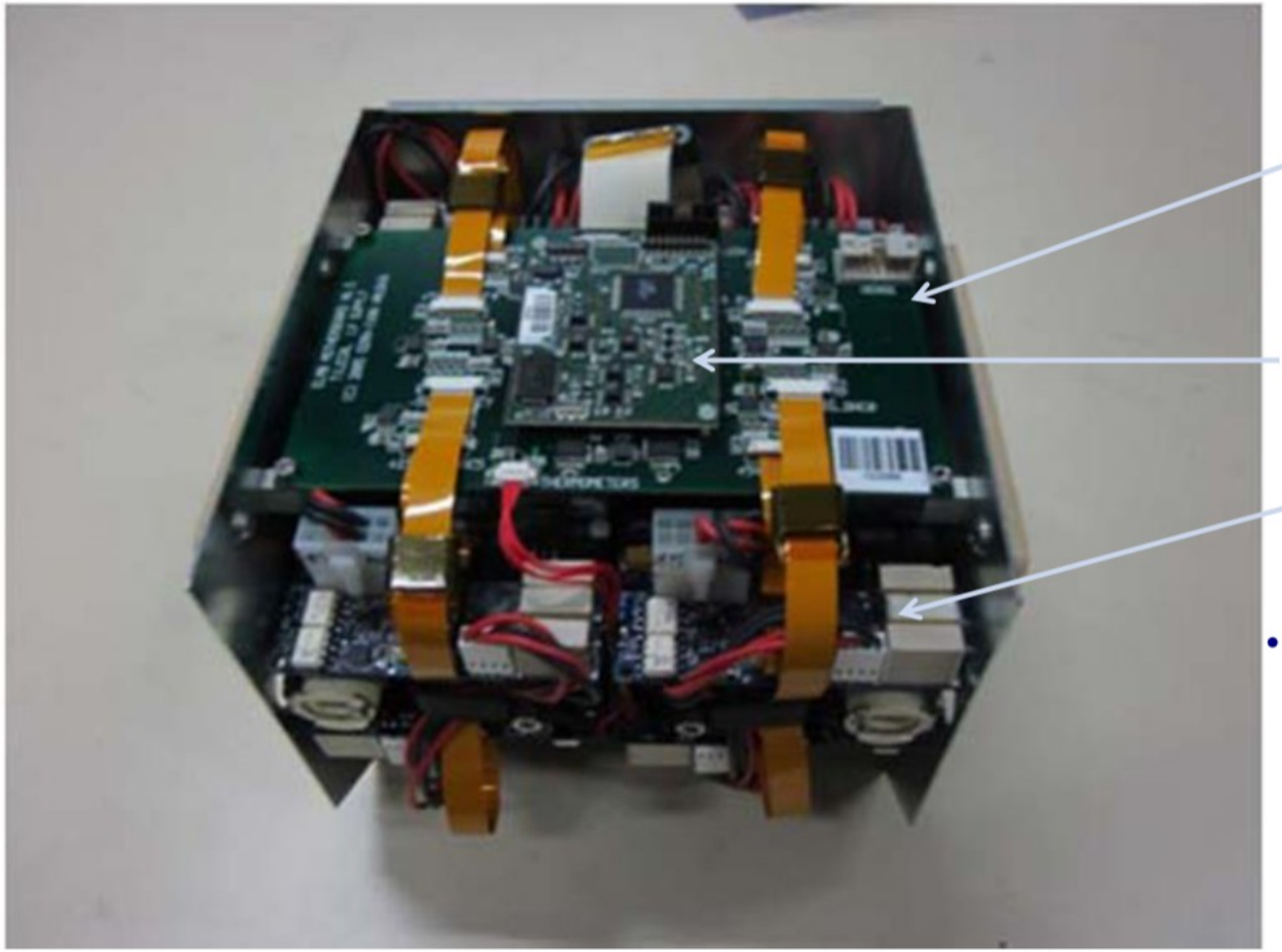




Currently HV regulation inside the detector
Primary HV outside the detector
Only 1 HV input cable per module
Global On/Off
HV boards exposed to radiation
Maintenance possible only in long or end of year shutdowns

Upgrade moves HV regulation outside the detector
Need up to 48 pairs of wires per module
Individual On/Off switches
No radiation
Always accessible for maintenance

LVPS Box

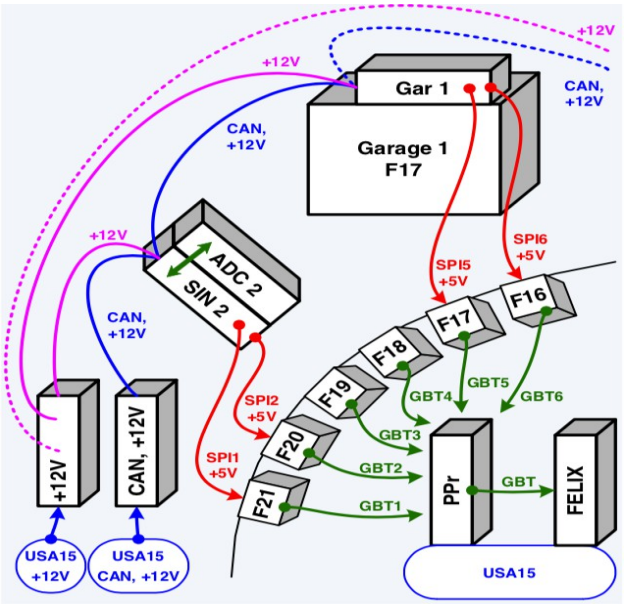


- Motherboard with ELMB2 handles communication between LVbox and Detector Control System
  - set voltages
  - monitor current, temperature

Tile Calibration systems

Cesium system

- Needs higher bandwidth, radiation tolerant data transport.
- Readout done via DaughterBoard (already tested). Option for PDR.
- We may use ELMB++ hub for communication with Cs control system



Laser system

- Upgrade of current system.
- Using commercial component for optics
- DAQ to be reorganized to match PPr system

MinBias System

- FENICs slow readout will be sent to the PPr.
- Higher rate readout than current system.
- Extensive linearity/noise tests were done with good results