International Conference on Computing in High Energy and Nuclear Physics 2019
November 4 – 8, Adelaide

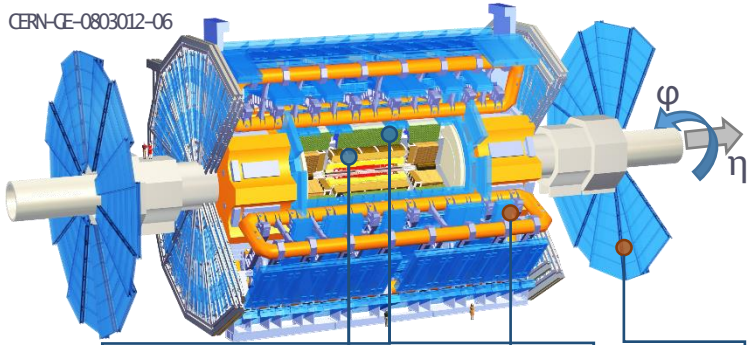
New Jet Feature Extraction and Topological Processor Modules for ATLAS Phase-I Upgrade:

from design to commissioning

Christian Kahra
ckahra@uni-mainz.de
on behalf of the ATLAS collaboration

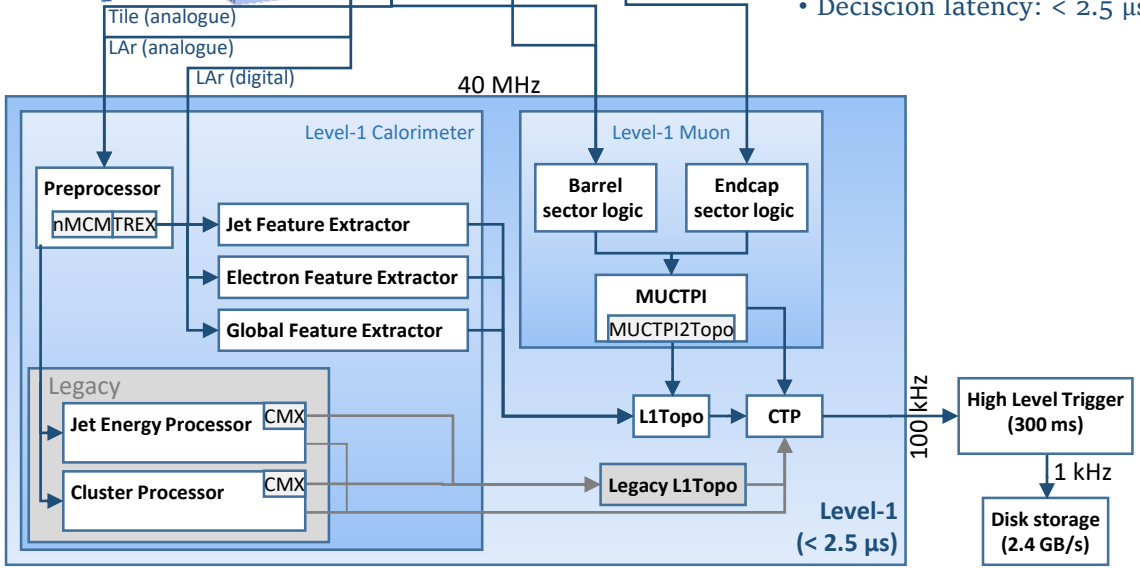
GEFÖRDERT VOM
Bundesministerium für Bildung und Forschung
FSP 103 ATLAS
ATLAS EXPERIMENT
Cluster of Excellence PRISMA
Precision Physics, Fundamental Interactions and Structure of Matter
JOHANNES GUTENBERG UNIVERSITÄT MAINZ
JG|U

ATLAS Level-1 Trigger: Phase-I Upgrade



ATLAS trigger system

- Crucial component of experiment
- Responsible for selecting events of interest
  - Recording rate: 1 kHz
  - LHC bunch crossing rate: 40 MHz
- Level-1 (L1) trigger is first rate reducing step
  - Output rate: 100 kHz
  - Deciscion latency: < 2.5 μs



- Conditions in Run 3
  - Energy: 7 TeV per beam
  - LHC luminosity: 2.0 x 10^{34} cm^{-2} s^{-1}
  - Pile-Up: up to 60 interactions per BC
  - L1Trigger rate ≤ 100 kHz
- Phase-I Upgrade: Physics Motivations
  - Physics sensitivity to electroweak processes
  - Boosted object tagging, H → ττ, vector boson scattering

  → low trigger thresholds (see TDR*)
- Topic of this presentation
  - jet Feature EXtractor (**jFEX**) replaces previous Jet Energy Processor (JEP)
    - Working on finer granularity
  - Upgrade of Topological Processor (**L1Topo**)
    - higher input bandwidth
    - more processing power

      → new functionalities, algorithms

* Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System: CERN-LHCC-2013-018

jFEX

Jet Feature Extractor (jFEX)

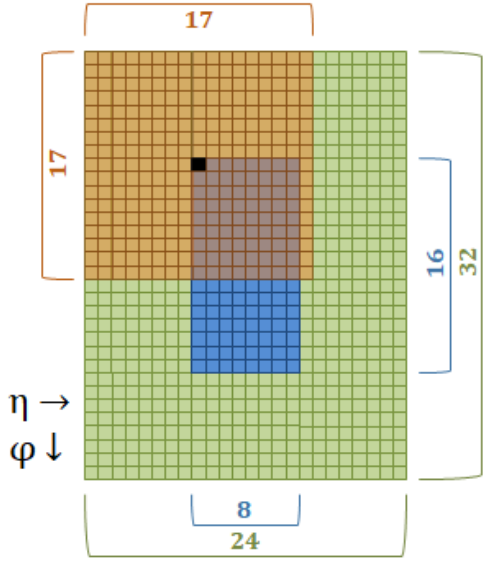
Requirements

Receive 'Trigger Towers' (energy sum of layers of em or hadr calorimeter cells with same η-φ-coordinate) from central and forward calorimeters

- Identification in real-time of jets with and without substructure, taus and forward electrons candidates
  - capability for large-radius jets (up to 1.7 x 1.7 in η x φ)
  - Parallelized identification of local maxima ('sliding window')
    - Comparing energy sums of search windows (0.5 x 0.5) of all possible jet positions
  - Calculation of jet energy sum
- Calculation of ΣE_T and E_T^{miss}
  - Fully exploit calorimeter information (best E_T resolution) at highest possible granularity (up to 0.1 x 0.1)
- Large overlap region necessary for every processor
  - High factor of data duplication
- Latency budget (including serial data transmission): 387.5 ns (=15.5 BC)

→ High input bandwidth and large processing power required

jFEX Processor η- ϕ –coverage



Processor core area (blue)
Overlap with neighbour processor (green)
Maximum window (orange)
around local max (black)

Jet Feature Extractor (jFEX)

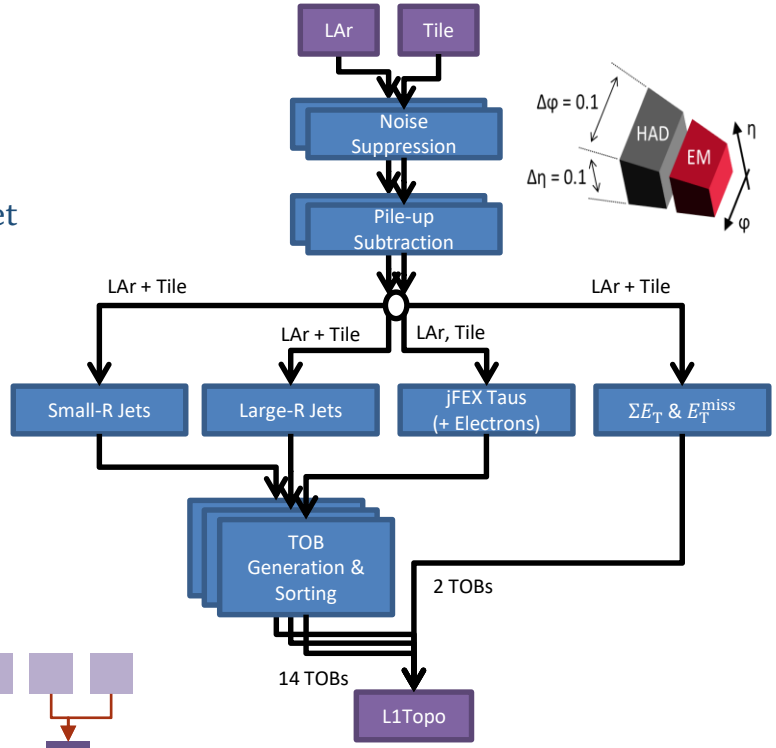
Algorithms

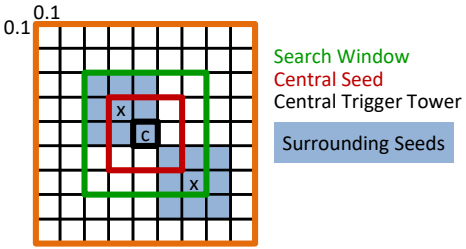
Example: Jet identification via 'Sliding Window' algorithm

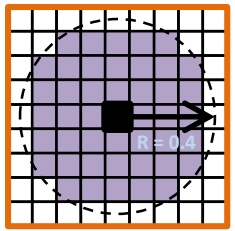
- Summation of Central Seed and of Jet energy sum for every possible jet position in parallel
  - Summation of energies of trigger tower within a radius of 0.4
- Identification of local maximum
  - Comparison of 'Seed energies' with surrounding seeds

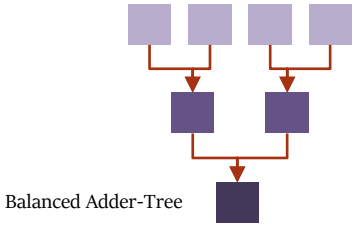
Summation via 'Adder-Trees'

- Binary tree of 2-input adders
- Tree balancing for propagation-time optimization and resource usage









L1Topo

Level-1 Topological Processor

Requirements

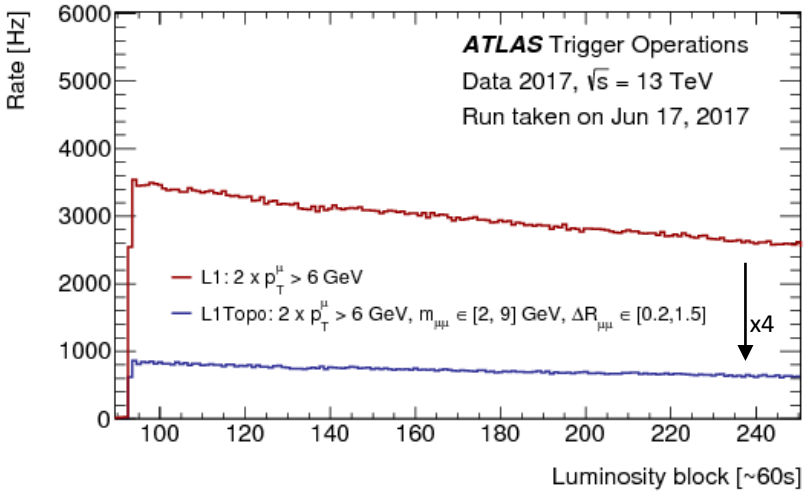
Receive 'Trigger Objects' (TOB) from L1Calo Feature Extractors and L1Muon (MUCTPI)

- Multiplicity triggers for L1Calo objects
- Event selection based on geometric and kinematic relationships
- Evaluation of angular distributions of TOBs:
  - $\phi, \eta, \Delta\phi, \Delta\eta, \Delta R = \sqrt{\Delta\eta^2 + \Delta\phi^2}$

  → Needed also for objects disambiguation
- Calculation of Invariant, Transverse and Effective Mass
- Compound triggers of e/γ, jets, μ, τ, E_T^{miss}

  → Combination of TOBs from calorimeter and muon system
- Consideration of TOBs from other bunch crossings (late muons)
- Legacy system will run in parallel for commissioning in beginning of Run-3

Performance of Run2 L1Topo
L1Topo rate for di-muon trigger with 2017 data
(High pile-up condition: μ > 46)

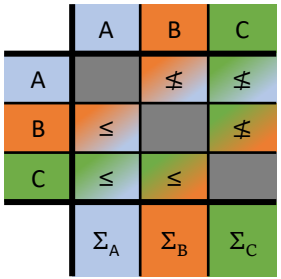


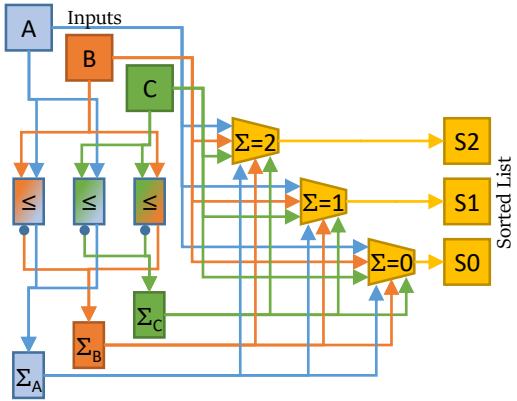
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/TriggerOperationPublicResults

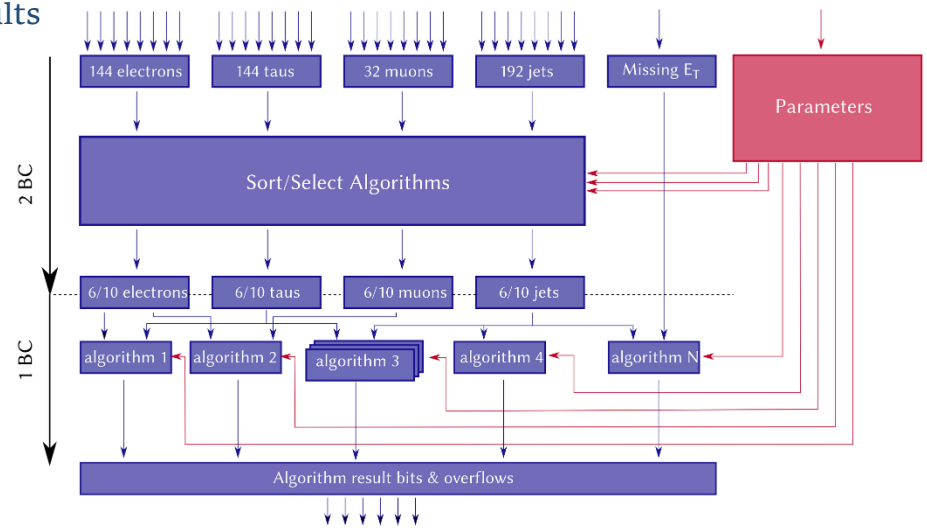
Algorithms

Example: Sorting algorithm in hardware with fixed propagation time

- **First step:** Comparison matrix
  - Comparison of each input pair in parallel
  - 'Count' for each input how often comparator condition was true
- **Second step:** Generation of sorted list
  - Multiplex inputs to sorted list positions by count results







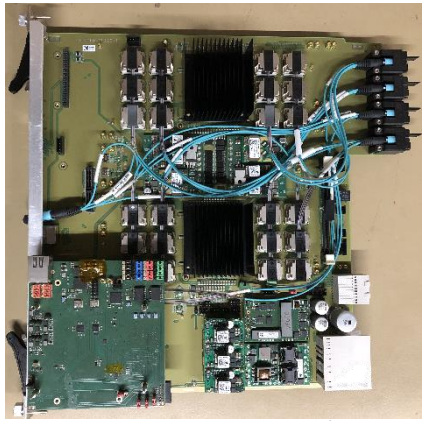
Hardware Design & Verification

Features

- ATCA boards (L1Topo derived from jFEX)
- Processor FPGAs (Xilinx Ultrascale+ XCVU9P)
  - Each processor has 120 high-speed transceiver (MGTs)
  - jFEX: 6 modules with each 4 processors
  - L1Topo: 3 modules with each 2 processors
- Optical receivers/transmitters (Avago MiniPODs)
  - per jFEX processor
    - 5 RX (each 12 links @11.2 Gbps) + 1 TX (each 12 links @12.8 Gbps)
  - per L1Topo processor
    - 10 RX (each 12 links @11.2 or 12.8 Gbps) + 2 TX (each 12 links @11.2 Gbps)

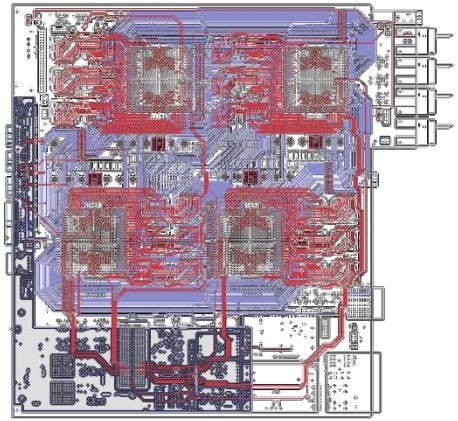
  → Input bandwidth per module: >2.6 Tbps
- jFEX
  - On-module data duplication necessary for φ-overlap
    - Active data duplication inside MGTs (Loopback)
  - Processor-Processor links
    - Per processor 93 Parallel-IO links to neighbour processors available for Pile-Up correction
    - Input bandwidth per processor : 74,4 Gbps (@800 Mbps)

jFEX Final-Prototype



L1Topo Final-Prototype

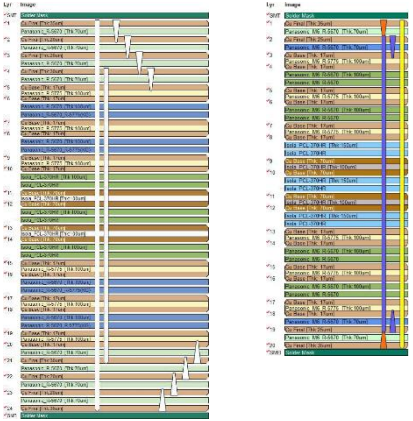
PCB



Layout

Challenges:

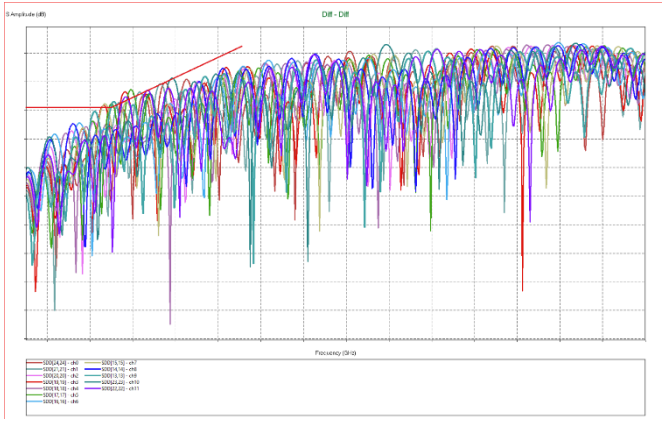
- Tight routing space (breakout of 51x51 BGA)
- Tightly-coupled differential traces
- Drilling aspect ratio and via clearance



Stackup

- jFEX: 24 layers
- L1Topo: 20 layers
- PCB material: Megtron6
- Stacked MicroVias for High-Speed links

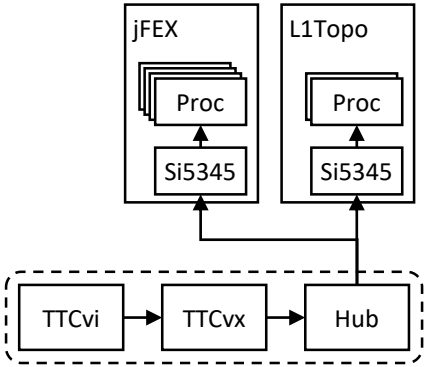
Simulation result for channel return S11

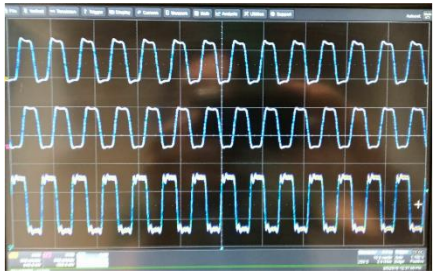


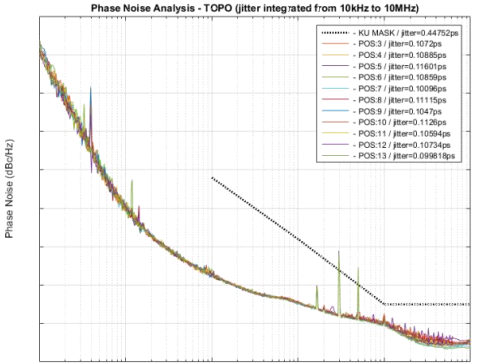
Signal-Integrity simulations

- Layout accompanied by SI simulations of High-Speed links
- Results compared with SFP+ specifications
- Good conformity, no show stoppers

Clock Distribution







System-wide clock

- LHC clock distributed to subsystems via TTC
- jFEX & L1Topo receive TTC clock from ATCA backplane
- Using Si5345 as local Jitter Cleaners on each module

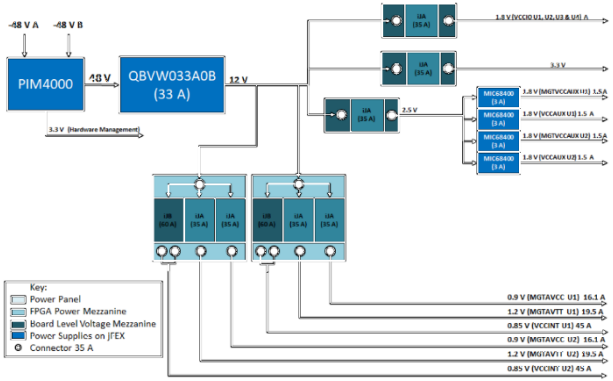
Synchronicity

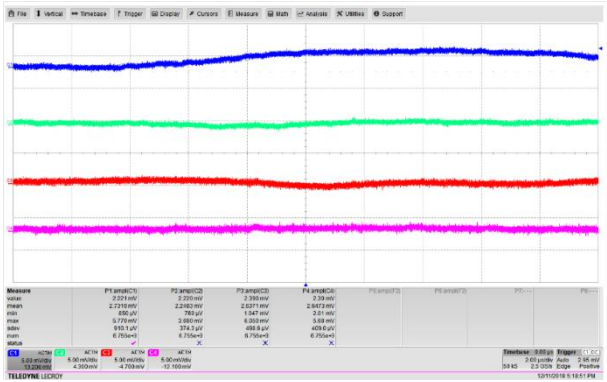
- Link tests (here: jFEX → L1Topo)
- High-Speed Receiver (MGT) recovers clock from serial data stream
- Comparing recovered clock and L1Topo clock
- jFEX and L1Topo are running synchronously

Jitter Measurement

- Phase Noise Analysis (Spectrum Analyzer)
- Within Xilinx specifications for GTY Transceiver Reference Clock
- Test performed with help of *Electronic Systems for Experiments* group (CERN-ESE)

Power Delivery Network





Power Supplies

- iJX series from TDK Lambda
  - iJA (max. 35 A)
  - iJB (max. 60 A)
  - on Power Mezzanines
- Linear Regulators MIC68400

Distribution

Board Level Supplies:

- 3V3, 2V5, 1V8 (each iJA)

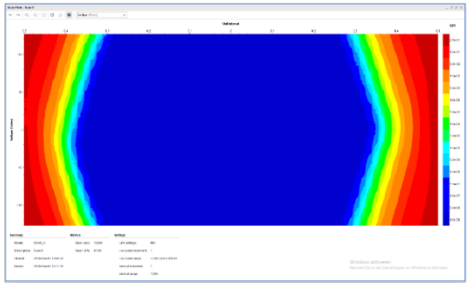
Processor FPGA Supplies:

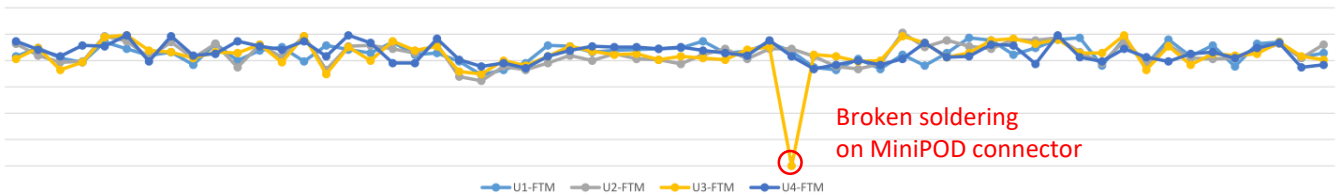
- $V_{MGTAVCC}$, $V_{MGTAVTT}$ (iJA)
- V_{CCINT} (iJB)
- V_{CCAUX}, $V_{MGTCCAUX}$ (MIC68400)

Power Ripple Measurement

- All values within Xilinx specifications (< 10 mV)

High-Speed Links





Bit Error Rate (BER) measurements

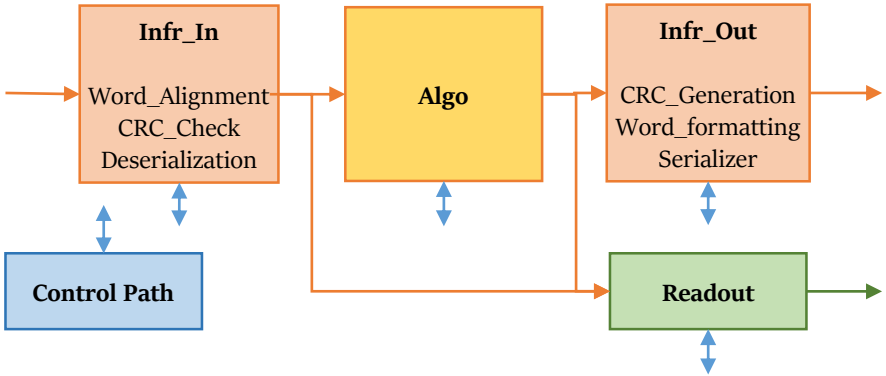
- Sending pseudo-random data (PRBS31) from other modules or via loopback (@ 11.2 Gbps and 12.8 Gbps)
- All links active at the same time
- **BER < 10^{-15}** per link (more than 24 hours)

Margin Analysis (Data Eye Scan)

- During BER measurements scan of error-free region of data eye
- Internal feature of high-speed receivers
  - Second sampler with adjustable offsets in time and voltage
- Scan shows how much margin is left

Firmware & Commissioning

FIRMWARE



Firmware structure

- Hierarchical design consisting of Infrastructure, Control-Path, Real-Time Data-Path (RTDP), Algorithms and Readout-Path
- Complete Processor-Firmware synchronous to TTC-clock
  - Clock-Domain Crossings inside hardware (MGT receiver)
- Processor-FPGAs are multi-die devices
  - Die-to-die connections induce further challenges in firmware design

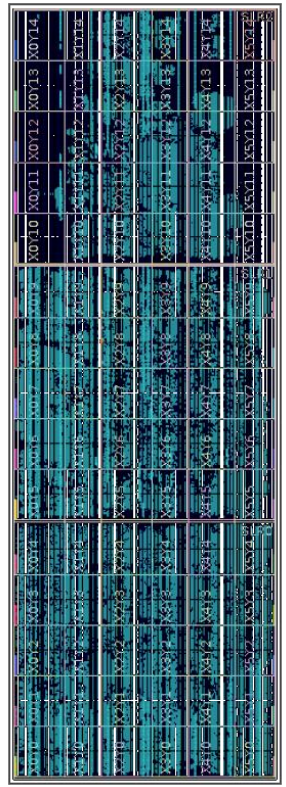
Resource Usage LUTs

- jFEX central: 35%
- jFEX forward: 49%
- L1Topo 1A: 38 %
- L1Topo 1B: 28%
- L1Topo 3A: 39%
- L1Topo 3b: 45%

Commissioning

- System-Level-Tests with other Calorimeter Trigger modules:
  - jFEX – L1Topo okay
  - eFEX – L1Topo okay
  - gFEX – L1Topo okay
  - TREX – jFEX okay
  - LAr – jFEX on-going

eFEX: Electron Feature Extractor
gFEX: Global Feature Extractor



jFEX forward: implemented design

Summary & Outlook

Summary And Outlook

- jFEX and L1Topo are new modules for Phase-I Upgrade of ATLAS Level-1 Trigger
  - State-of-the-art FPGAs provide huge increase in input bandwidth and processing power
  - Design of L1Topo boards derived from jFEX
- Final prototypes / preproduction boards were produced and thoroughly tested
  - Start of both productions at end of the year
  - Commissioning (system-level tests) already on-going
- Commissioning of full system to be finished mid of next year
- Start of Run3: March 2021