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The BIS78 Pad trigger board for the Phase-I Upgrade of the Level-1 Muon Trigger of the ATLAS experiment at LHC

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The BIS78 project

In preparation for the coming years of LHC running at higher luminosity, the ATLAS Muon spectrometer [1, 2] will install New Small Wheel [3, 4] in the end-cap regions (1.05 < |η| < 2.4) and 32 RPC triplets in the transition region between the ATLAS barrel and the endcaps (1 < |η| < 1.3), Resistive Plate Chambers are already used in the ATLAS experiment and provide the muon trigger and two coordinate measurements in the barrel region |n|<1.05.
The BIS78 project proposes to reinforce the fake rejection and the selectivity of the muon trigger in the transition region between the ATLAS barrel and the endcaps (1 < |η| < 1.3), as this region is characterized by high rate due to secondary charged tracks generated by beam halo protons and a lack of detector instrumentation.
Due to the narrow available space, the project foresees to replace the existing MDTs in this area with integrated muon stations formed by small diameter tubes MDT (sMDT) and a new generation of RPC chamber, capable of withstanding the higher rates and provide a robust standalone muon confirmation.
These new RPCs are based on novel design of the gas volume with thinner gas gap (1mm vs 2mm of the legacy RPCs), thinner resistive electrodes, a lower operating voltage and new high gain front-end electronics.
Besides the use in Run-3 and onwards, this project is also of particular relevance as a pilot test in view of the High Luminosity upgrade of the LHC during Long Shutdown 3 when an additional full layer of new RPC triplets is expected to complement the full barrel region in the innermost plane [5, 6].

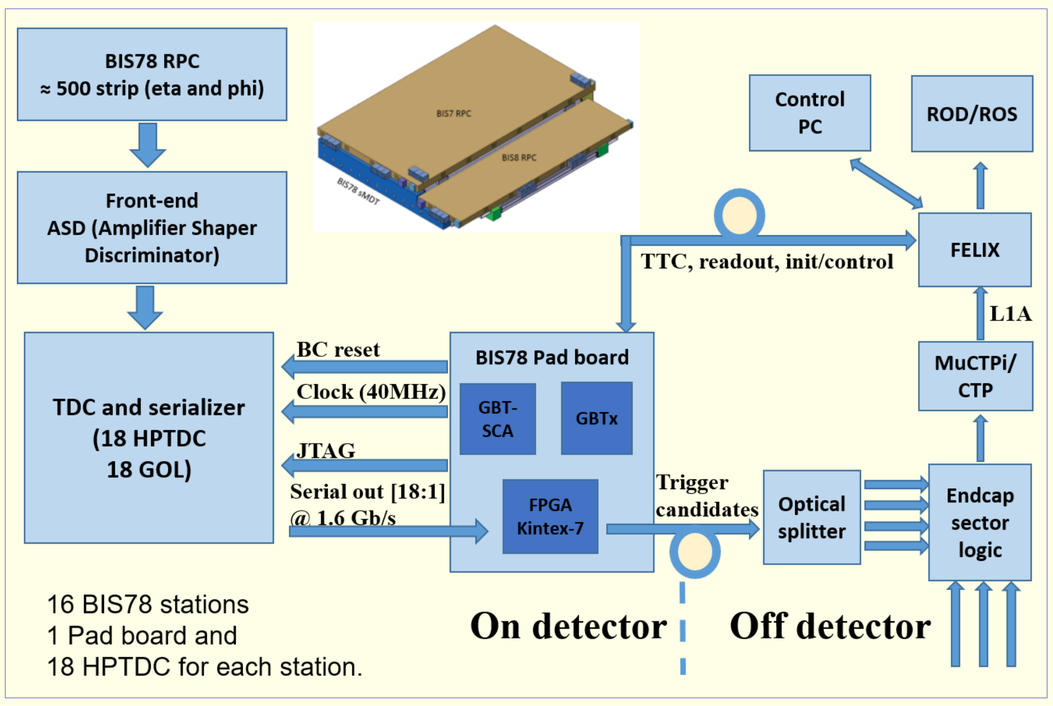


Fig.2: **Block diagram of the BIS78 Muon TDAQ system.**

The BIS78 PAD board

The Pad board is shown in Figure 3; it is designed around a Xilinx FPGA [10], which supports the optical transmission with fixed latency and employs radiation-tolerant techniques to ensure robustness against Single Event Upsets (SEUs) and Total Ionizing Dose (TID) radiation effects.
The expected dose fluence for Phase 2 (i.e. up to 3000 fb^-1) (including safety factors on simulation) are: 6 krad for 10 years HL-LHC(TID), 2.2 x 10^12 1MeV neutrons/cm^2 (NIEL) and 3.75 x 10^11 > 20MeV hadron/cm^2 (3.15 x 10^3 >20MeV hadrons/cm^2/s) (SEE).
The total latency amounts to 40 BC, 1000 ns; in Table 1 are shown the latency contributions.
The Pad board will collect data from front-end electronics, receiving 18 serial data at 1.6 Gb/s from HPTDC board, performing a 2/3 majority logic (3 RPC gas gap) to select a muon candidate and then, after applying a zero-suppression algorithm, it will send data to the off-detector electronics.
Furthermore, the Pad board receives the Trigger, Timing, and Control (TTC) signals from the Sector Logic (SL) board. The data transmission is handled by one GBTx chip [11], which is also locally connected to a GBT-SCA chip [12] for monitoring and configuration, while the trigger data transmission is handled by the FPGA.
The RPC readout data are stored in FPGA and, when a L1-accept signal is detected, by means of GBTx they are sent through the optical link to the Felix system [12].
The BIS78 Pad board is also considered a prototype of the DCT (Data Collector and Transmitter) board, which will be employed in the Phase-II barrel Level-0 muon trigger upgrade.

The BIS78 PAD board in the TDAQ system

The BIS78 Pad is an FPGA-based (Field Programmable Gate Array) board which collects the BIS78 RPC hit data, performs the local trigger coincidence on the hits of the RPC triplets, and sends the trigger information to the off-detector endcap Sector Logic board. The RPC detector readout is done through Felix (Front-End Link Interface eXchange) system [7].

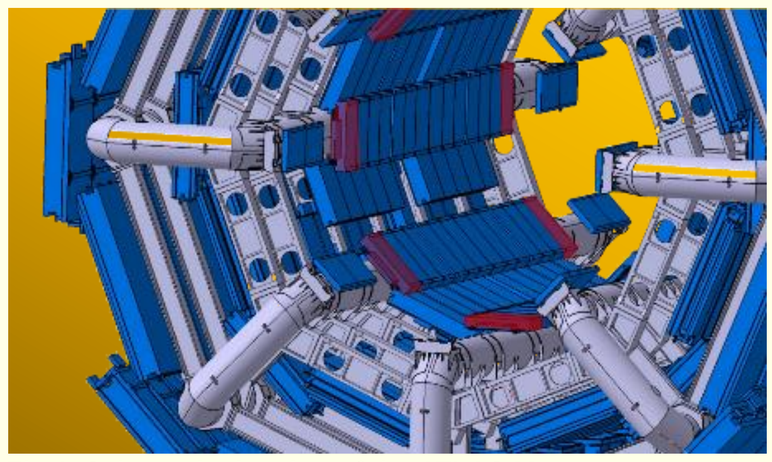


Fig.1: **Schematic drawing of the ATLAS Muon spectrometer, the BIS78 stations are in red.**

Trigger data are transferred to the off-detector endcap Sector Logic boards, which combine the trigger information of TGC, BIS78 RPC and NSW to generate the Level-1 endcap muon trigger candidate. A Pad board will be installed on each of the BIS78 chambers and its signals are treated as illustrated in the TDAQ block diagram of Figure 2.
Each BIS78 RPC station is equipped with 544 eta and phi strips; the hit signal on the strips is amplified, shaped and discriminated by the front-end electronics.
The High Performance Time to Digital Converter (HPTDC) [8] board samples the signals coming from the front-end in order to implement a Time Over Threshold (TOT) measurement; then the digital information coming from the HPTDC is serialized by means of the Gigabit Optical Link (GOL) chip [9] and transmitted to the BIS78 Pad board.

LATENCY CONTRIBUTION	TIME [ns]
T.o.F.	25
RPC strip propagation	10
RPC front-end	10
HPTDC digitisation	360
GOL serialiser	50
Front-end to Pad cable	15
Pad trigger board	200
Fibre to USA15	330

Tab.1: **Latency requirements.**

Test bench results

Preliminary integration tests of the PAD board in the TDAQ system have been made; boards have been configured and tested; HPTDCs have been configured and the FPGA programmed, by means of the Felix system, in the same GBT-SCA JTAG chain; the maximum JTAG frequency is 10 MHz.
The GBT-SCA GPIO and ADC signals (such as temperatures and power supplies) have been tested.
The PAD board is able to receive and send data back to the Felix system in GBT mode at 320 Mb/s (8b/10b E-link encoding).

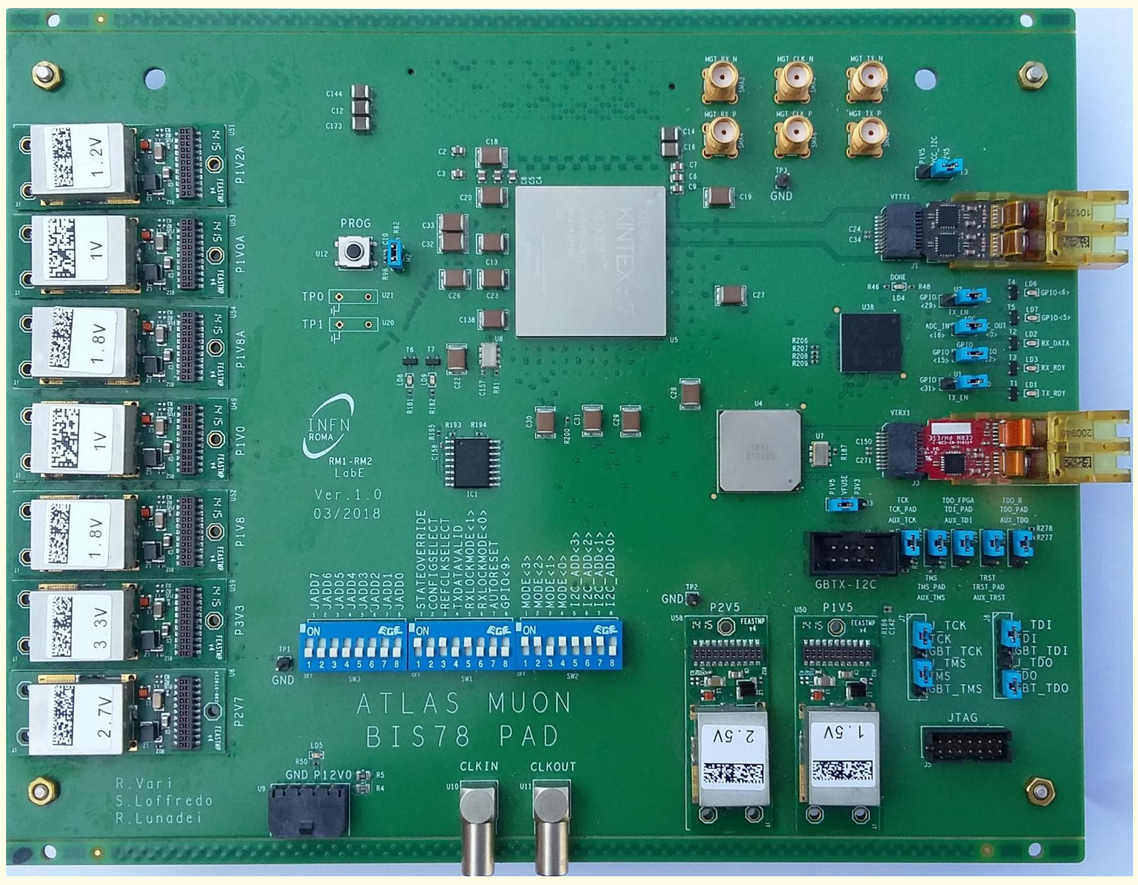


Fig.3: **The BIS78 PAD board.**

All HPTDCs have been correctly readout by means of the TDAQ system.
First integration tests with endcap Sector Logic have been made, in which the link sends trigger data at 6.4 Gb/s, 31 bit PRBS Pattern to the endcap Sector Logic.
IBERT Tests have been made for different fibre lengths (until 200 m) and the PAD output is buffered by means of a 1-to-2 passive optical splitter. The PAD board was always capable to send correctly the data and bit error rate was less than 1.65E-15.
Figure 4 shows the eye diagram of the optical splitter output for a total fibre length of 206 m; it is open widely (48.48 UI opening).

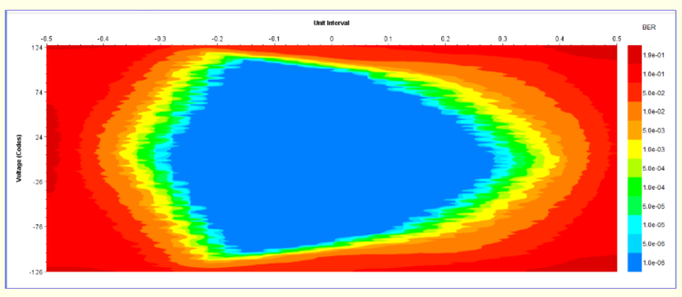
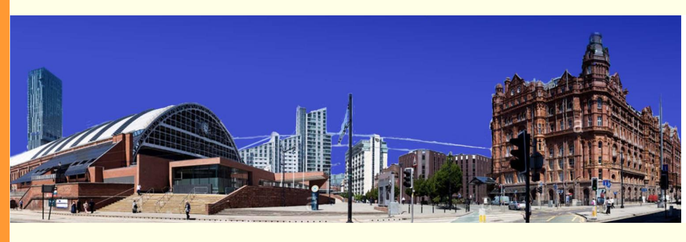


Fig.4: **Eye diagram of the optical splitter output.**



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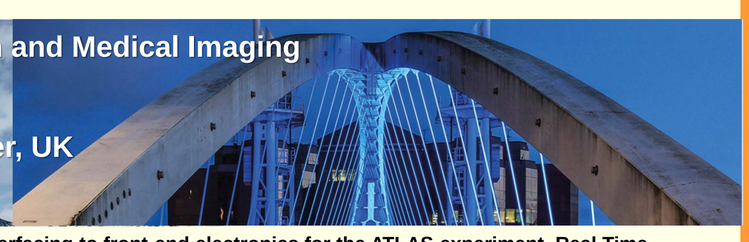

[1] ATLAS muon spectrometer: Technical Design Report. https://cds.cern.ch/record/331068
[2] ATLAS level-1 trigger: Technical Design Report. https://cds.cern.ch/record/381429
[3] New Small Wheel Technical Design Report. https://cds.cern.ch/record/1552862
[4] Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System. http://cds.cern.ch/record/1602235
[5] Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer. https://cds.cern.ch/record/2285580
[6] Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System. https://cds.cern.ch/record/2285584
[7] J. Anderson et al. FELIX: The new approach for interfacing to front-end electronics for the ATLAS experiment. Real Time Conference (RT), 2016 IEEE-NPSS. https://ieeexplore.ieee.org/document/7543142/
[8] J. Christiansen. HPTDC: High Performance Time to Digital Converter. https://cds.cern.ch/record/1067476/files/cer-002723234.pdf
[9] P.Moreira, T.Toifl, A.Kludge, G.Cervelli, A.Marchioro, J.Christiansen. GOL Reference Manual.
[10] https://www.xilinx.com/products/silicon-devices/fpga/kintex-7.html
[11] P. Moreira. GBTX MANUAL V0.15 (2016). https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf
[12] S. Bonacini. GBT-SCA User Manual V8.2 (2017). https://espace.cern.ch/GBT-Project/GBT-SCA/Manuals/GBT-SCA-UserManual.pdf