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VELO Upgrade Module Nomenclature

Abstract

The nomenclature and geometry of the various constituents of VELO upgrade hybrid sensors are defined, as well as their position within the modules. The modules nomenclature and their position along the z-axis are defined.

LHCb Velo Group

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Contents

1 Introduction

As part of the LHCb upgrade, the existing Vertex Locator (VELO) which is based on silicon strip sensors will be replaced by a hybrid pixel detector [1]. This note aims to define the basic conventions of the module layouts and sensor nomenclature. We aim to define the way in which the sensors are arranged on the module and the way in which the modules are physically arranged in each detector half, together with the numbering scheme for the sensors and modules. As a starting point this note uses information from previous detector and software descriptions [2].

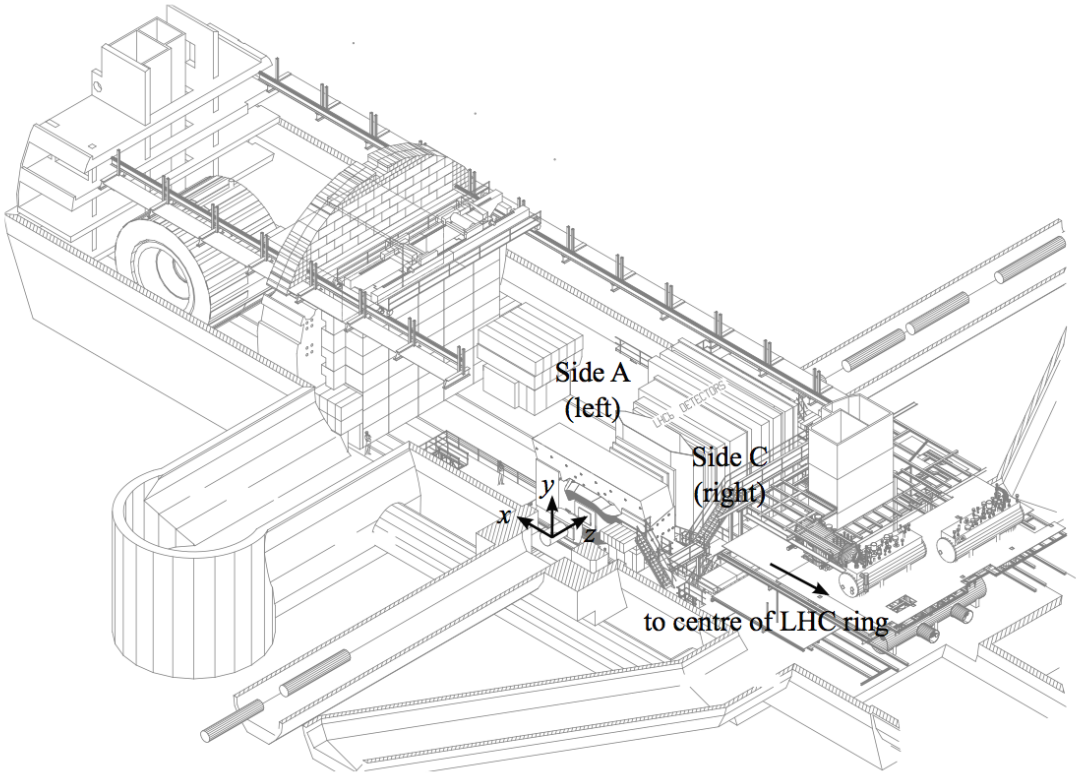

Figure 1: The cavern at LHC Point 8, showing a schematic of the LHCb coordinate system.

The standard LHCb reference system, illustrated in Fig. 1, is used for the global positioning of the modules. It is a right-handed Cartesian system, with the origin placed at the nominal LHC interaction point. The z axis is collinear with the beam line and points in the direction of the muon chambers, and the y axis points up towards the ceiling of the cavern. The x axis then points in the direction of the LHCb counting houses, towards the outside of the LHC ring. The positive x side is commonly referred to as "A side" and the negative x side as "C side".

The overall layout of the upgraded VELO (illustrated schematically in Fig. 2) is conceptually similar to that of the existing VELO. The detector consists of two retractable halves, which are enclosed in aluminium boxes shielding the detector against radio-frequency (RF) pickup from the beam and separating the machine vacuum from the secondary vacuum in

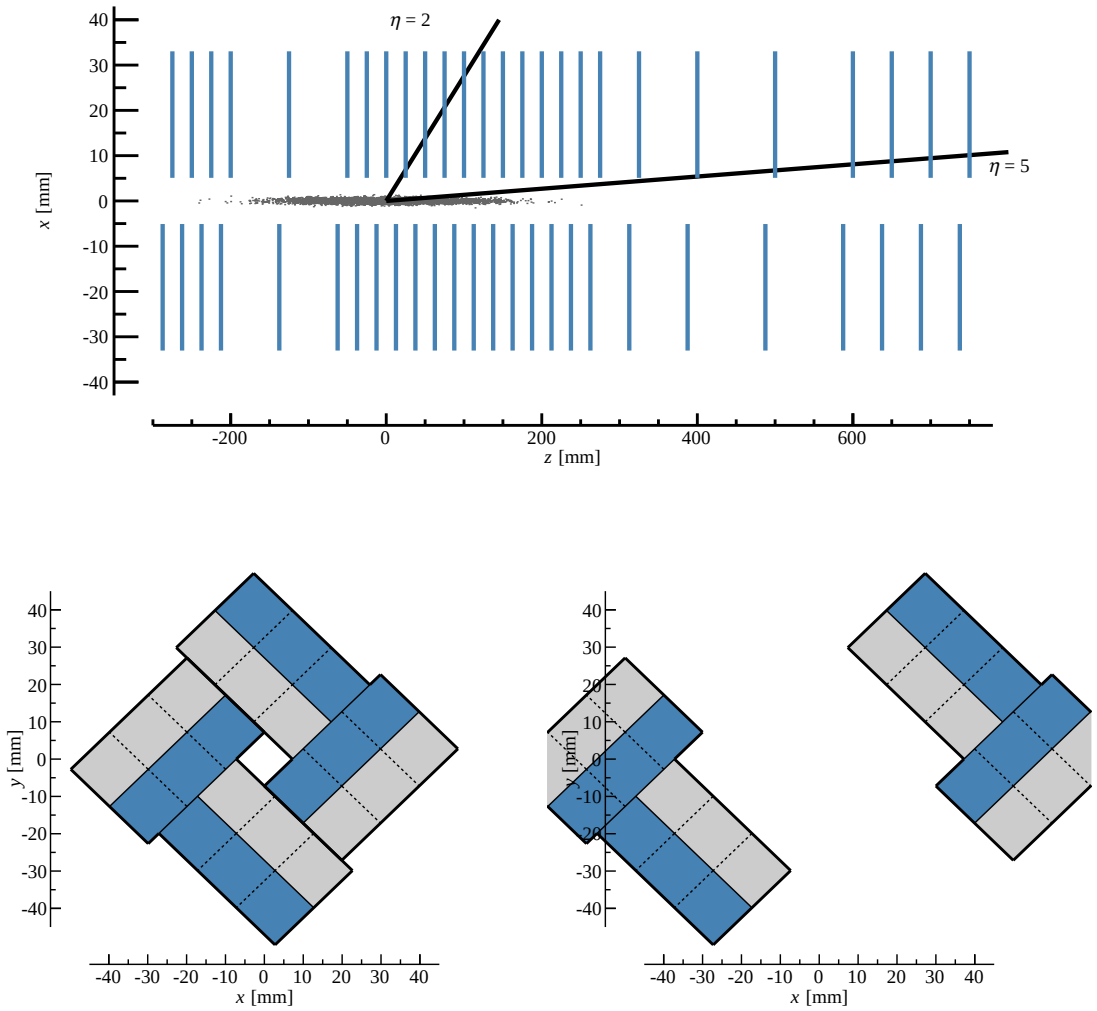

Figure 2: Layout of the upgraded VELO. Top: schematic cross-section at $y = 0$, together with illustrations of the z-extent of the luminous region and the nominal LHCb acceptance. Bottom: schematic layout in the xy plane (left: VELO closed, right: VELO fully open).

which the modules are located. The thin corrugated walls of the boxes facing the beam are known as RF foils. Each of the two halves houses an array of 26 L-shaped silicon pixel detector modules.

2 Silicon tiles

2.1 ASICs

The VeloPix ASIC features a matrix of 256×256 active pixels, with cell dimensions of $55\,\mu\text{m} \times 55\,\mu\text{m}$. On the periphery side of the ASIC, an additional row of pixels is implemented. When the ASIC is bump-bonded to a sensor, this row serves to tie the innermost guard ring of the sensor to the ASIC ground. The distance between the edge of the pixel matrix and the scribe line of the ASIC is $30\,\mu\text{m}$.

The active columns and rows are numbered from 0 to 255. Row 0 is the one closest to and row 255 the one furthest away from the periphery. Looking at the front side (*i.e.* the pixel side) of the ASIC, with the periphery at the bottom, column 0 is the leftmost one.

2.2 Sensors

The 208 silicon pixel sensors for the VELO upgrade are all identical. The sensor is $200\,\mu\text{m}$ thick n-in-p with $450\,\mu\text{m}$ inactive edge width[1]. Each sensor comprises 768×256 pixel implants and is bump-bonded to three ASICs. On three sides of the ASIC the sensor dimensions are larger, such that the ASICs do not extend beyond the sensor. However on the side of the ASIC periphery the region of the ASIC with the wire bonding pads extends beyond the sensor. The metallisation process deposits an additional row of under-bump metallisation (UBM) pads on the innermost guard on one side of the sensor only, connecting the guard ring to the ground row of the ASIC. When the ASIC is bump bonded to the sensor this row serves to tie the guard ring to the ASIC ground, on the periphery side.

Figure 3 shows a sketch of the bump-bonded tile and the pixel matrix layout.

The sensor needs to feature a small gap between the matrices of $165\,\mu\text{m}$ to allow the ASICs to be placed side by side. In order not to lose efficiency the pixels on either side of the gap are elongated by half this distance ($82.5\,\mu\text{m}$), from $55\,\mu\text{m}$ to $137.5\,\mu\text{m}$. A sketch of the inter-ASIC region is shown in Fig. 4.

Taking the above into account, the overall sensor dimensions are

$$\underbrace{256 \times 55\,\mu\text{m}}_{=14.080\,\text{mm (active)}} + \underbrace{2 \times 450\,\mu\text{m}}_{\text{(inactive)}} = 14.980\,\text{mm}$$

in the short dimension, and

$$\underbrace{3 \times 256 \times 55\,\mu\text{m} + 2 \times 165\,\mu\text{m}}_{=42.570\,\text{mm (active)}} + \underbrace{2 \times 450\,\mu\text{m}}_{\text{(inactive)}} = 43.470\,\text{mm}$$

[1] We define edge width (or pixel-to-edge distance) as the distance between the edge of the pixel matrix and the cut edge of the sensor.

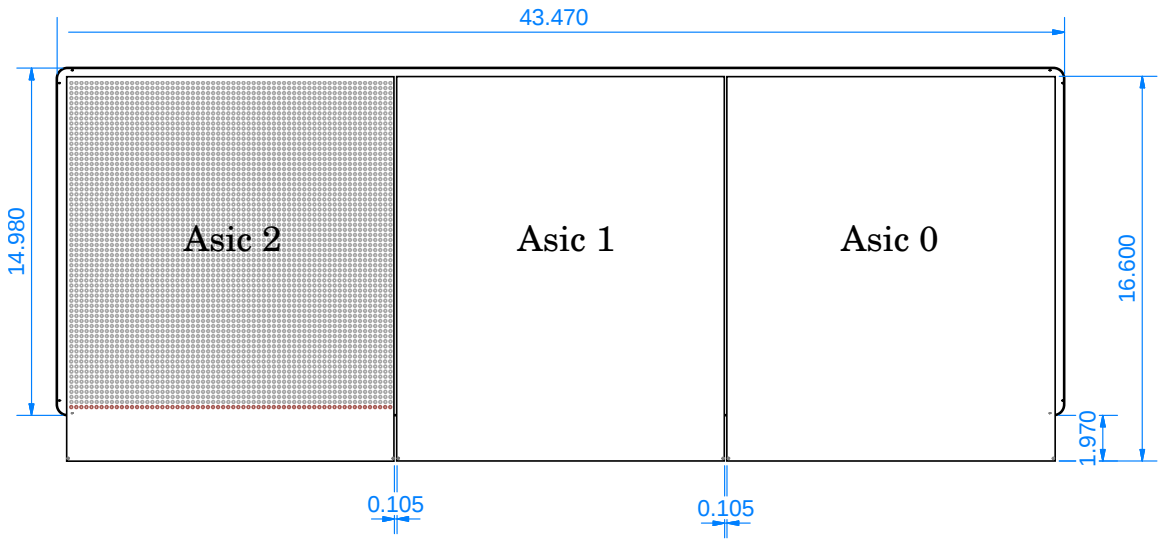

Figure 3: Sketch of the sensor tile, showing the overall dimensions of the sensor and the pixel layout underlying the ASICs. There are 256×256 active bonded pixels (only every fourth pixel is shown in the figure). An additional row of pixels identified in dark red provides a connection between the ASIC ground and the innermost guard ring of the sensor.

in the long dimension. A technical drawing of the sensor is given in EDMS document number 1706379. Note that the sensor size as given in this document corresponds to the requested size of the sensor to the manufacturer, as diced, with a tolerance of 20 μm.

Pixels in each sensor are assigned a (column, row) address, where the row runs from 0 to 255, and the column from 0 to 767. The inter-ASIC columns with elongated pixels are then 255 – 256 and 511 – 512. The column and row numbering scheme as well as the local coordinate system are illustrated in Fig. 6.

A technical drawing of the sensor bonded to ASICs assembly is given in EDMS document 2086903

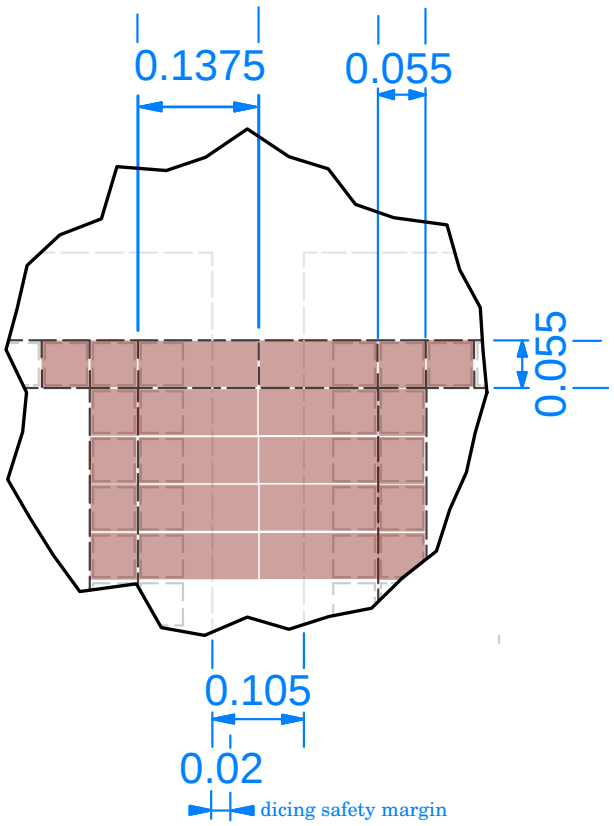

Figure 4: Schematic of the inter-ASIC region. The elongated pixels of the sensors are each $2.5 \times 55\,\mu\text{m}$ long. ASIC pads are in dashed gray while sensor pixels are in shaded red. In addition to the $30\,\mu\text{m}$ between the edge of the pixel and the edge of the chip, the inter-ASIC distance can be reduced by $20\,\mu\text{m}$ on each side from the safety margin taken for dicing.

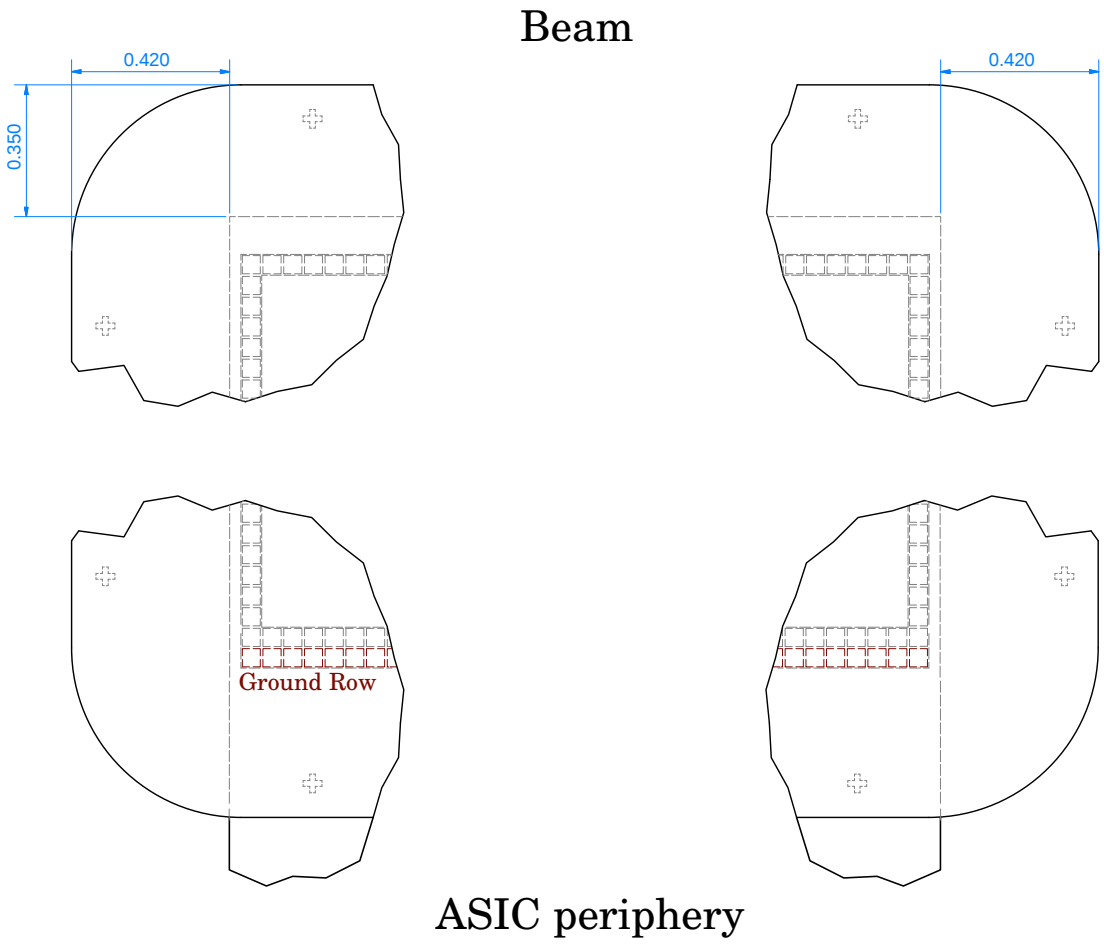

Figure 5: Schematic of the corner regions.

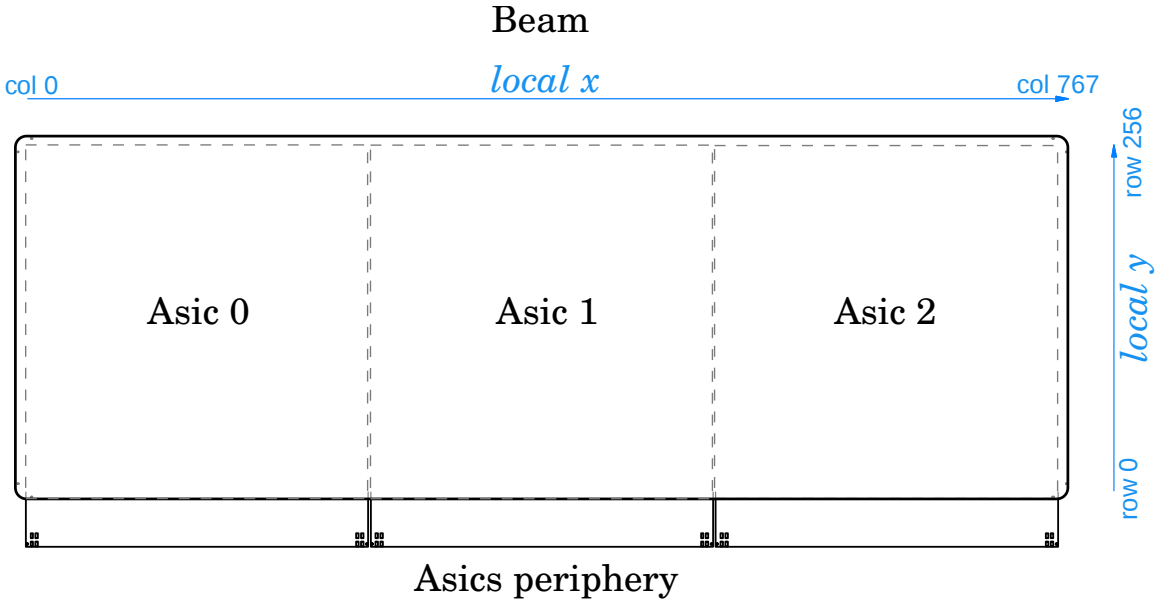

Figure 6: Local coordinate system and pixel numbering scheme of a sensor.

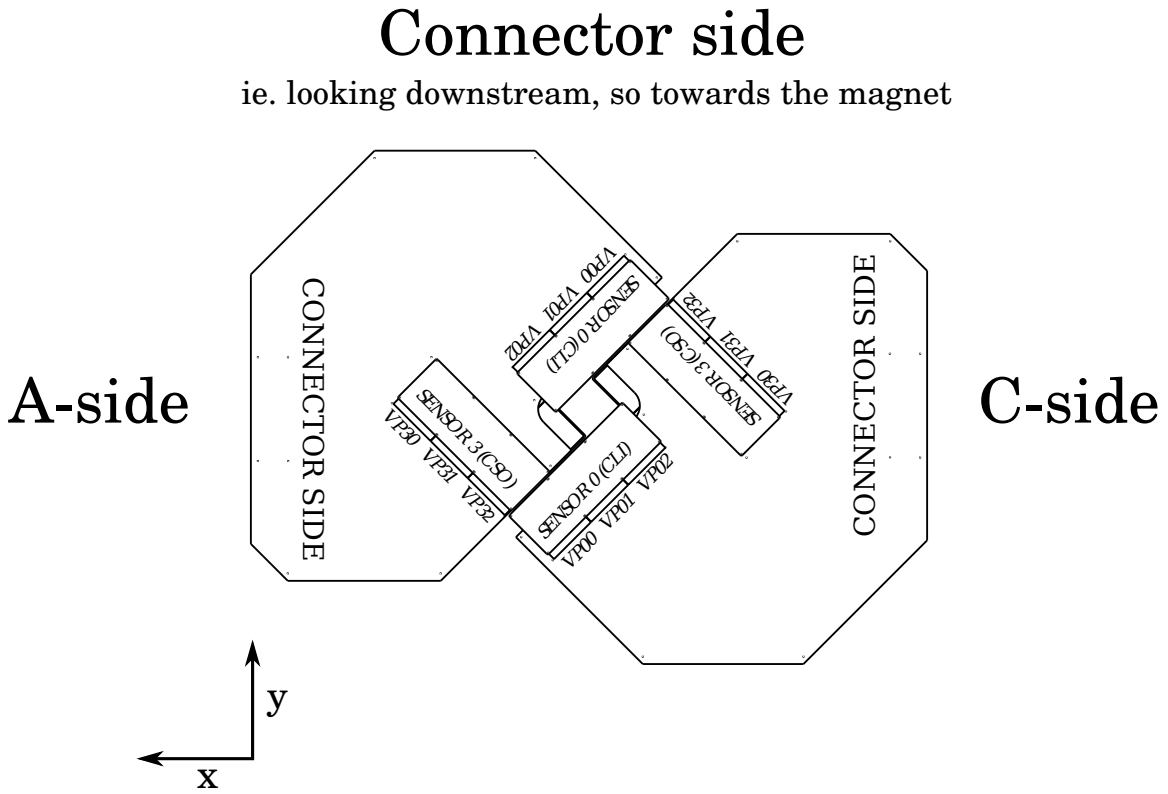

Figure 7: View looking downstream, from the VELO towards the magnet. The connector side of both modules is visible.

3 Module handedness

Each module has an identical sensor layout. Acronyms are used to distinguish the four sensor positions. The module has two faces, distinguished by the face where the cooling connector is soldered. The inside edge of the substrate resembles a letter "L", and the sensors are referred to as being mounted on the long or short side of this "L". Finally, the sensors can be on the innermost or outermost position with respect to distance from the beam. The acroynm indicating the sensor positions then consists of three letters.

- The first letter indicates whether the sensor is mounted on the **C**onnector or **N**on-connector face of the module.
- The second letter indicates the **L**ong or **S**hort side of the substrate.
- The third letter indicates that the sensor is **I**n or **O**ut with respect to the beam.

It is helpful to collect different views of the module from the connector and non-connector side, and with the two modules as mounted in the final experiment. These views are given in Figs. 7 and 8.

The sensor tiles within a module are numbered from 0 to 3. The correspondence between sensor numbers and position acronyms is given in Table 1.

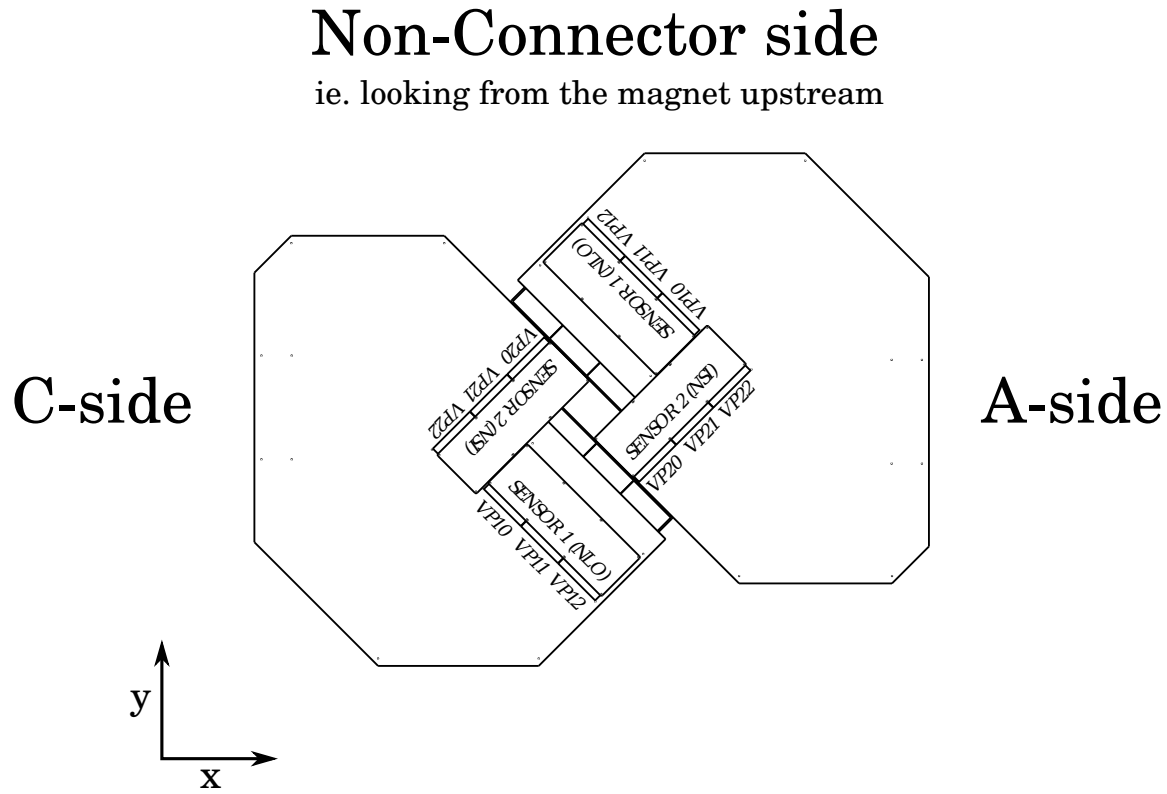

Figure 8: View looking upstream, from the magnet towards the VELO. The non-connector side of both modules is visible.

Table 1: Correspondence between sensor numbers and positions.

Sensor number	Position acronym
0	CLI
1	NLO
2	NSI
3	CSO

A technical drawing of the module layout and nomenclature is given in EDMS document number 1851416.

4 Module positions and numbering

Table 2 shows the positions of the 52 modules, which have been optimised using the full LHCb simulation, then moved to fit on a regular spacing [3]. The modules are arranged in 26 stations (*i.e.* A-C pairs), with A and C side module being separated by $\Delta z = 12.5\,\text{mm}$.

The modules in the half at positive x (A side or "left" half) are assigned odd numbers (starting from 1), while the modules in the half at negative x (C side or "right" half) have even numbers (starting from 0). The numbering of the modules is hence ordered by z-position. as listed in Table 2.

The sensors are also numbered consecutively (from 0 to 207), with sensors 0 – 3 being located on module 0, sensors 4 – 7 on module 1 and so on.

Table 2: Module z layout. The z-positions are given with respect to the nominal interaction point.

Station	C-side			A-side			Mean z
	Module	Sensors	z [mm]	Module	Sensors	z [mm]	[mm]
0	0	0 – 3	−287.50	1	4 – 7	−275.00	−281.25
1	2	8 – 11	−262.50	3	12 – 15	−250.00	−256.25
2	4	16 – 19	−237.50	5	20 – 23	−225.00	−231.25
3	6	24 – 27	−212.50	7	28 – 31	−200.00	−206.25
4	8	32 – 35	−137.50	9	36 – 39	−125.00	−131.25
5	10	40 – 43	−62.50	11	44 – 47	−50.00	−56.25
6	12	48 – 51	−37.50	13	52 – 55	−25.00	−31.25
7	14	56 – 59	−12.50	15	60 – 63	0.00	−6.25
8	16	64 – 67	12.50	17	68 – 71	25.00	18.75
9	18	72 – 75	37.50	19	76 – 79	50.00	43.75
10	20	80 – 83	62.50	21	84 – 87	75.00	68.75
11	22	88 – 91	87.50	23	92 – 95	100.00	93.75
12	24	96 – 99	112.50	25	100 – 103	125.00	118.75
13	26	104 – 107	137.50	27	108 – 111	150.00	143.75
14	28	112 – 115	162.50	29	116 – 119	175.00	168.75
15	30	120 – 123	187.50	31	124 – 127	200.00	193.75
16	32	128 – 131	212.50	33	132 – 135	225.00	218.75
17	34	136 – 139	237.50	35	140 – 143	250.00	243.75
18	36	144 – 147	262.50	37	148 – 151	275.00	268.75
19	38	152 – 155	312.50	39	156 – 159	325.00	318.75
20	40	160 – 163	387.50	41	164 – 167	400.00	393.75
21	42	168 – 171	487.50	43	172 – 175	500.00	493.75
22	44	176 – 179	587.50	45	180 – 183	600.00	593.75
23	46	184 – 187	637.50	47	188 – 191	650.00	643.75
24	48	192 – 195	687.50	49	196 – 199	700.00	693.75
25	50	200 – 203	737.50	51	204 – 207	750.00	743.75

References

[1] LHCb Collaboration, *LHCb VELO Upgrade Technical Design Report*, CERN-LHCC-2013-021. LHCB-TDR-013.

[2] T. Bird *et al.*, *VP Simulation and Track Reconstruction*, LHCb-PUB-2013-018. CERN-LHCb-PUB-2013-018.

[3] T. Bird, M. Gersabeck, T. Head, and G. Lafferty, *VELO upgrade studies and layout optimisations*, LHCb-INT-2014-044. CERN-LHCb-INT-2014-044.