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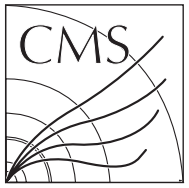

**The Compact Muon Solenoid Experiment**

# Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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# The CMS Pixel Detector for the High Luminosity LHC

Giacomo Sguazzoni on behalf of the CMS Collaboration

**Abstract**

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is expected to collide protons at a centre-of-mass energy of 14 TeV and to reach the unprecedented peak instantaneous luminosity of $5 - 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with an average number of pile-up events of 140-200. This will allow the ATLAS and CMS experiments to each collect integrated luminosities up to $3000 - 4500\,\mathrm{fb}^{-1}$ during the project lifetime. To cope with this extreme scenario the CMS detector will be substantially upgraded before starting the HL-LHC, a plan known as CMS Phase-2 upgrade. The entire silicon pixel detector will be replaced and the new detector will feature increased radiation hardness, higher granularity and capability to handle higher data rate and longer trigger latency. We present the plans and status of the upgrade pixel detector, focusing on the features of the detector layout and on the development of new pixel devices.

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# The CMS Pixel Detector for the High Luminosity LHC

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**Abstract**

The High Luminosity Large Hadron Collider (HL-LHC) at CERN is expected to collide protons at a centre-of-mass energy of 14 TeV and to reach the unprecedented peak instantaneous luminosity of $5-7.5\times10^{34}\,\mathrm{cm^{-2}s^{-1}}$ with an average number of pile-up events of 140-200. This will allow the ATLAS and CMS experiments to each collect integrated luminosities up to $3000-4500\,\mathrm{fb^{-1}}$ during the project lifetime. To cope with this extreme scenario the CMS detector will be substantially upgraded before starting the HL-LHC, a plan known as CMS Phase-2 upgrade. The entire silicon pixel detector will be replaced and the new detector will feature increased radiation hardness, higher granularity and capability to handle higher data rate and longer trigger latency. We present the plans and status of the upgrade pixel detector, focusing on the features of the detector layout and on the development of new pixel devices.

*Keywords:* HL-LHC, Tracker, Silicon pixel detector

## 1. Introduction

The High Luminosity phase of the LHC (HL-LHC) is expected to start in 2026. With a ramping up of the instantaneous luminosity to $5-7.5\times10^{34}\,\mathrm{cm^{-2}s^{-1}}$ by 2028, the aim is to collect between $3\,\mathrm{ab^{-1}}$ and $4.5\,\mathrm{ab^{-1}}$ of integrated luminosity per experiment over about ten years. The HL-LHC will operate at a centre-of-mass energy of 14 TeV with a bunch crossing spacing of 25 ns. The number of pile-up collisions will reach an average of $\sim$140, increasing to $\sim$200 in the best performance scenario. The radiation levels will be unprecedented, especially in the innermost layers of the CMS detector, where a fluence of $2.3\times10^{16}(1\,\mathrm{MeV}\,n_{\mathrm{eq}})/\,\mathrm{cm^2}$ and a total ionizing dose of 12 MGy (1.2 Grad) are foreseen for the baseline integrated luminosity of $3\,\mathrm{ab^{-1}}$. The present Outer Tracker [1] and Phase-1 Pixel detector [2] will be unable to cope with the HL-LHC environment [3] due to the significantly higher rate, the longer latency of the upgraded trigger system, and the fatal consequences of the irradiation. The entire Tracker will thus be replaced [4] during the long shutdown in 2024-2025 (LS3) when the LHC will also be upgraded. The new Tracker, similar to the current one, will be made up of two subdetectors: the Outer Tracker (OT) [5] and the Inner Tracker (IT).

The main requirements for the Tracker upgrade [3] can be summarized as follows:
– radiation tolerance and cold (−20°C) operation, functional up to $3\,\mathrm{ab^{-1}}$ (with margins to comply with the best performance scenario);
– increased granularity (occupancy $< O(1\%)$ for the OT and $< O(0.1\%)$ for the IT) and optimized layout for robust pattern recognition;

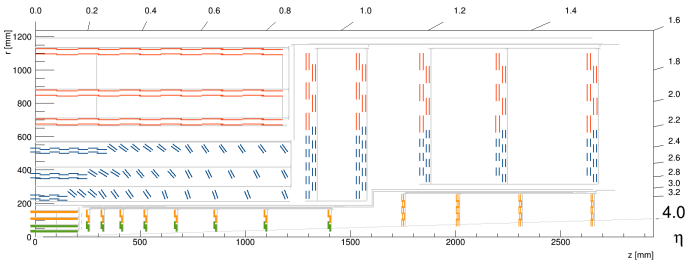


Figure 1: The layout of the upgraded tracker. Yellow and green lines represent IT $2\times2$ and $1\times2$ modules, respectively. Blue and red lines represent OT modules.

– reduced passive material;
– contribution of tracking information towards the Level 1 trigger (applicable only to the OT);
– large readout bandwidth and deep front-end buffers for higher rate (750 kHz) and longer latency (12.5$\mu$s) of the upgraded L1 trigger system;
– extended coverage up to $|\eta|\sim4$ for efficient pile-up mitigation and better physics object reconstruction in the forward region;
– very forward part of IT usable as a luminosity monitor;
– IT fully accessible for maintenance and part replacement.

The layout of the upgraded Tracker is shown in Fig. 1.

## 2. The Inner Tracker

The Inner Tracker consists of $\sim4.9\,\mathrm{m^2}$ of silicon pixel detectors for a total of 2 billion readout channels. The IT is built up from two types of hybrid pixel modules with either $1\times2$ or $2\times2$ readout chips (ROC), organized into four barrel layers (TBPX) plus eight small disks (TFPX) and four large disks (TEPX) per

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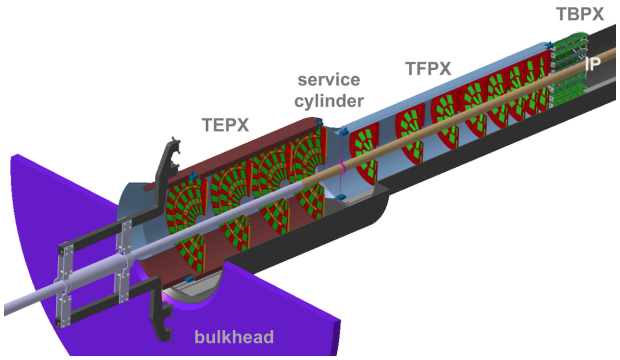


Figure 2: A sketch of the IT mechanical structure showing the various subparts.

side. A quarter of the mechanical implementation of the IT is shown in Fig. 2.

### 2.1. IT Pixel Sensors and Readout Chip

Thin planar n-in-p sensors, with 100 – 150 $\mu$m maximum active thickness, have been selected for the IT for their consistent charge collection efficiency after irradiation. These particular sensors require a high bias voltage (up to 0.8 – 1 kV) and spark protection between the ROC and the sensor. The alternative option of 3D sensors is still under consideration for the innermost layer since this kind of sensor is potentially more radiation tolerant, but requires a more complex fabrication and has larger cell capacitance that impacts front-end electronics noise [6]. A sketch illustrating the concept of the two different options can be seen in Fig. 3.

Two possible pixel aspect ratios are being scrutinized for the IT: $25 \times 100\,\mu\text{m}^2$ (current baseline) and $50 \times 50\,\mu\text{m}^2$. The bond pad pattern stays the same as shown in Fig. 4.

The ROC required for the IT is a technology frontier device that needs to withstand 1.2 Grad of total ionising dose and a maximum hit rate of 3.2 GHz/cm$^2$. It is being developed by the RD53 collaboration [7] in 65nm technology and features a $50 \times 50\,\mu\text{m}^2$ elementary cell, low threshold ($< 1000e^-$), high hit and trigger rate (thanks to up to four 1.28 Gb/s output links), radiation resistance and serial powering capabilities.

RD53A is the first prototype (about half the matrix size with respect to the final chip dimensions of $16.8 \times 21.6\,\text{mm}^2$ corresponding to 336 rows times 432 columns) and it is also being used as part of the IT R&D programme. The final chip prototypes will be available in 2020.

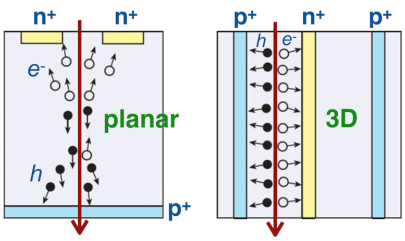


Figure 3: Illustration of planar (left) and 3D (right) pixel sensor concepts.

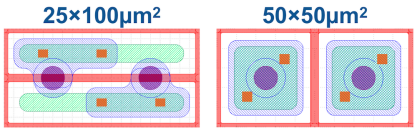


Figure 4: The $25 \times 100\,\mu\text{m}^2$ and $50 \times 50\,\mu\text{m}^2$ pixel cells. Green and violet structures are junction implants and metal layers, respectively, with orange squares representing contacts between them. Red lines are the p-stop profiles. The violet circles are the bump-bond pad openings.

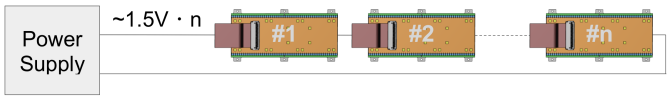


Figure 5: A sketch illustrating the serial powering concept used within the IT.

### 2.2. Serial Powering

Serial powering is the only possible powering scheme compatible with HL-LHC physics requirements, as it provides the 50 kW necessary for the IT, while minimizing the material in the system which can adversely affect tracking performance. It is a major technological challenge though, since it has never been used on large scale. In a serial powering approach the modules are arranged in groups of 8 to 12 into a chain (sketched in Fig. 5). All chain elements receive the same current (by construction) and the voltage is equally shared if all elements represent the very same and constant load. This is the task of the *ShuntLDO*, an IP block of the ROC, shown schematically in Figure 6, that implements the combination of a linear regulator (LDO) and a shunt.

This integrated on-chip solution, the heart of the serial powering capability of the ROC, is intrinsically low mass (no extra ASICs are required) and radiation hard. Since the ShuntLDO is electrically equivalent to a resistor in series with a voltage source, the current sharing gets balanced when ShuntLDOs are operated in parallel. In fact, two ShuntLDOs are operated in parallel on each ROC to independently feed the Digital and Analog domains. Furthermore, ROCs and, consequently, all their ShuntLDOs will operate in parallel within the same pixel module.

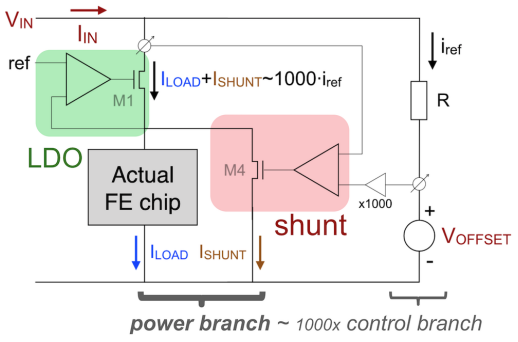


Figure 6: A sketch illustrating the operating principle of the ShuntLDO device featured in the RD53A prototype.

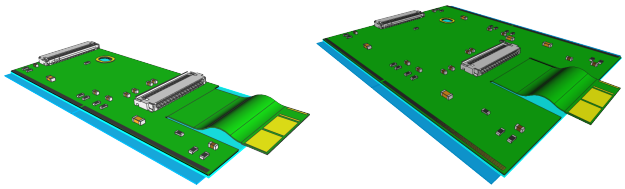

Figure 7: CAD drawings of 1x2 (left) e 2x2 (right) IT pixel modules.

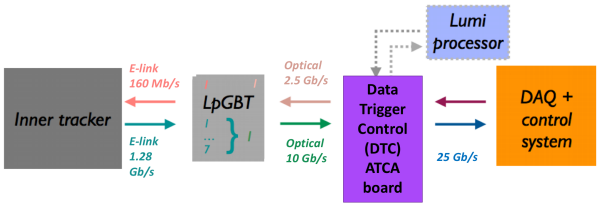


Figure 8: A schematic representation of the IT data acquisition chain.

The serial power approach also has some drawbacks: it is intrinsically inefficient, requiring voltage and current overhead for proper functioning of the LDO and the shunt, respectively. Each module must also have its own local ground, requiring AC-coupled I/O and a non-trivial bias distribution to sensors. Moreover a brand new world of failure modes are possible and need to be carefully studied by extensive and accurate tests at the system level. Nevertheless in the case of CMS, the primary failure mitigation comes from the possibility to fully access the IT for replacement of parts.

### 2.3. The IT Pixel Modules

The IT is based on pixel sensor modules in two flavours, with readout chips in either $1 \times 2$ or $2 \times 2$ configurations, shown in Fig. 7. Each module consists of a sensor bump-bonded to the ROC chips, a High-Density Interconnect (HDI) to distribute signals and power, and additional minimal elements (e.g. aluminium nitride rails) for fixture onto the support structure and to ensure sufficient mechanical strength. No extra ASICs other than the ROC are needed.

### 2.4. Data Flow

The readout and control system, schematically represented in Fig. 8, is based on the Low power GigaBit Transceiver (LpGBT) [8] that embeds both the up- and down- link to/from the detector. Custom electrical links (e-links) are needed to connect the pixel modules to the specific 'portcards' that host the LpGBT and the optoconverter (VL+) [9]. These portcards are placed on the service cylinder (see Fig. 2), where radiation levels are sustainable for the components. Up-links carry data from modules (on receipt of a L1 accept) and monitoring information to the counting room electronics: up to 6 electrical up-links at 1.28 Gb/s are foreseen per pixel module depending on its location, i.e. on the local hit rate, taking into account a 25% bandwidth headroom on e-link occupancy. The down-links take care of clock, trigger, commands and configuration data to modules: one electrical down-link at 160 Mb/s per module is foreseen. Detailed studies are being carried out to optimize the e-link implementation with respect to data rates, reliability and material. In addition, efficient data formatting techniques are being studied targeting a factor of ~2 reduction in data rate to minimise the number of LpGBTs required. At the back end 28 DTC (Data Trigger Control) boards are required for the IT. They will be appropriately interfaced with the luminosity processors for instantaneous luminosity measurements and the central CMS data acquisition (DAQ) system.

### 2.5. IT Luminosity Measurement

During Run-I and Run-II several methods have been deployed in CMS to measure beam conditions and luminosity [10]. Among these, one is based on the PLT (Pixel Luminosity Telescope) [11], a device dedicated to luminosity measurement made up of 16 towers, 8 per side, placed around the beam pipe at $|z| = 1.8$ m. Each tower consists of 3 single-die pixel detectors. The PLT operates in any beam condition and the luminosity figures are extracted from simple triple coincidence (but no track reconstruction) counting corrected for accidentals (due to beam halo). Another method, the PCC (Pixel Cluster Counting) [12], makes use of the pixel detector that operates only in stable beams. The luminosity figures are estimated over a 'lumi-section' (23s) by counting the clusters. This measurement has excellent linearity (thanks to low occupancy), time stability and very good agreement with other luminometers.

This experience will be used in Phase-2 where, thanks to special extra triggers, TEPX will serve as a bunch-by-bunch luminometer for CMS. TEPX will operate during Van Der Meer scans and in all safe beam conditions (ADJUST, STABLE BEAMS). Outside data taking all bandwidth will be available for luminosity triggers. During data taking, luminosity triggers (up to +10%, ~75 kHz) will be added on top of physics triggers. Moreover the innermost rings of the most extreme TEPX disks (falling outside the tracking acceptance of $|\eta| > 4$) will be fully dedicated to BRIL ('Beam Radiation Instrumentation and Luminosity') functionalities, e.g. beam background and luminosity measurements during Machine Development and other unsafe beam conditions. For these applications hermetic coverage is not required and occasional failures are tolerable. Thanks to the complexity and acceptance of TEPX, several methods are under study for the luminosity measurement: cluster counting that is characterized by high statistics but suffers from large fake rate; multi-hit 'stub' counting using overlaps that would allow for a reduction of the fake rate while still maintaining fairly large statistics; or track counting that would need additional processing in the back-end processors.

### 2.6. Cooling

The Tracker will be operated and maintained well below −20°C using a two-phase $CO_2$ cooling system running at −30°C. The total power dissipated by the Tracker within the tracking volume is estimated to be around ~100 kW for the OT and ~50 kW for the IT. The cooling system is a common system that serves OT and IT and relies on five identical 50 kW cooling

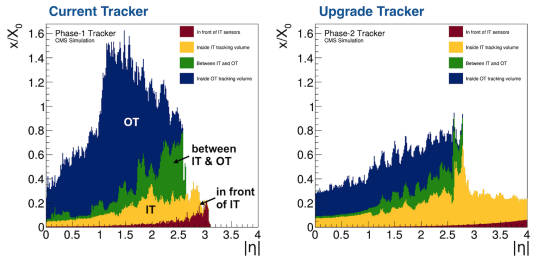


Figure 9: Material budget comparison for the Phase-1 and Phase-2 tracker detectors.

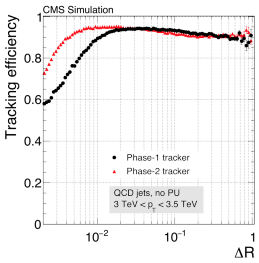


Figure 11: Track reconstruction efficiency as a function of the distance $\Delta R = \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2}$ from the jet axis for the Phase-1 and upgraded Phase-2 tracker detectors.

plants. For redundancy, one is kept always on stand-by ready to take over if needed.

### 2.7. Material Budget and Performance

The upgrade project aims to significantly reduce the impact of the tracker material with respect to the current Phase-1 Tracker. In fact, overall, the estimated material budget of the upgraded Tracker shows a significant reduction thanks also to the serial power concept, in particular around $|\eta| = 1.5$, as visible in Fig. 9 where the Phase-2 vs. Phase-1 comparison is shown.

Some highlights of the expected offline tracking performance for which the IT plays a significant role are discussed in [4]. For other results please refer to [5].

The track reconstruction efficiency for the Phase-2 detector at a pile-up of 140 and 200 for simulated $t\bar{t}$ events, shown in Fig. 10 (left) for $t\bar{t}$, would be as good as the tracking efficiency with the current detector at a pile-up of 50. The fraction of reconstructed fake or duplicate tracks would be slightly higher, but still adequate for CMS event reconstruction. The forward and very-forward extension of the pixel detector extends the $|\eta|$ range by about 1.5 units. The impact of the much better granularity and the reduced passive material on physics performance is visible in Fig. 10 (right) where the resolution on the transverse impact parameter is improved by a factor ∼2 going from the Phase-1 to Phase-2 detector.

The ability to perform track reconstruction in a dense environment such as the core of a jet is an important figure of merit for a tracking device at a pp collider. The resolutions

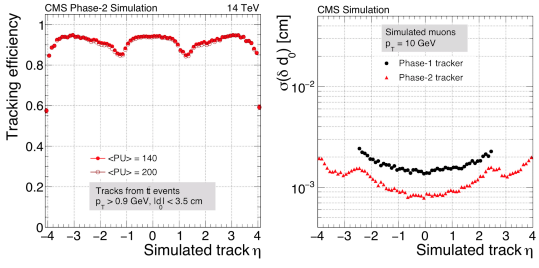


Figure 10: Tracking performance as a function of $|\eta|$: efficiency on simulated $t\bar{t}$ events at pile-up 140 and 200 (left) and muon transverse impact parameter resolution in the comparison between the Phase-1 tracker and the upgraded, Phase-2, tracker (right).

of jet-related observables very much depend on the possibility to disentangle (e.g. by using vertex information) the tracks belonging to the jet with respect to pile-up tracks accidentally close-by. The clear improvement in this respect is visible in Fig. 11 where the track reconstruction efficiency as a function of the distance $\Delta R = \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2}$ from the jet axis is shown for the Phase-1 and Phase-2 tracker detectors.

## 3. Conclusions

The Inner Tracker is the new CMS pixel detector that will be deployed in the context of the Phase-2 upgrade of the CMS Tracker detector for HL-LHC. The development of the Inner Tracker is well advanced. The detector layout is being optimized and finalized and several R&D activities are ongoing on sensors, electronics and mechanics. The project will soon enter into parts production and integration.

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