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An 8-Channel ASD in 130 nm CMOS for ATLAS Muon Drift Tube Readout at the HL-LHC

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Spatial resolution and efficiency of the ATLAS muon Monitored Drift Tubes (MDT) depend on drift time resolution, noise levels, and accurate threshold setting. A new 130 nm readout device is developed and optimized for the required time resolution, to guarantee rise times below 10 ns with acceptable time slewing effects. Moreover, the large chain-amplification results in increased sensitivity to any disturbance, mainly from the supply. To avoid additional costs to clean up the setup from such disturbances, the readout chain adopts innovative techniques at system, circuit, and design levels. These are minimizing readout chain disturbance sensitivity. This paper describes the achieved performance by showing measurement results and presenting resolution studies taken in a high energy test beam at CERN.

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1. The Role of the ASD Chip in the ATLAS Muon Spectrometer

The precision muon track measurement in the ATLAS experiment is performed by monitored drift tubes (MDTs). These are gaseous detectors consisting of an aluminum tube with a tensioned wire in its center. A high voltage of $\approx$ 3 kV is applied to the wire and the tubes are filled with Ar/CO_2 gas (93% / 7%). They are stacked up to chambers covering the outside of the ATLAS detector. The tiny charge signal on the order of a few femtocoulomb generated on the wire by a muon is fed into the amplifier, shaper and discriminator (ASD) ASIC. The output of the ASD is discrete in level (digital) and continuous in time. The track information can be derived from the time of the threshold crossing and is measured by a time-to-digital converter (TDC) chip, which sends its data to the muon readout system. Both chips are located on a front-end mezzanine card. [1]
The ATLAS muon spectrometer consists of about 1,150 MDT chambers, hosting more than 14,000 mezzanine cards with about 43,000 ASD chips. As the peak instantaneous luminosity at high luminosity LHC (HL-LHC) is expected to rise by a factor of 7 to $\mathscr{L} = 7 \cdot 10^{34}$ cm^{-2}s^{-1}, there will be an increased muon hit and background rate. In order to cope with this, the MDT front-end mezzanine cards will be exchanged with new electronics featuring high bandwidth low latency electronics.
The new ASD2 chip is designed in a relatively modern 130 nm CMOS process. It will replace all of the ASD chips currently installed in ATLAS. The key parameters could been taken over from the already existing chip. They are summarized in table 1.

Input impedance	Z_{in} = 120 Ω
Equivalent noise charge (ENC)	6,000 e$^-$ RMS $\approx$ 5 primary electrons (pe$^-$)
Shaper peaking time	t_p = 15 ns
Sensitivity at discriminator input	1.65 mV/pe$^-$ (with gas gain = $2 \cdot 10^4$) = 8.9 mV/fC
Linear range	900 pe$^-$ = 1.5 V
Discriminator threshold	-255 … 255 mV (in steps of 2 mV)
Programmable dead time	20 … 535 ns
Number of channels	8

Table 1: Key parameters of the ASD chip. [2]

2. Measurement Results of the Latest ASD2 Prototype (ASD2v5)

The current ASD2 prototype (ASD2v5) has been thoroughly tested and examined using a semi-automated setup. It consists of commercial off-the-shelf (COTS) components, custom designed FR4-PCBs and software. The chip die is directly glued and bonded onto the board and protected by a black glob top. A charge can be applied to the input using a voltage step over a capacitor, where $Q = C \cdot \Delta U$. Measurements can be taken at the analog test output of channel 8 or at the 8 digital outputs. Using a small adapter board, the new chip can be placed on existing well characterized mezzanine cards, where its performance can be easily studied and compared to previous results. [5]

2.1 Analog Performance

In most of the crucial parameters the ASD2v5 shows a better performance than the legacy ASD. It has a fast peaking time of 9–15 ns shown in figure 1 compared to 13–23 ns of the legacy chip. This results in less time-slewing and thus a better spatial resolution. Figure 2 shows an excellent linear range for small charges, which is essential for time slewing corrections using the pulse height information. The first return to the baseline is about 5 ns faster than in the legacy ASD, which corresponds to the faster rise time. The saturation behavior after large input pulses of 2000 fC is good. The latest return to the baseline happens about 350 ns, which is comparable to the legacy ASD. [5]

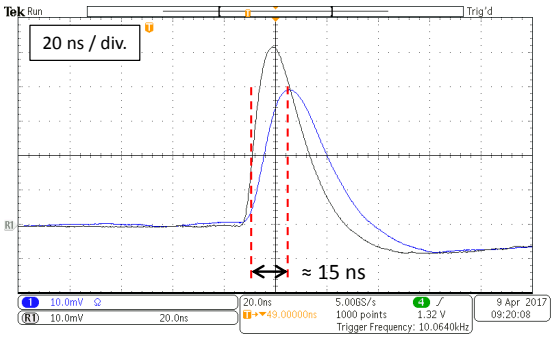

Figure 1: Peaking time of the ASD2v5 with (blue) and without (black) 56 pF capacitive load at the input.

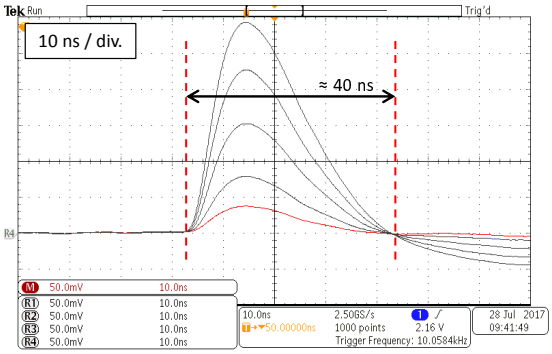

Figure 2: Analog output waveform over input charge steps of 5, 10, 20, 30, 40 fC.

2.2 Threshold Scans, Channel-to-Channel and Chip-to-Chip Uniformity

Threshold scans are a powerful tool to extract parameters like effective threshold, linearity, noise, channel uniformity, etc. from the digital outputs. During the scan, a given charge is applied to the input with a given frequency of 1 kHz. The output is monitored with a counter, while the threshold setting of the ASD is varied. The count rate changes with the threshold forming an S-like curve a plotted in figure 3.

The threshold scans show that the ASD2v5 has less noise, a better channel-to-channel and chip-to-chip uniformity than the legacy ASD. The total threshold variation of 13 tested ASD2v5 chips is only 8 mV, whereas the legacy ASD shows a spread of 17 mV among two chips. Uniformity is important because there is only a common setting shared by all 8 channels. So the value needs to be adjusted in order to satisfy the worst channel, which will be sub-optimal for the best channel. All ASD2v5 chips are from one multi-project waver.

The programmable dead time shown in figure 4 also is in the expected range and has a good channel-to-channel uniformity. The same is true for other parameters like run-down current and integration gate width. [5]

2.3 Solved Issues from Previous Versions

Most of the issues found in the legacy ASD and earlier prototypes of the ASD2 have been solved. The LVDS output levels, that showed sometimes illegal states in the legacy chip, are

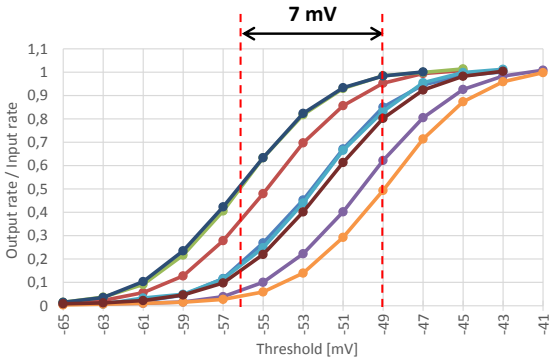

Figure 3: The threshold scan shows a channel-to-channel variation of 7 mV. This was the worst ASD2v5 chip measured, the best one has a spread of only 3 mV.

Figure 4: Excellent channel-to-channel uniformity of the programmable dead time setting. A range of 50–850 ns in steps of $\approx$ 110 ns is covered.

completely stable now. A feedback from the digital part to the sensitive preamplifier has been removed by separating the substrates of the analog and digital circuit by a high resistive path (called BFMOAT, a trench of low-conductivity BF_2^+) and guard rings. Also a bug concerning the programming of the parameter settings has been addressed. [6]

2.4 Tracking Performance with Cosmic Muons and at a High-Energy Test Beam

A set of ASD2v5 chips was mounted on a front-end mezzanine board and attached to an sMDT chamber with 15 mm ϕ tubes. Drift time spectra have been recorded and show the same distribution like in the legacy chip. Although most muons with p < 2 GeV were removed by a layer of lead, multiple scattering is still too high for spatial resolution studies. Therefore, the setup was taken to a high energy muon test beam at the gamma irradiation facility (GIF++) at CERN. There the spatial resolution versus the γ conversion rate was measured. Figure 5 shows a slightly better resolution for the ASD2v5 compared to the legacy chip. The main contributor is the faster peaking time. The results prove that the new chip can safely work under ATLAS phase-II conditions. [6]

3. Conclusions and Outlook

The current ASD2v5 prototype chip shows a good performance in both the laboratory and experimental setup. It could already be used as a replacement for the legacy ASD chips installed in ATLAS based on measurement and simulation results. A new, improved ASD2v6 has been submitted and is being manufactured. Mass production is scheduled to begin in 2018.

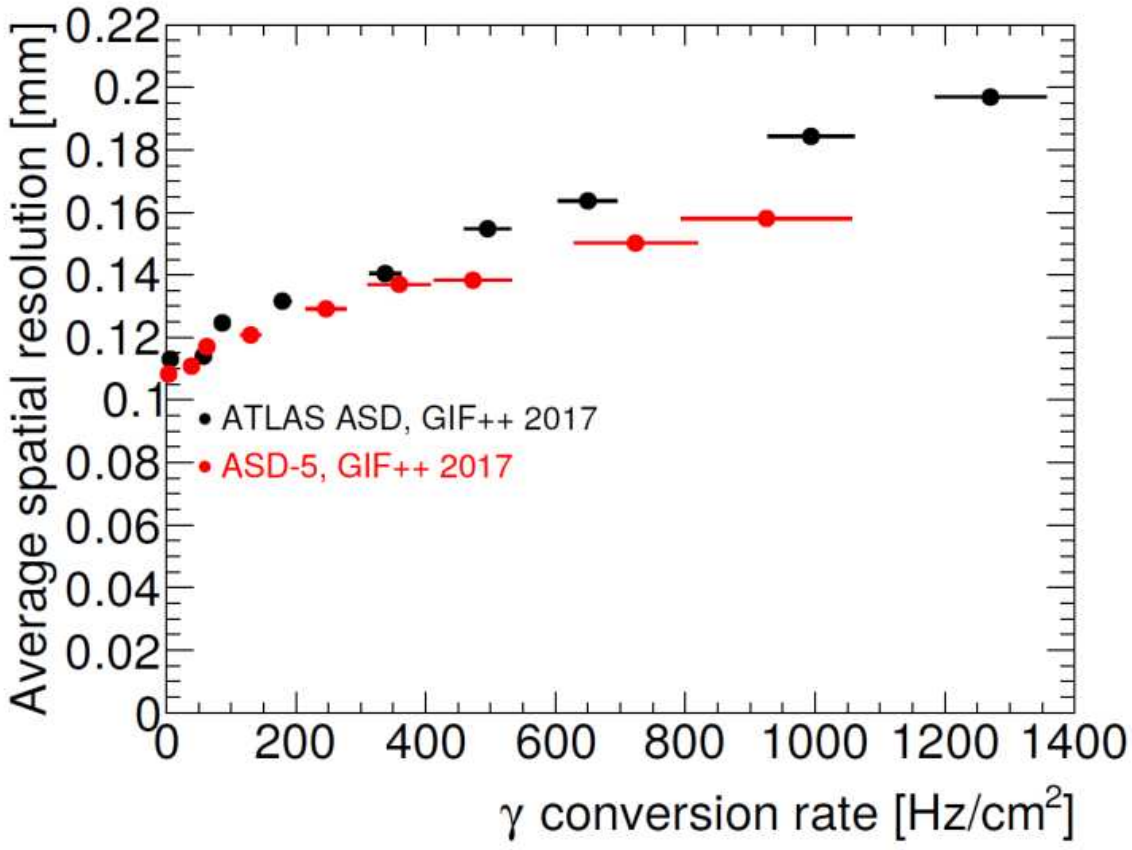

Figure 5: Comparison of the spatial resolution of the ASD2v5 (red) and the legacy ASD (black). The new chip shows slightly better values.

References

[1] H. Kroha et al., *Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC*, 2015 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)

[2] Christoph Posch, Eric Hazen, John Oliver, *MDT-ASD User's Manual*, ATL-MUON-2002-003, September 2007

[3] M. De Matteis et al., *Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC*, Journal of Instrumentation 11.02 (2016): C02087

[4] M. De Matteis et al., *An Eight-Channels 0.13-μm-CMOS Front End for ATLAS Muon-Drift-Tubes Detectors*, IEEE Sensors Journal 17.11: 3406-3415

[5] Sergey Abovyan, *Setup for automated testing/measurement of ASD2v5 performance*, Preliminary Design Review, 05 September 2017

[6] Robert Richter, *Status of the ASD preamp for MDT R/O in Phase-II*, Preliminary Design Review, 05 September 2017