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Quad Module Hybrid Development for the ATLAS Pixel Layer Upgrade

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A quad chip module hybrid assembled with FE-I4B chips has been fabricated to test performance in a serially powered module chain as would be used in the upgraded ATLAS pixel layer at the High Luminosity LHC. This poster present results of the development of a flex circuit board interface for the quad chip modules and system integration tests of modules installed on an I-beam. Experience from these hybrid assemblies will inform the design of a flex hybrid for the new large format readout chip, RD53A, which will be produced in 2017 by the RD53 collaboration.

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1. Introduction

RD53[1], a cross-experiment collaboration between ATLAS[2] and CMS[3], is developing pixel readout chips in 65 nm technology to meet the requirements of the High Luminosity LHC environment. The ATLAS Phase 2 upgrade will replace the Inner Detector with a new all-silicon tracker known as the Inner Tracker. A demonstrator chip, RD53A, will be fabricated with three analog front end variations for design evaluation. Hybrid pixel detector modules combining RD53A with bump bonded silicon sensors will allow verification of hit detection efficiency, charge resolution, low noise, high hit and trigger rates, and radiation tolerance. Serial power of modules using on-chip Shunt-LDO regulators will be explored as a low mass power distribution system.

Before the arrival of the RD53A chip, the current readout technology in use in the Pixel Detector (the FE-I4B chip[4]) has served as a stand in for testing preparation. The development of FE-I4B quad modules has provided experience with hybrid circuit board design, module handling, flex cable connections near fragile wire bonds, and serial power distribution in which the return voltage for one module becomes the input voltage for the neighboring module. From this experience a similar hybrid circuit board has been designed and manufactured to be implemented in single RD53A chip modules. Measurements done with such hybrid modules will inform the design of a final Pixel chip to be implemented in the new Inner Tracker.

2. FE-I4B Quad Module Hybrid Design

The hybrid printed circuit board provides an interface for the quad module to the outside world. The PCB is a 2-layer board of FR4 material with 15 mil thickness. The data, power and high voltage are transmitted and received through a flex cable connector in the center of the board. Power is distributed in parallel to all front ends on one module. Solder pads for voltage and voltage return allow the ground for one module to become the input for a neighboring module in a serial chain. External resistors are added to set the reference current for the Shunt-LDO regulators (two per chip). Clock and command are distributed in parallel to all front ends on one module with low voltage differential signal (LVDS) pairs. Clock and command signals are terminated on the PCB. Each front end has a dedicated data out LVDS pair. A In a serial powered chain, all modules will sit at different ground levels than the data acquisition system. AC-coupling of data signals is required to interface between different logic levels. AC coupling of data output signals is off-board, on the data acquisition side. A plated hole allows the high voltage sensor bias to be wire bonded down to the surface of the silicon sensor.

3. Quad Module Assembly

Two "dummy" quad modules (modules without a bump bonded connection to a silicon sensor) were assembled by arranging four FE-I4B chips on a vacuum chuck and applying epoxy to their surfaces. A piece of silicon was adhered on top, followed by the hybrid PCB. The chips were then wire bonded to the hybrid. Three previously assembled modules with bump bonded sensors needed only the hybrid PCB to be glued with epoxy and wire bonded. Figure 1 shows a side view of a hybrid quad module and Figure 2 shows the assembly procedure for the dummy modules.

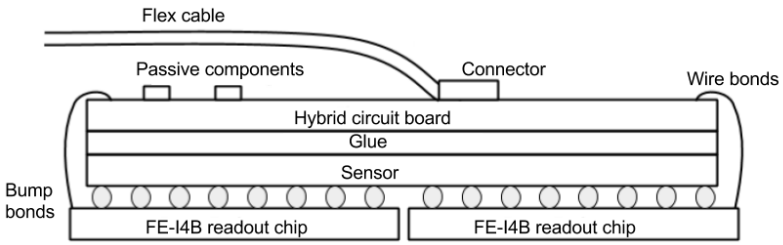

Figure 1: Side view of a hybrid quad module. The readout chips are bump bonded to a silicon sensor. This sensor is glued to the hybrid circuit board. The readout chips are wirebonded to the hybrid circuit board. A flex cable transmits data between a DAQ system and the module.

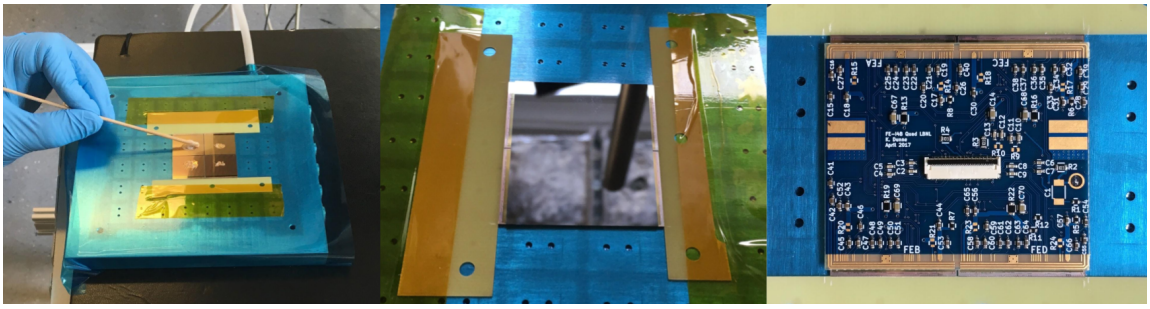

Figure 2: Assembly of a dummy FE-I4B quad module. (Left) Epoxy is applied to four FE-I4B chips arranged in quad module layout on a vacuum chuck. (Center) A piece of silicon is applied on top of the epoxy. (Right) The hybrid circuit board is epoxied on top of the silicon.

4. Characterization

The five quad modules were characterized to verify the performance of the hybrid PCB. Using the YARR readout software[5], modules underwent tests for noise, Shunt-LDO operation, and a self trigger scan with an Ami^{241} source to verify bump bonded pixels could pick up particle hits. Figure 3 shows self trigger scan results for one quad module overlaid upon an image of the hybrid PCB to show affects from components. The module was irradiated with the source for 19 hours. The z axis shows the accumulated number of hits over that time period. The effects seen on the inner edges are from unconnected pixels.

Figure 4 shows the effect of the analog shunt circuit in each chip in one quad module. The change in current from an unconfigured state to a configured state is shown for increasing analog current which is controlled by a setting within the preamplifier bias register. Front ends A,B, and D have wire bonds which activate the shunt circuit. The shunt burns off current that is in excess of a reference current. Front end C did not have the analog shunt wire bond set.

5. RD53A Single Chip Hybrid Design

Experience from the FE-I4B hybrid interface informed the development of a similar PCB to be used in a RD53A single chip module. The RD53A hybrid PCB is a 2-layer board with 10 mil thickness and uses many design features of the FE-I4B board such as solder pads for serial power of single chips. The RD53A chip will receive control signals through one data pair with the clock

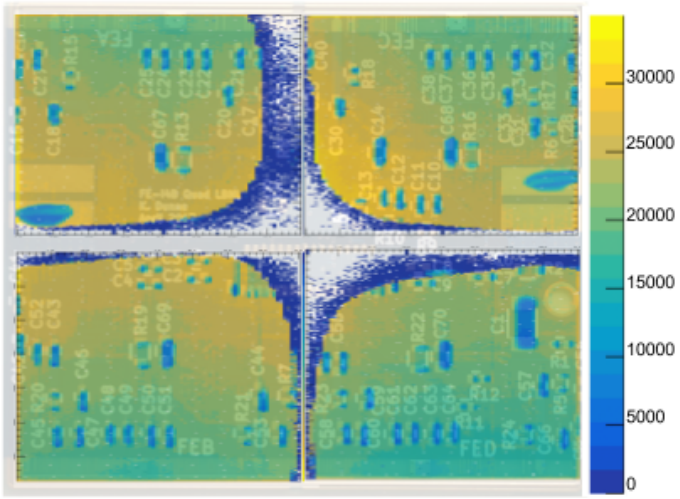

Figure 3: Self-Trigger scan results from Am^{241} source. Z axis gives accumulated hits over 19 hours. Overlaid onto board geometry to show shadow regions from components. Effect on inner edges is from unnconnected pixels.

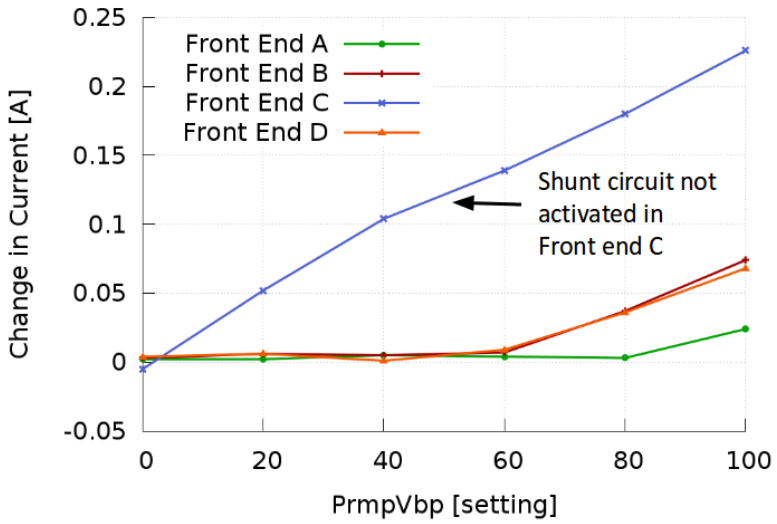

Figure 4: Current fluctuation measured before configuration and after configuration for each front end chip on one module.

recovered on-chip. In addition to a single data pair for command, the interface board is designed with a data pair for an externally supplied clock and four output data pairs which transmit at 1.28 Gbps each, for a total of 5.12 Gbps.

Figure 5 shows the layout of four RD53A single chip hybrid PCBs. The boards are manufactured with copper traces connecting them boards in parallel. This is in effect a 1x4 quad module of single chips. In this case, command is sent individually to each chip unlike the FE-I4B hybrid board in which the chips are controlled in parallel. In the 1x4 quad, power is distributed in traces that can be severed when single boards are cut part.

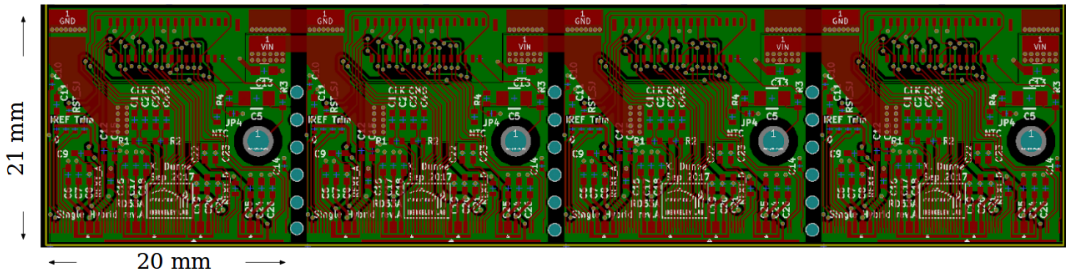

Figure 5: CAD layout of four single RD53A chip hybrid circuit boards. The boards are manufactured with power distributed in parallel between them which creates a 1x4 quad module. Single boards can be cut apart, severing the parallel connection.

6. Conclusion

A hybrid printed circuit board to interface with a quad module assembly of FE-I4B chips has been designed, manufactured, and tested. This board will facilitate tests of serially powered quad modules. Experience from this design was applied to the development of a similar interface for single RD53A chip modules which will be implemented on the arrival of the RD53A chip.

7. Acknowledgments

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