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FIRST PROTOTYPE INDUCTIVE ADDER FOR THE FCC INJECTION

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Abstract

A highly reliable kicker system is required as part of the injection for the FCC. A significant weak point of conventional kicker systems is often the pulse generator, where a Pulse Forming Network/Line (PFN/PFL) is discharged through a thyratron switch to generate the current pulse for the kicker magnet. This design has several disadvantages: in particular the occasional erratic turn-on of the switch which cannot be accepted for the FCC. A potential replacement is the inductive adder (IA) that uses semiconductor switches and distributed capacitors as energy storage. The modular design, low maintenance and high flexibility make the IA a very interesting alternative. In addition, the ability to both turn-on and off the current also permits the replacement of the PFN/PFL by capacitors. A first FCC prototype IA, capable of generating 9 kV and 2.4 kA pulses, has been designed and built at CERN. It will be upgraded to a full-scale prototype (16 kV, 2.4 kA) in mid-2018. This paper presents measurement results from the 9 kV prototype and outlines the conceptual changes and expected performance of the 16 kV prototype.

INDUCTIVE ADDER

Switching technologies for kicker magnet pulse generators is a challenging topic of research. Solid State switches have developed strongly during the past decade. Especially wide-band-gap devices such as SiC MOSFETs show very promising switching characteristics and have the potential to replace thyratrons from their well-established place in some applications. However, in terms of voltage and current rating, SiC MOSFETs still have substantially lower values than thyratrons. Power modulators such as the inductive adder (IA) [1] or Marx generator [2] are able to generate high voltage (HV) and current pulses with of-the-shelf components. The IA is a stack of 1:1 pulse transformers, with the secondary windings connected in series. To obtain a high output current each primary layer consists of multiple parallel branches: each branch contains a fast, high voltage, MOSFET to electrically connect or disconnect a precharged pulse capacitor in parallel with the primary of the transformer. The charging voltage of the pulse capacitor defines the layer voltage and the sum of all layer voltages gives, approximately, the output voltage of the IA. An electrical schematic of the IA can be found in [3].

PULSE REQUIREMENTS AND DESIGN PARAMETERS

The main parameters which influence the design of an IA are output voltage and current, pulse length, system impedance, pulse rise and fall time as well as the flattop ripple. The requirements for the injection kicker system of the FCC are described in [3] and [4]. During the last year the specified field rise time increased to 430 ns. The rise time of the current pulse of the generator is unchanged and is 75 ns. To obtain a field flat top length of 2 μs, the pulse generator must be capable of generating an electric pulse with a flattop duration of 2.35 μs.

To feed a current of 2.4 kA into a magnet of 6.25 Ω characteristic impedance [5], requires an output voltage of 15.0 kV. The preliminary design parameters for the IA, published in [4], are still correct except for the number of constant voltage layers, which will be reduced to twenty [6].

PCB DESIGN AND GATE DRIVER

A layer of the FCC injection IA consists of twelve PCBs, one of which is shown in Fig. 1: there are two branches per PCB. The PCBs are connected together with pins on the sides of the board: high voltage and low voltage are distributed from PCB to PCB and only one connection, to each power supply, is required per layer. To avoid matching and timing problems, while distributing the trigger signal, the signal is

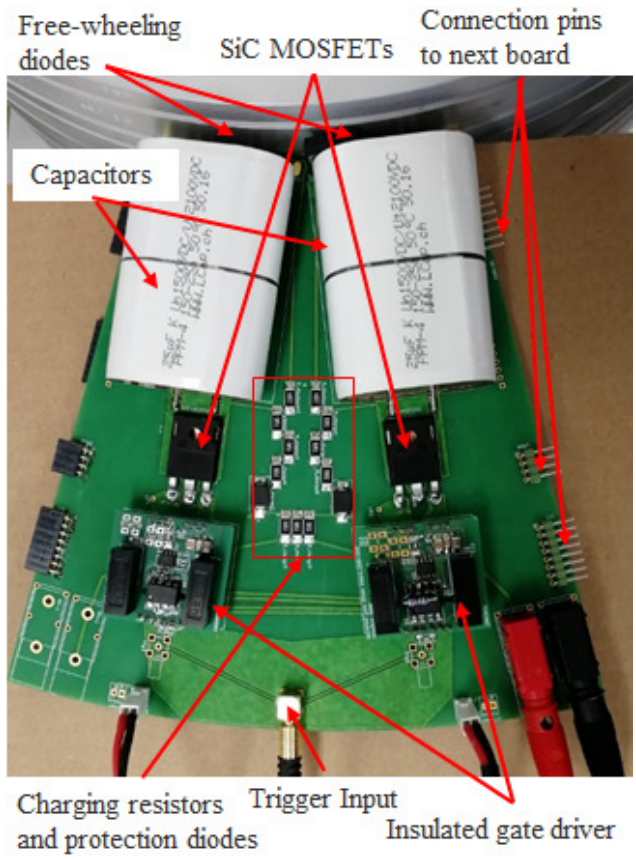

Figure 1: One FCC injection IA PCB with two branches: up to twelve PCBs per layer can be used.

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directly connected to each PCB. Hence the trigger is split and distributed on its own cable: each cable is terminated in 50 Ω.

The pulse capacitor of each branch is charged through a HV diode and charging resistors. The diode avoids discharging of all parallel connected branches if one switch of the layer fails to short circuit. A high value (2.2 MΩ) discharge resistor ensures a safe discharge of the pulse capacitor once the HV dc supply is switched off. Free wheeling diodes are located in parallel with each primary layer: these diodes conduct magnetizing current of the core when the MOSFETs of a layer are turned off. Additionally the diodes bypass the layer if it fails to trigger when other layers turn-on, ensuring that the IA provides a significant portion of the output pulse.

Two separate, smaller, PCBs include a gate driver circuit: these cards are plugged into each main PCB. The trigger signal on the gate driver PCB is galvanically isolated from the MOSFET with a digital insulator [7]: the digital insulator is chosen to ensure low jitter triggering. The gate driver is capable of delivering 14 A, to ensure fast turn-on of the MOSFET. To realize a negative gate voltage for switch off, as is recommended by several manufacturers for SiC MOSFETs [8, 9], the ground pin of the gate driver is connected to a negative low voltage power supply. Hence the MOSFET gate-source is actively driven between the positive and negative values.

Positive and negative supply voltages of the gate driver are connected with voltage regulators, which ensures several kV of isolation. Hence, in case of a gate failing to a short circuit to either drain or source, the high voltage is limited to the gate driver board of one branch of one layer. The PCB is designed so that any TO-247 package of MOSFET, can be used. For the FCC injection prototype a SiC MOSFET with 1200 V rated voltage and 250 A rated pulse current is used. The pulse capacitor [10] is custom made with a value of 25 μF and a rated voltage of 1500 V: the average leakage inductance of the capacitors is 28 nH: testing of sample components was documented in [4]. All components are located on the PCB as close as possible to the transformer core to minimize the parasitic inductance of the primary circuit: in addition, the parallel connection of 24 branches (12 PCBs) further reduces the parasitic inductance.

LAYER DESIGN FOR FAST RISE TIME

A fast rise time at the IA output requires a short pulse propagation time through the IA stack and fast semiconductor switches in the primary circuits. Hence, in general, the inductance of the primary circuit and the secondary circuit should be as small as possible. A strong contributor to the pulse propagation time is the height of the IA stack. If the secondary is short circuited at one end of the IA and connected to a terminated load at the other end, which is usually the case, the pulse has to propagate each layer twice [11]. The total propagation delay (t_{prop}) can be estimated as:

$$t_{\mathrm{prop}} = 2N \cdot \sqrt{(L_{\mathrm{prim}} + L_{\mathrm{ss}}) \cdot C_{\mathrm{ss}}} \qquad (1)$$

Where N is the number of layers in the IA, L_{prim} is the effective primary inductance per layer and L_{ss} and C_{ss} are the inductance and capacitance formed by the coaxial structure of the primary and secondary windings, per layer. L_{ss} and C_{ss} can be estimated from the coaxial geometry [6]. Expressing t_{prop} with the stack design parameters leads to:

$$t_{\mathrm{prop}} = 2N \cdot \sqrt{L_{\mathrm{prim}} \cdot \frac{2\pi\epsilon h}{\ln \frac{d_{\mathrm{o}}}{d_{\mathrm{i}}}} + \mu\epsilon h^2} \qquad (2)$$

Where ϵ is the permittivity of the insulation material, h the layer height, d_{o} the outer diameter of the insulation material between the primary and secondary, d_{i} the inner diameter of the insulation material and μ the permeability of the insulation material. Since several parameters in Eq. (2) are preselected to match the impedance of the IA, as described in [4], only the layer height h can be modified to reduce the propagation delay and hence its influence upon the rise time: however, the layer height is a strong influence. Main components limiting the reduction of the layer height are the height of the magnetic core, required to efficiently achieve the cross-sectional area, and the height of the pulse capacitor. For the FCC injection IA prototype, a layer height of 4 cm was chosen which leads to a two way propagation time of 37.67 ns for the 20-layer stack, which is half of the required 75 ns pulse rise time, and leaves ~37 ns for the rise time of the current of each layer.

STATUS OF PROTOTYPE

The start of the assembly of the 10-layer prototype can be seen in Fig. 2. Each layer of the stack consists of one tape wound, nanocrystalline, magnetic core with a height of 3 cm. Insulation between the core and aluminum housing ensure that the housing does not create a short circuit between turns

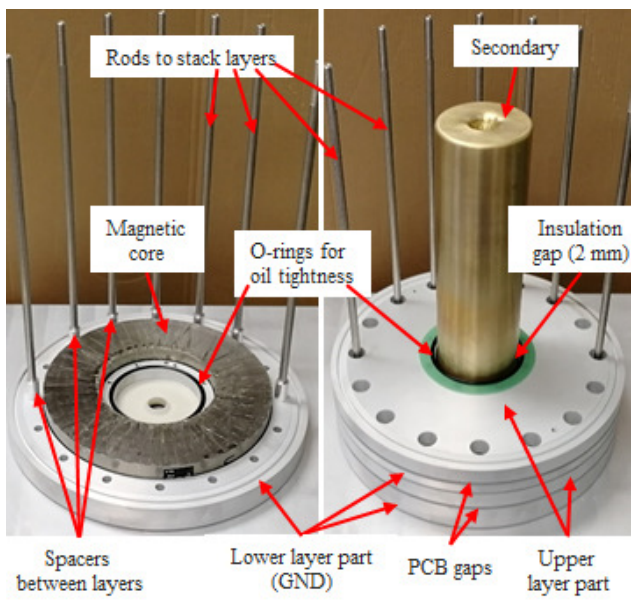

Figure 2: Assembly steps of the 10-layer IA prototype.

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of the tape. To serve as the primary winding the upper and lower part of the aluminum housing must be in good electrical contact at the inside of the housing. There is a gap between the upper and lower housing around their outer circumference: good RF contact between the housing and PCBs is ensured by using canted coil springs [12]. The lower aluminum housing of each layer is at ground potential and the lower housings are electrically interconnected by conducting spacers indicated in Fig. 2.

The secondary is placed through the middle of all layers (Fig. 2): there is a 2 mm insulation gap to the aluminum housings of the primary windings. For high voltage and impedance reasons this gap will be filled with oil. A rubber O-ring is used between adjacent layers, as well as between the two housings of a layer (Fig. 2) to ensure oil-tightness. However, for the initial tests the insulation gap was not yet filled with oil. In addition, high and low voltage supply was distributed with jump wires from layer to layer.

In Fig. 3 the fully assembled 10-layer stack is shown. Each layer is equipped with one PCB of two parallel branches. The trigger signal, coming from a pulse generator with synchronized outputs [13], is distributed so as to trigger each PCB simultaneously.

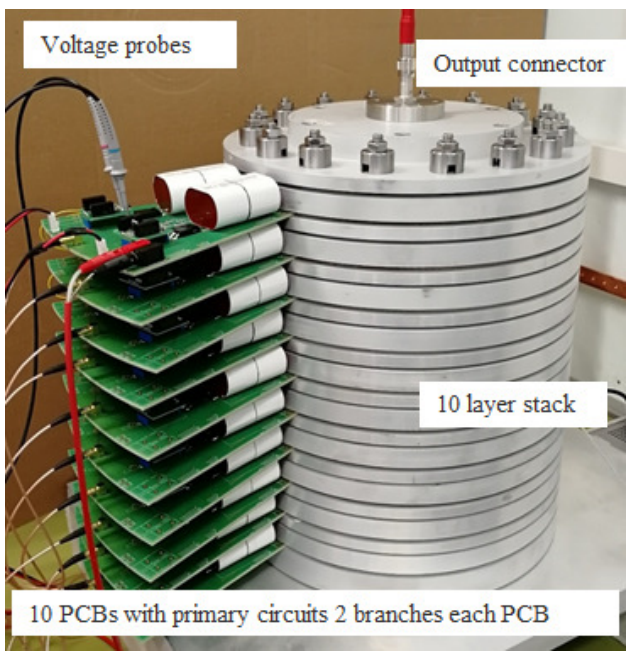

Figure 3: Assembled 10 layer prototype with one PCB of two branches each per layer.

MEASUREMENTS

Initially, while awaiting the delivery of the mechanical parts required for the FCC injection IA stack, the PCBs have been tested with an existing 5-layer IA stack, not specifically designed for the FCC. The output of the stack was connected to a 50 Ω load resistor. During these measurements the layer voltage was increased up to 1 kV to give a pulse output voltage of 5 kV and a current of up to 100 A (Fig. 4) which corresponds to up to 50 A per MOSFET. The measured rise time of the output voltage, across the load, from 0.5 to 99.5 % was ~40 ns, which is very close to the required value.

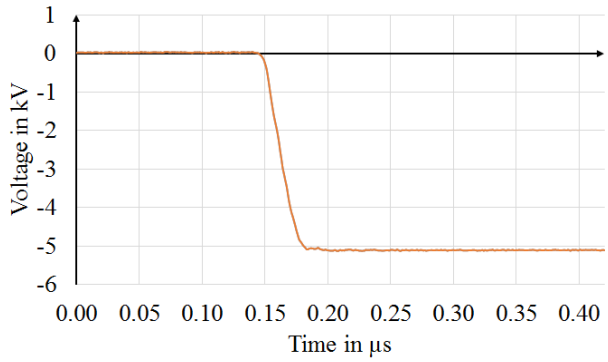

Figure 4: Measured output pulse of a 5-layer prototype.

Subsequently the PCBs were assembled in the 10-layer prototype. Figure 5 shows the 10-layer test setup with one PCB mounted in each layer. The trigger signal, gate driver output, drain-source voltage and output voltage of the stack have been measured with an oscilloscope. By driving each layer at ~400 V an output pulse voltage of 4 kV was generated across the 50 Ω load. The measured rise time was ~50 ns. Further measurements with higher voltages are pending.

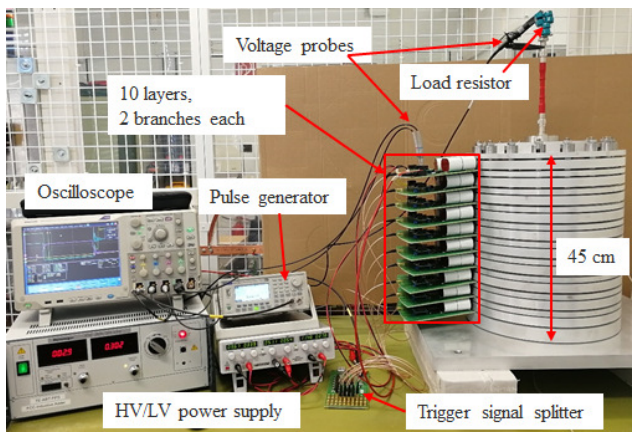

Figure 5: Test setup for the 10-layer prototype with oscilloscope, power supplies and trigger system.

CONCLUSION

A first 10-layer prototype IA for the FCC injection kicker system has been assembled. The design for the PCBs, of the prototype IA, is completed and the PCBs were tested in two different stacks up to a voltage of 1 kV per layer. Initial rise time measurements on both the 5-layer and 10-layer stacks are very promising. The fully equipped prototype with 24 branches per layer and better impedance matching is expected to have an improved performance.

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