Radiation-induced Effects on Data Integrity and Link Stability of the RD53A Pixel Readout Chip

M. Vogt[a,1] **on behalf of the RD53 collaboration**

[a]*University of Bonn,*
Nussallee 12, 53115 Bonn, Germany

E-mail: vogt@physik.uni-bonn.de

Abstract: The phase-2 upgrade of the LHC will require novel pixel readout chips, which deliver hit information at drastically increased data rates and tolerate unprecedented radiation levels. The large-scale prototype chip RD53A has been designed by the RD53 collaboration and manufactured in a 65 nm CMOS process, suitable for the innermost layers of both the ATLAS and the CMS experiment. In order to verify the radiation hardness design goal of 500 Mrad total ionizing dose, RD53A has been irradiated using X-rays. The radiation effects on the performance of the data link, reset circuit and the clock generation have been investigated. Furthermore, the operating margins in terms of supply voltage and frequency have been analyzed.

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[1]Corresponding author.

Contents

1 Introduction

The phase-2 upgrade of the Large Hadron Collider (LHC) [1] will substantially increase the instantaneous luminosity by a factor of at least 5. This requires novel pixel readout chips with highly complex digital architectures, which deliver hit information at drastically increased data rates. Unprecedented radiation tolerance is essential, especially close to the interaction point. The RD53 collaboration [2] was formed to approach these challenges by designing a prototype pixel readout chip in a 65 nm CMOS technology, which is suitable for the innermost layers of the pixel detector in the ATLAS [3] and CMS [4] experiments.

The large scale prototype chip RD53A [5] has been produced and is available since December 2017. The stability and locking behavior of the high speed Aurora links of non-irradiated RD53A chips have been investigated in lab environments with different cables, powering schemes, Command Data Recovery (CDR) configurations and synchronization patterns. Performance characterization measurements of the output drivers are ongoing. The readout system BDAQ53 [6] has been developed [7] to perform characterization- and test beam measurements. It consists of an FPGA-based readout board and a Python-based data acquisition and analysis framework.

In order to understand the degradation of the clocking- and communication periphery of RD53A, dedicated irradiation campaigns are necessary. Various test routines monitored the chip performance during the irradiation. Based on the results, methods to improve the operating parameters and design changes for the upcoming RD53B chip submission will be evaluated.

2   The RD53A pixel readout chip

RD53A combines three different analog front end designs and two memory architectures, which are currently being reviewed, to select one of each for the second prototype chip RD53B. A new design concept was used for the pixel matrix: It is divided into 8x8 pixel cores, which are assembled from 2x2 pixel analog quads, embedded in synthesized digital logic. A pixel core can be simulated on transistor-level. All pixel cores are identical, which allows for efficient hierarchical verification [8].

3   Total Ionizing Dose effects

One of the most important Total Ionizing Dose (TID) surface damage mechanisms of MOS transistors is charge trapping, which takes place in the thin field oxide between the bulk substrate and the polysilicon layer. Thereby, transistors can alter their threshold voltage and transconductance, which leads to speed degradation and increased jitter in digital circuits. Modern 65 nm CMOS processes have been evaluated [9] and show relatively high intrinsic radiation tolerance [10], which makes them suitable for high radiation environments. However, especially narrow transistors suffer from additional TID effects like increased leakage current.

4   TID campaign

In the inner layers of the new pixel detector for the High Luminosity LHC, a total ionizing dose of up to 1 Grad is expected, including a safety factor. The pixel detector however will be replaced after 500 Mrad and the readout chip is designed to meet this specification. The radiation damage by TID is a cumulative effect and thus, accelerated high dose-rate campaigns are a common method to evaluate the radiation hardness of semiconductor devices. However, lower dose rate exposure, as present in the experiment, may yield different results. Dedicated irradiation studies are inevitable.

The transistor performance in the 65 nm process used for RD53A, was investigated up to 1 Grad [10]. Radiation effects on different digital standard cells in 65 nm have been investigated with simulations and measurements using the dedicated test chip DRAD [11]. The 500 Mrad radiation models developed within RD53 collaboration overestimate the TID damage level, because they assume worst-case bias conditions at room temperature and don't consider annealing effects. Further TID studies with RD53A are necessary to test the simulation predictions.

4.1   Setup and methodology

The irradiation campaign was carried out using a new X-ray facility in Bonn (figure 1). The tungsten target tube was operated at an acceleration voltage of 40 kV. During the irradiation, the chip was cooled to −5 °C in dry N_2 atmosphere and operated with a monitor script, which included digital scans, temperature and power consumption measurements.

In order to observe effects of charge trapping, it is important to create realistic biasing conditions. To ensure this, all three front ends of the pixel matrix were active and clocked during the irradiation. Due to problems with the initial dosimetry, the actual dose was lower than expected. Instead of the anticipated dose of 600 Mrad, only ~370 Mrad were achieved. This total ionizing dose was reached in multiple steps with dose rates of 2.8 Mrad/h for the first 12 Mrad and 3.7 Mrad/h for the rest of
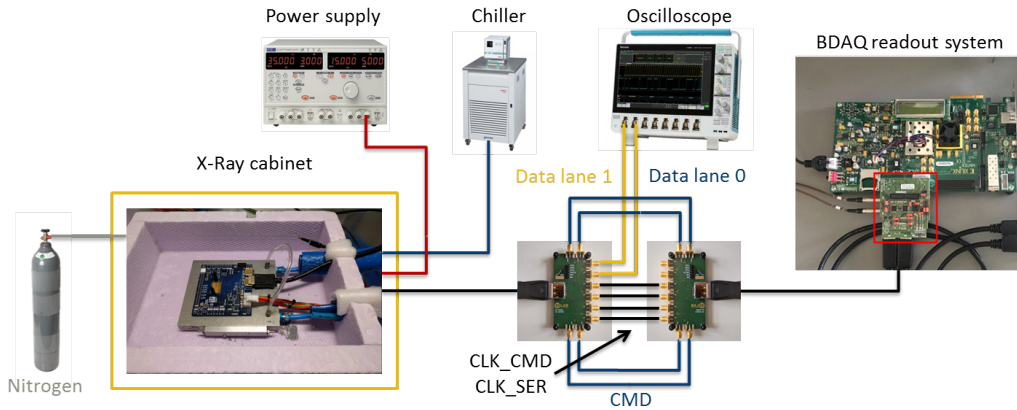
Figure 1: X-ray irradiation setup.

the campaign. At each TID step, time consuming and detailed measurements like full shmoo scans (section 4.4) and eye diagrams were performed.

The final pixel readout chips will be operated at 1.2 V and a nominal system clock frequency of 160 MHz. During this campaign, RD53A was operated at an extended range of digital supply voltage, $V_{DDD} = 0.8 - 1.3$ V and input clock frequency, $f_{CMD} = 140 - 180$ MHz, in order to determine the operating margin before and after irradiation. At each combination within this parameter space, tests were performed to evaluate the reliability of operation. In order to disentangle the radiation effects on the digital logic and the clock recovery circuit (section 4.3), the chip was operated in the so called CDR-bypass mode. This allows to externally supply two reference clocks, which normally are generated by the chip. The readout system BDAQ53 allows to operate RD53A in this mode by providing two variable frequency clocks with fixed phase relation: The previously mentioned f_{CMD} and a second, faster clock f_{SER}, for the output data links.

4.2 Reference current

One of the crucial requirements for RD53A is a stable master reference current of 4 µA. As depicted in figure 2a, it is derived from a bandgap voltage source, followed by a voltage-to-current converter and a current mirror. Two resistors in series, $R1$ and $R2$, define the conversion factor. A 4-bit DAC can be used to trim the current and thereby compensate for process variations.

During the campaign, I_{REF} was measured between the irradiation steps (figure 2b). The current degradation is significant for the first 6 Mrad and becomes linear above ~ 120Mrad. After 370 Mrad, I_{REF} has decreased by 7.5% of the initial value. The reason for this behavior is still subject of investigation. One possible explanation lies in the design of the feedback resistors. In order to achieve high temperature stability, a combination of two different resistor implementations was used. The temperature coefficients of polysilicon and diffusion resistors partially compensate due to their opposite sign. The radiation sensitivity, especially of the diffusion resistor, is suspected to be responsible for the high reference current shift.

This behavior was observed during multiple different X-ray TID campaigns within the collaboration as well. Consequently, RD53B will use external high precision metal film resistors instead, to reduce the probability of radiation-induced reference current changes.
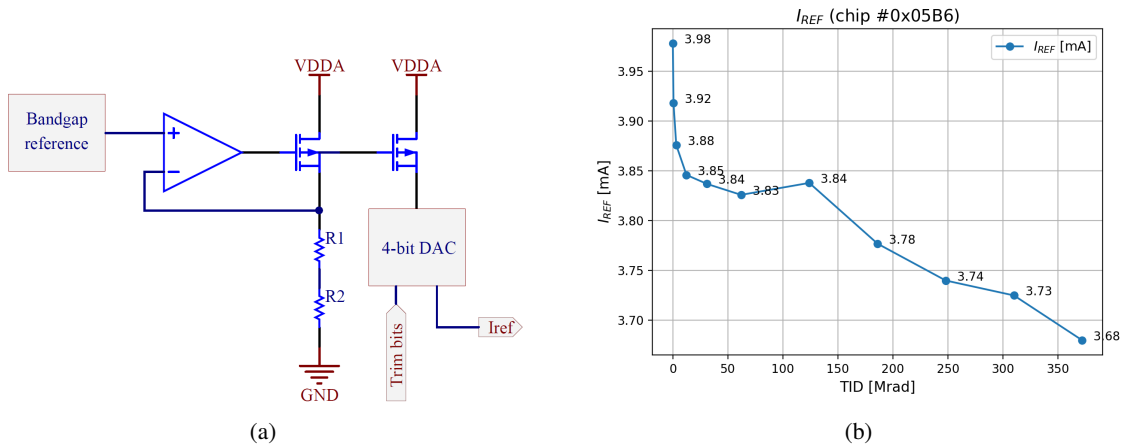
Figure 2: a) Schematic of the reference current source. b) I_{REF} as a function of the TID.

4.3 CDR and CML output drivers

In the default operation mode, the CDR block recovers the reference clock of nominally 160 MHz from the received command data stream (figure 3a). The CDR includes a Voltage Controllable Oscillator (VCO) and generates a high frequency clock, which is phase-locked to the recovered clock and used by the serializer to generate the 1.28 Gbit/s output data stream. By varying a control voltage (V_{CTRL}), the CDR tunes the VCO frequency to a nominal value of $f_{SER} = 8 \times f_{CMD} = 1.28$ GHz. The VCO tuning range of a non-irradiated chip lies between 300 MHz and 1.9 GHz.
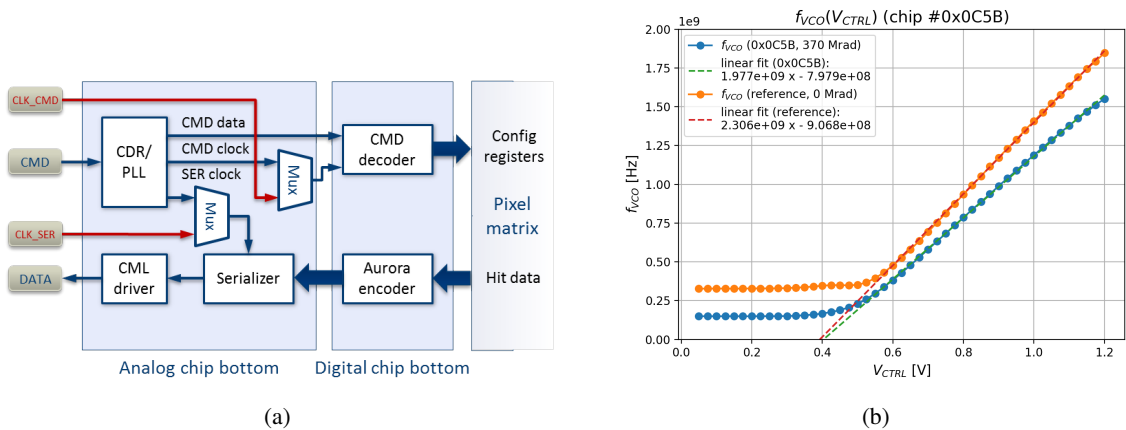

Figure 3: (a) Simplified clock generation and data flow blocks. (b) VCO gain curve measurement for a non-irradiated chip and after 370 Mrad.

The tuning range is expected to change after irradiation, as the propagation delays of the buffers in the VCO ring oscillator degrade. The VCO gain curve has been measured for a non-irradiated chip and after 370 Mrad with V_{CTRL} between 25 mV and 1.2 V (figure 3b). Compared to the non-irradiated sample, the VCO gain decreased slightly and the tuning range shifted towards lower frequencies by $\sim$ 250 MHz. The nominal value of 1.28 GHz can still be reached, thus the data link operation at 1.28 Gbit/s is unaffected. For RD53B, the VCO transistor sizes will be increased to
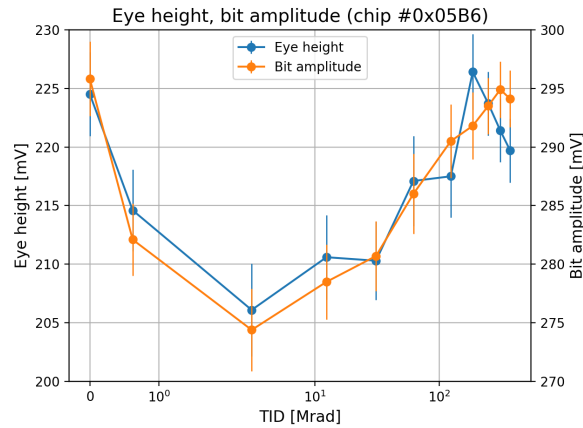
Figure 4: Eye height and bit amplitude of the CML output driver.

improve the performance and radiation hardness. The cable drivers of RD53A are implemented as Current Mode Logic (CML) buffers with programmable pre-emphasis. The bit amplitude and the eye height (figure 4) have been measured as part of the measurement routines at each irradiation step. Both eye diagram characteristics fluctuated within 10% of their initial value during the irradiation.

4.4   Digital injection scans

A common method to visualize the response of integrated circuits to varying operating conditions is the *shmoo plot* (figure 5). Each field represents a combination of possible conditions, in terms of supply voltage and input clock frequency. The measured response is the result of a test procedure. In case of this RD53A irradiation campaign, the test is a digital injection scan and the parameters are: $0.8\,V \leq V_{DDD} \leq 1.3\,V$ and $140\,MHz \leq f_{CMD} \leq 180\,MHz$. The analog supply voltage V_{DDA}, which does not affect the digital scans, is kept at a constant value of 1.2 V during all measurements.

For each combination of settings, the following measurement procedure is performed:

- power off the chip
- set V_{DDD} and f_{REF} to the new values
- power on, try to establish communication (up to 3 times)
- run a digital scan with 100 injections per pixel

The different colors in figure 5 represent the results of the digital scans, which inject 100 times per pixel into the digital hit processing chain. For the full matrix, this leads to an expected integrated occupancy of 7.68×10^6 hits. For the extreme cases in the lower left corner of the plots, where the chip is operated at low voltages and high frequencies, no communication can be established - represented by gray colored entries. At higher voltages still below the nominal value of 1.2 V, for some combinations the link can be established, but the injections are either not registered at all or they are not fully processed. Those cases are represented by red and yellow entries, respectively. The remaining green entries depict the combinations, which yield the expected occupancy.

4.5   Power On Reset

The digital logic of RD53A is designed to operate with V_{DDD} down to 0.9 V at the default reference clock frequency of 160 MHz. However, after 124 Mrad, the chip could not be reset reliably at this
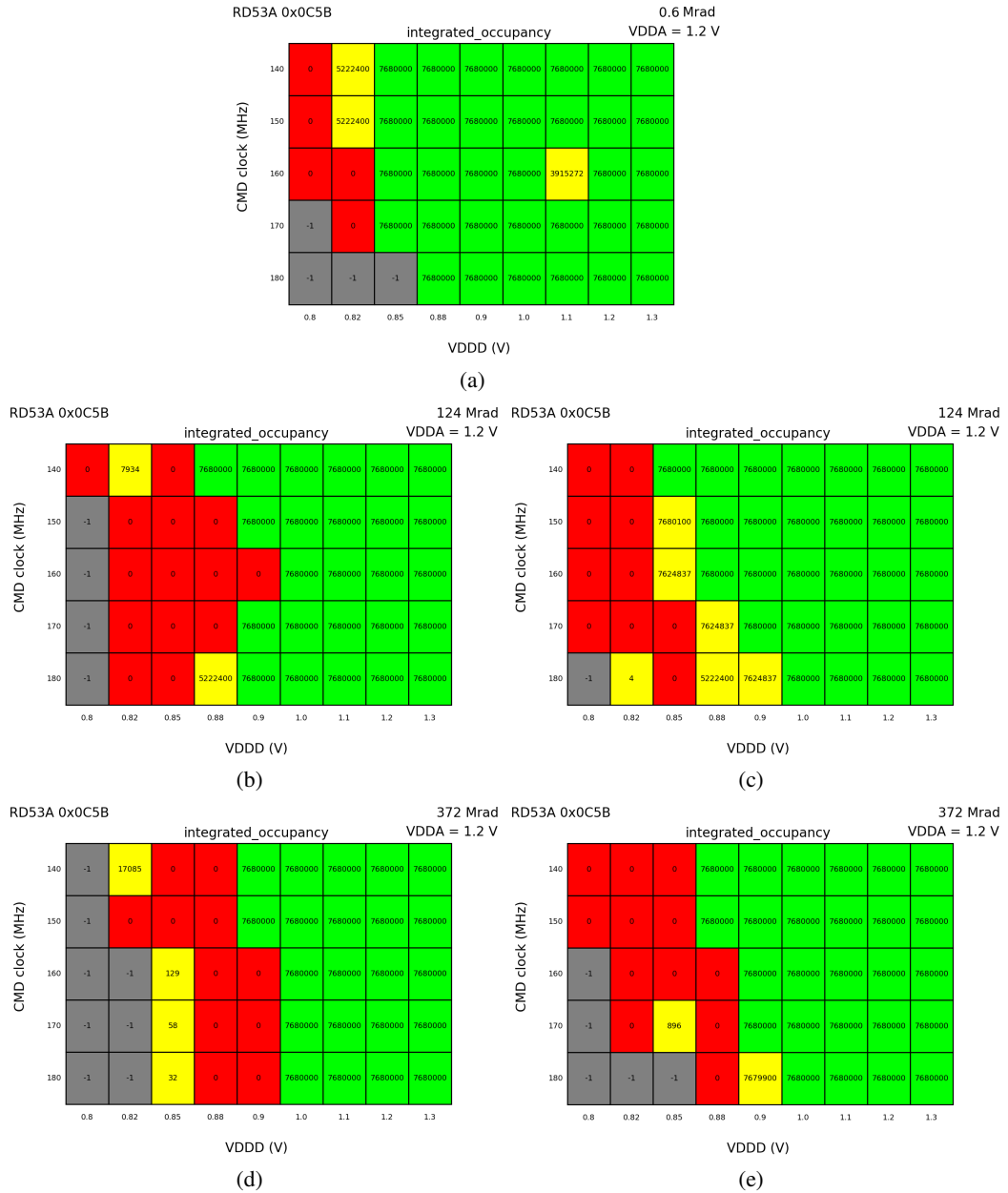
Figure 5: Shmoo plots for 0.6, 124 and 370 Mrad. a), b) and d) show the POR behavior at V_{DDD}, c) and e) represent POR at 1.2 V (described in section 4.5).

voltage. The Power On Reset (POR) was investigated as the potential source of this behavior. A different POR method was introduced with an additional scan. Compared to the procedure described in section 4.4, the initial V_{DDD} value was fixed to 1.2 V during the POR and afterwards decreased to the desired value. This ensures that the chip reset is always performed at the same voltage. As shown in figure 5c and 5e, the operating margin is increased, especially for 124 Mrad.

The simulation at $-5\,°C$ and variable V_{DDD} (figure 6) shows that the internal reset signal width decreases to a narrow pulse with reduced amplitude for $V_{DDD} \leq 1$ V, which is insufficient to perform a successful chip reset. The POR circuit was designed using the analog corner, assuming a minimum

V_{DDD} of 1.05 V. Since the operation voltage will be larger than 1.1 V during the lifetime of the readout chip, this limitation is not critical.
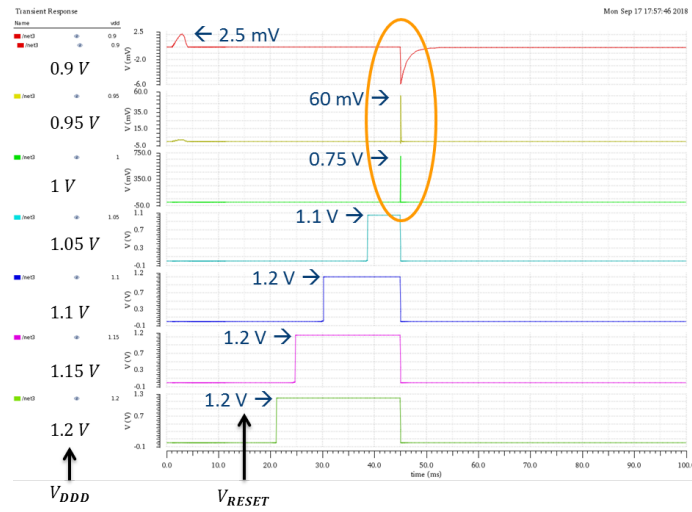

Figure 6: Simulation of the power-on reset pulse width and amplitude with varying V_{DDD}.

4.6 Command clock phase shift

In CDR-bypass mode, the phase relation between the external command clock and the command data is critical, as it is not anymore controlled by the CDR. Instead, the command data signal is sampled at the rising edge of the command clock. If this mode is used, the phase needs to be set correctly.

Measurements with an external dual-channel clock generator were performed at different temperatures after the campaign. They revealed, that the minimum hold time (distance between data transition and the next clock edge) increases by $15°$ after a TID of 370 Mrad, compared to a reference chip (figure 7). At a temperature of $-20°C$, the critical phase region width increases from $20°$ at 6 Mrad to $45°$ at 370 Mrad. The temperature dependence is $\sim 0.16°/°C = 2.9$ ps/$°C$ for both samples. Therefore, even after 370 Mrad, the timing is uncritical, as long as the readout system synchronizes the command data with the falling edge of the clock signal.

5 Conclusion and outlook

RD53A has been irradiated to 370 Mrad. No significant degradation of the CML driver and the VCO tuning range has been observed. The POR circuit is not reliable at $V_{DDD} < 1$ V after ~120 Mrad. However, this behavior is not supposed to cause issues in the default operation conditions of the experiment. The reference current showed significant radiation sensitivity and has decreased by 7.5%. This will be mitigated in RD53B, by the usage of external precision resistors.

Nevertheless, further measurements are required to gain a better understanding of radiation damages under different operating conditions, in order to find mitigation strategies for RD53B and the final pixel readout chip. For example, a low dose rate irradiation with a ^{85}Kr source is in progress, and a low dose X-ray campaign is starting soon.
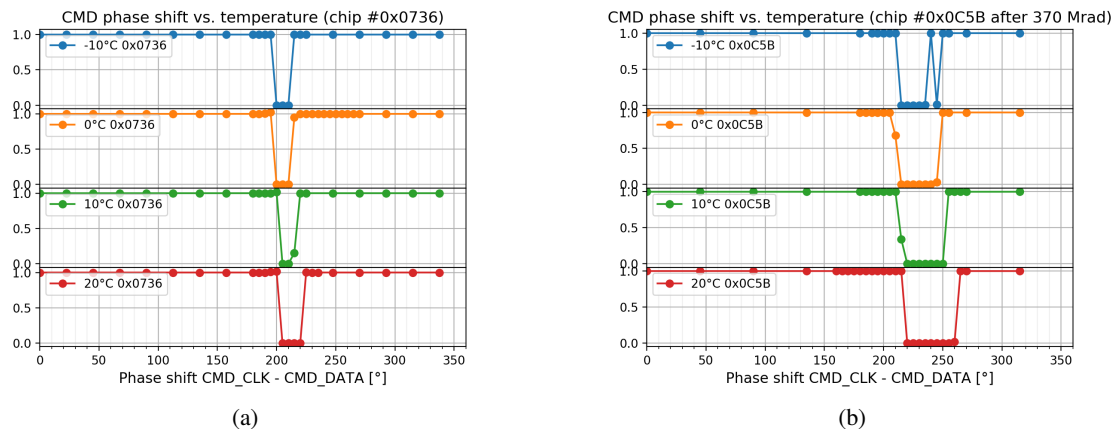
Figure 7: Phase margin of the command data signal in CDR-bypass mode

Acknowledgments

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