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Pixel detector R&D for the Compact Linear Collider

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Abstract

The physics aims at the proposed future CLIC high-energy linear e^+e^- collider pose challenging demands on the performance of the detector system. In particular the vertex and tracking detectors have to combine precision measurements with robustness against the expected high rates of beam-induced backgrounds. A spatial resolution of a few microns and a material budget down to 0.2% of a radiation length per vertex-detector layer have to be achieved together with a few nanoseconds time stamping accuracy. These requirements are addressed with innovative technologies in an ambitious detector R&D programme, comprising hardware developments as well as detailed device and Monte Carlo simulations based on TCAD, Geant4 and Allpix-Squared. Various fine pitch hybrid silicon pixel detector technologies are under investigation for the CLIC vertex detector. The CLICpix and CLICpix2 readout ASICs with 25 μm pixel pitch have been produced in a 65 nm commercial CMOS process and bump-bonded to planar active edge sensors as well as capacitively coupled to High-Voltage (HV) CMOS sensors. Monolithic silicon tracking detectors are foreseen for the large surface ($\approx 140\,\text{m}^2$) CLIC tracker. Fully monolithic prototypes are currently under development in High-Resistivity (HR) CMOS, HV-CMOS and Silicon on Insulator (SOI) technologies. The laboratory and beam tests of all recent prototypes profit from the development of the CaRIBou universal readout system. This talk presents an overview of the CLIC pixel-detector R&D programme, focusing on recent test-beam and simulation results.

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Abstract: The physics aims at the proposed future CLIC high-energy linear e^+e^- collider pose challenging demands on the performance of the detector system. In particular the vertex and tracking detectors have to combine precision measurements with robustness against the expected high rates of beam-induced backgrounds. A spatial resolution of a few microns and a material budget down to 0.2% of a radiation length per vertex-detector layer have to be achieved together with a few nanoseconds time stamping accuracy. These requirements are addressed with innovative technologies in an ambitious detector R&D programme, comprising hardware developments as well as detailed device and Monte Carlo simulations based on TCAD, Geant4 and Allpix^2. Various fine pitch hybrid silicon pixel detector technologies are under investigation for the CLIC vertex detector. The CLICpix and CLICpix2 readout ASICs with 25 µm pixel pitch have been produced in a 65 nm commercial CMOS process and bump-bonded to planar active edge sensors as well as capacitively coupled to High-Voltage (HV) CMOS sensors. Monolithic silicon tracking detectors are foreseen for the large surface ($\approx 140\,\mathrm{m}^2$) CLIC tracker. Fully monolithic prototypes are currently under development in High-Resistivity (HR) CMOS, HV-CMOS and Silicon on Insulator (SOI) technologies. The laboratory and beam tests of all recent prototypes profit from the development of the CaRIBou universal readout system. This paper presents an overview of the CLIC pixel-detector R&D programme, focusing on recent test-beam and simulation results.

Keywords: Solid state detectors, Radiation-hard detectors, Particle tracking detectors, Electronic detector readout concepts (solid-state)

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1 Introduction

The CLIC high-energy linear e^+e^- collider, under development by international collaborations hosted by CERN, is based on the novel two-beam acceleration method, operating with large gradients of 70 to $100\,\mathrm{MV\,m^{-1}}$ in a normal conducting accelerating structure. It is proposed to be operated in a staged scenario with respectively $380\,\mathrm{GeV}$, $1.5\,\mathrm{TeV}$ and $3\,\mathrm{TeV}$ centre-of-mass energy [1]. The CLIC beam is composed of trains that consist of 312 bunches separated by $500\,\mathrm{ps}$ with a $50\,\mathrm{Hz}$ train repetition rate. In the CLIC vertex and tracking detector, a high rate of incoherent pairs and $\gamma\gamma \rightarrow$ hadrons generated from beam-beam interactions.

The CLIC detector aims at performing high precision measurements of standard and beyond standard model physics. This imposes challenging performance requirements on the detectors. The vertex detector, illustrated in Figure 1, consists of barrel and disks directly surrounding the beam pipe, covers a surface of $0.84\,\mathrm{m}^2$ and is composed of pixel detectors with a pitch of $25 \times 25\,\mathrm{\mu m}^2$ for an expected single point resolution of $3\,\mathrm{\mu m}$. The Tracking detector, illustrated in Figure 2, is composed of pixelated silicon detectors with a pixel pitch of $25 \times 1000\,\mathrm{\mu m}^2$ and covering a large area of $140\,\mathrm{m}^2$. In both detectors, in order to cope with the occupancy and help with pattern recognition, a timing resolution of $5\,\mathrm{ns}$ is required. To meet the performance requirements of CLIC, the material budget allowed for each of the six layers and seven disks of the pixel detector is $0.2\,\%\,\mathrm{X_0}/\mathrm{layer}$ and 1 to $2\,\%\,\mathrm{X_0}/\mathrm{layer}$ for the five layers of the Tracker, including local support and services.

Taking advantage of the low duty cycle of the accelerator, the vertex and tracking detector are operated using power pulsing. The readout and front-end electronics is turned off when not in used, in order to reduce the power consumption to $50\,\mathrm{mW\,cm^{-2}}$ for the vertex detector and below $150\,\mathrm{mW\,cm^{-2}}$ for the Tracking detector. This reduction in power consumption allows for

the use of air cooling which reduces the need for material for active cooling in the vertexing volume. The radiation damage estimated in the vertex detector is of less than $1 \times 10^{11}\,\mathrm{n_{eq}/cm^2/year}$ and $1\,\mathrm{kGy/year}$ and is considered negligible in the Tracking detector.

Figure 1: Layout of the CLIC vertex detector. **Figure 2**: Layout of the CLIC tracking detector.

2 CLICdp tools for pixel detector prototype characterisation and simulation

The CLICdp collaboration studies the available pixel detector technologies, evaluates their tracking performance and identifies promising technologies for the construction of the CLIC tracking and vertex detectors. In order to carry out the characterization and modeling of the the prototypes realized in these technologies, a set of tools have been developed.

To extract the single-point resolution, particle detection efficiency and timing resolution of the prototypes, the Timepix3 telescope [2], [3] has been constructed. To provide a versatile platform for the development of a readout system for each of the prototypes, the CaRIBOu test system was developed [4].

Simulation tools such as technology computer-assisted design (TCAD) simulation and Monte-Carlo charge transport were employed to increase the understanding of the detector and provide feedback for the designers realizing the prototypes. The Allpix^2 framework [5] was developed to integrate the benefits of Geant4 [6], charge transport algorithm and TCAD simulations into a user friendly platform for simulation of silicon detectors.

2.1 The CLICdp Timepix3 telescope

The Timepix3 ASIC [7] is a readout designed for silicon and gaseous pixelated detectors with an array of 256×256 pixels with a pitch of $55 \times 55\,\mu\mathrm{m}^2$, providing for each detected hit a $10\,\mathrm{bit}$ Time-Over-Threshold (TOT) measurement with $25\,\mathrm{ns}$ granularity and a $14\,\mathrm{bit}$ Time-Of-Arrival (ToA) measurement with a $1.5625\,\mathrm{ns}$ binning.

The telescope consists of $7\times$ Timepix3 assemblies readout by the SPIDR system [8]. The clock distribution to the planes is assured by a Trigger Logic Unit (TLU) providing the time reference (t_0) and measuring accurately the coincidence signal of two scintillator tiles located at each end of the telescope. The mechanical assembly of the telescope is illustrated in Figure 3.

The Devices Under Test (DUTs) characterized with the telescope are positioned at the center of the telescope and aligned using motorized rotation and translation stages. The clock from the TLU and the t_0 signal are provided to the DUT along with a trigger signal produced from the

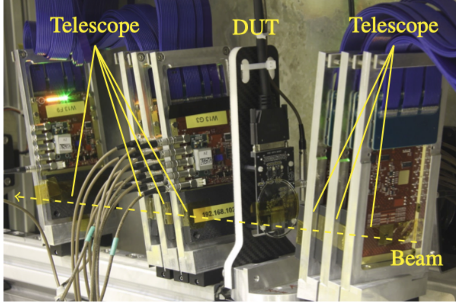


Figure 3: The CLIC Timepix3 telescope installation at CERN SPS H8 beam line.

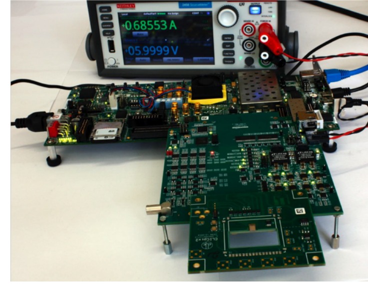


Figure 4: The CaRIBOu readout system hardware with a mounted CLICpix2 carrier board.

coincidence of the scintillator tiles. The data collected are reconstructed using the Corryvreckan and EUTelescope reconstruction framework [9], [10]. Combining the timing information of the scintillators and the telescope planes, a timing resolution per track of 1 ns is achieved along with a pointing resolution at the DUT of 3 µm.

2.2 The CaRIBOu test system

The control and readout interface board unit (CaRIBOu) [4] is a versatile readout system designed to facilitate the design of the interface to pixel detector prototypes. It consists of a hardware system, composed of the CaR board, the Zynq ZC706 FPGA development board and a prototype specific carrier board unit, as illustrated in Figure 4.

The CaR board is a custom board interfacing to the Zynq FPGA that provides the resources needed for a variety of prototypes, listed below.

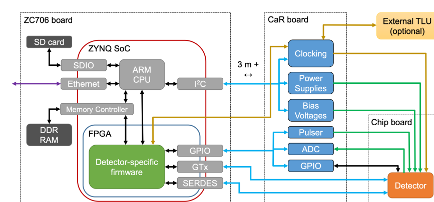


Figure 5: Schematics of the hardware, firmware and software interface of the CaRIBOu system.

- 8 × adjustable power supplies, 0.8 to 3.6 V,3 A
- 32 × adjustable voltage references, 0 to 4 V
- 8 × adjustable current references, 0 to 1 mA
- 4 × programmable injection pulsers
- 10 × output and 14 × input CMOS signal, 0.8 to 3.6 V
- 17× LVDS signal routed to FPGA + 8× full-duplex GTx links for high speed data transmission up to 12 Gbit/s
- Low jitter clock generator, slow and fast ADC, 8 × 50 ks/s, 16 × 65 Ms/s

The firmware for the CaRIBOu system is developed using a modular architecture with the different functionalities needed for the readout integrated in self-contained Intellectual Property blocks (IPs) interfaced to the Zynq ARM CPU through a standard AXI4 bus. The software for the system is based on the yocto Linux distribution and provides the libraries to control the interfaces connected to the FPGA, as illustrated in Figure 5. The software provides a Hardware Abstraction

Layer (HAL), a convenient way to control all the resources of the CaR board and communicate with the device specific firmware IP blocks implemented for each DUT. For test-beam operation with the Timepix3 telescope, an interface to the TLU receiving the clock and t_0 signal have been implemented to synchronize the DUTs to the telescope and enable their characterization.

2.3 TCAD and Allpix^2 Monte-Carlo simulation

During the detector design phase of our prototypes, input from TCAD simulation is used to provide guidance to make technological choices. However, the computing time required for simulating the interaction of particles with the detector spans from minutes for simplified two dimensional simulations to hours for more complex three dimensional simulations which makes it impractical to predict the behavior of devices in statistical terms.

The Allpix^2 framework [5] was developed to provide a versatile, generic tool for Monte-Carlo simulations of pixel detectors. The geometry to be simulated is described using text interface and includes all the features of pixel detectors such as support printed circuit boards (PCB), bump-bonds and other materials attached to the device. The particle sources are defined and the interactions of the particles with the detectors are simulated using Geant4. The resulting deposited energy, converted to electron-hole pairs, can be propagated through the bulk of the sensors using the provided propagation modules that include effects of drift, diffusion and the Lorentz effect when in presence of magnetic field as shown in Figure 6. The electric field can be selected from implemented models or imported from a TCAD simulation software in the DF-ISE format. The resulting propagated charges can then be converted to signal provided to the front-end electronics. The digitization of the signal is performed using parameterised models of the front-end response. . The final simulation results can be output in various telescope reconstruction frameworks such as Corryvreckan [9], Proteus [11] and Eutelescope [10]. This feature allows for easy comparison between simulated and test-beam data.

The software structure of Allpix^2 is highly modular, with a core software providing the required facilities such as geometry description, parsing tools, logging tools and persistent storage of the generated data. The simulation steps, from energy deposition to digitization are enclosed in modules that make use of the core functions. New modules can easily be integrated to replace or supplement the simulation flow. A typical simulation configuration is illustrated in Figure 7.

3 Vertex and tracker detector prototypes

The CLICdp collaboration's effort in developing new technologies for vertexing and tracking covers the study of hybrid solutions and novel monolithic pixel detector technologies. Hybrid detectors, by separating the readout electronics from the sensor, allow for more complex integration and logic at the cost of more complicated interconnect technology. Planar sensors, capacitively-coupled CMOS sensors (CCPD) and enhanced lateral drift sensors (ELAD) are under study. The monolithic CMOS approach, integrating the sensor and readout in the same silicon die, avoids the complex interconnect process and achieve lower material budget, at the cost of reduced functionality with regard to the hybrid solution. Silicon-on-insulator (SOI) CMOS pixels, high-voltage HV-CMOS and high-resistivity HR-CMOS technologies are under study. SOI-CMOS and Enhanced lateral Drift (ELAD) hybrid sensors are covered in a separate proceeding article of this series.

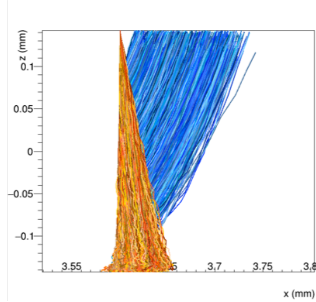


Figure 6: Propagation of the generated electrons (blue) and holes (red) in the substrate of an example pixel detector.

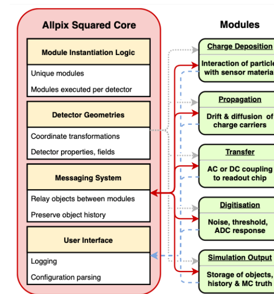


Figure 7: Structure of the Allpix^2 framework for a typical simulation.

Table 1: CLICpix2 in-pixel analog front-end performance for continuous operation.

Parameter ($C_{det} = 20$ fF)	Value
Area	25×12 μm^2
Power dissipation	6.6 μW
Amplifier gain	33 mV/ke$^-$
ToT dynamic range	270 ke$^-$ (h$^+$)/ 150 ke$^-$ (e$^-$)
ToA accuracy	10 ns (w/ offline cal.)
Input-referred noise	67 e$^-$
Input-referred mismatch error	28 e$^-$
Minimum threshold	438 e$^-$ (w/ 6σ margin)

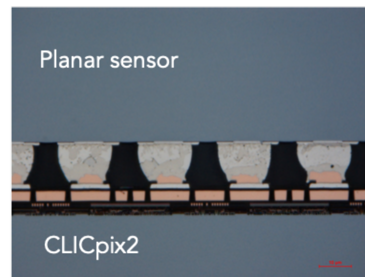


Figure 8: Bump bonds in a cross-section of a CLICpix2 and planar sensor assembly. Credits: IZM

3.1 Planar sensor assemblies and CLICpix2

The CLICpix2 ASIC [12] is a 65 nm CMOS pixel readout designed to meet the requirements of the CLIC vertex detector. The matrix consists of 128×128 pixels with a pitch of $25 \times 25\,\mu\mathrm{m}^2$. Each pixels provides a 5 bit TOA and 8 bit TOT measurement over a clock up to 100 MHz. Power-pulsing of the matrix and readout circuitry is implemented and executed through an external control signal to reach the power consumption target for CLIC vertex detector of $50\,\mathrm{mW\,cm^{-2}}$ in CLIC operation conditions. Table 1 summarize the achievable simulated performance of the analog front-end. A low threshold ($\geq 440\,\mathrm{e}$) and low noise ($70\,\mathrm{e}$) are required to handle the small signal of the thin, low material budget sensors under study.

Hybridization of the CLICpix2 to planar sensors produced with active-edge technology produced with Advacam and FBK was performed at IZM using SnAg bump-bonding technology. The ASICs, already diced, were mounted on support wafers and went through the bump deposition process. The fine pitch of 25 µm of the ASIC and sensor represent a challenge for this technology, but preliminary results shows that interconnect yields of above 99.9% can be achieved. Figure 8 show an example of successful bump connection between the sensor and ASIC. Further studies of the assemblies are ongoing and and new high-density interconnect technologies such as an-isotropic conductive films (ACF) are explored.

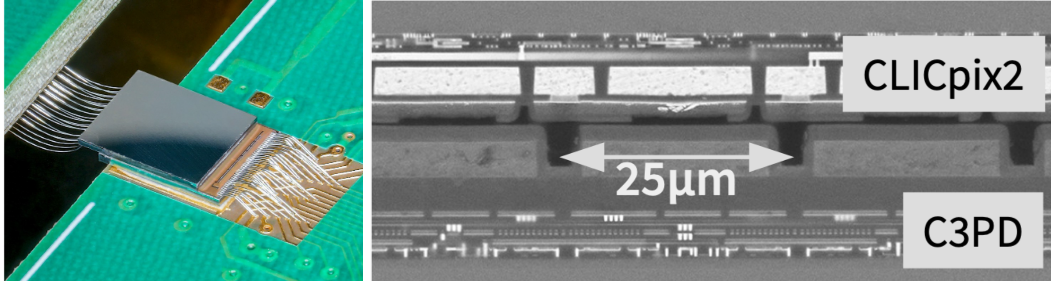
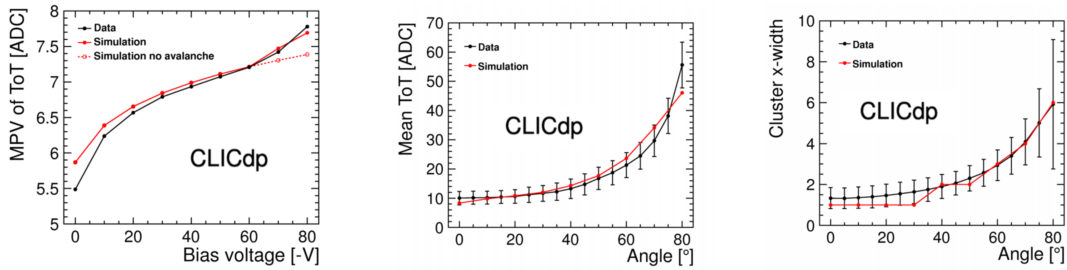


Figure 9: C3PD and CLICpix2 assembly wire-bonded to its carrier board (left), electron microscopy of the C3PD and CLICpix2 ASIC interface after gluing. A layer of less than 100 nm of glue is present between the passivation layers, creating a large capacitance for the transmission of the signal (right).



(a) Most Probable Value (MPV) for energy deposition in TOT unit versus bias voltage.

(b) MPV versus incident particle angle.

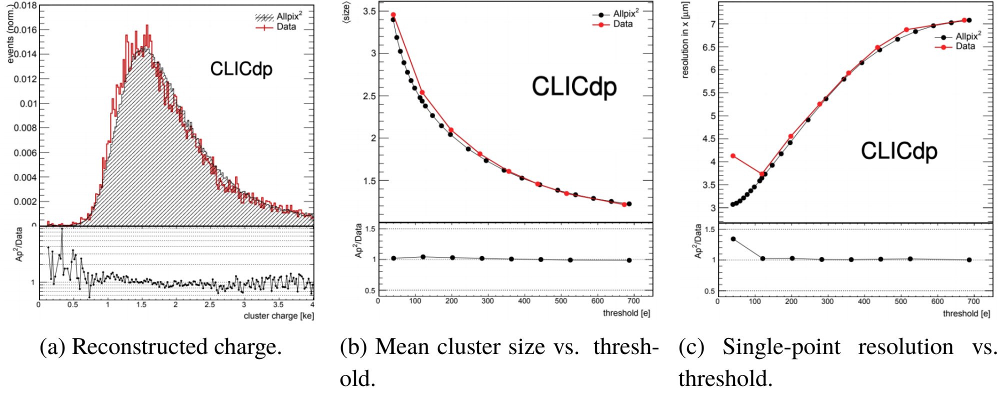
(c) Cluster size versus incident particle angle.

Figure 10: Comparison of test-beam data and TCAD simulation for the CCPDv3 sensor coupled to the CLICpix ASIC [17].

3.2 Capacitively Coupled Pixel Detector (CCPD) sensor assemblies

CCPDs were investigated using sensors designed for AC coupling to readout ASIC and produced in a commercial 180 nm HV-CMOS technology. The C3PD sensor [13] and its predecessor the CCPDv3 [14] were produced with the footprint of the CLICpix2 and its predecessor the CLICpix [15]. The coupling to the ASIC is performed through a thin glue layer applied to the sensor with a glue dispenser, followed by precision alignment and connection with the use of an ACCμRA 100 high accuracy bonder [16]. Figure 9 shows an example of a glue assembly on a PCB and of the achieved interface between ASIC and sensor.

The CCPDv3 and C3PD were simulated using TCAD [17]. The signal generated by particles at different angle of incidence was simulated and the transfer function of the readout electronics was applied to the simulated signal. The produced assemblies were characterized in test-beam using the Timepix3 telescope. Figure 10 shows a comparison of results obtained with TCAD and front-end simulation and the experimental results obtained from test-beam. Further characterization of CCPD assemblies can be found elsewhere [18].



(a) Reconstructed charge. (b) Mean cluster size vs. threshold. (c) Single-point resolution vs. threshold.

Figure 11: Comparison of measured and simulated tracking characteristics of the ALICE Investigator

3.3 Monolithic small fill-factor sensors

For the CLIC tracking detector, monolithic pixel sensors are foreseen due to their large scale production capabilities and low material budget achievable. Small fill-factor CMOS sensors are composed of a small n-type collection electrode separated from a large p-type well in which the readout electronics is located. The separation of the CMOS circuitry from the collection diode well allows to reduce cross-talk between the two elements. The small size of the collection electrode leads to a small input capacitance and therefore low noise and power consumption of the front-end. The ALICE Investigator chip [19] was characterized in test-beam using the Timepix3 telescope. Detailed TCAD simulation of the different diode geometries included in the Investigator were produced [20] in order to understand the charge collection process with small collection diodes. The electric field simulated was imported into Allpix^2 and a detailed simulation of the test-beam was carried out. Figure 11 show comparisons of the simulation to test-beam measurements showing a good agreement between the model and collected data.

Following the encouraging results from the ALICE Investigator, a CLIC specific sensor has been designed meeting the requirements of the CLIC tracking detector. Using TCAD and Monte-Carlo simulation validated with Investigator data, the implant layout and geometry of the pixels was optimized to meet CLIC requirements. Details of the simulations can be found elsewhere in the proceeding series. The CLICTD technology demonstrator consists of physical pixels of $30 \times 37.5\,\mu\mathrm{m}^2$ containing a pre-amplifier and discriminator combined in a logical pixel of $30 \times 300\,\mu\mathrm{m}^2$, as illustrated in Figure 12. Each logical pixel can measure TOT with 5 bit precision and TOA with 8 bit precision using a 100 MHz clock. Each logical pixel also provides the information on which physical pixels were fired during the active period. The ASIC implements power-pulsing of the front-end and readout electronics in order to meet CLIC power consumption requirements. CLICTD was sent for production in

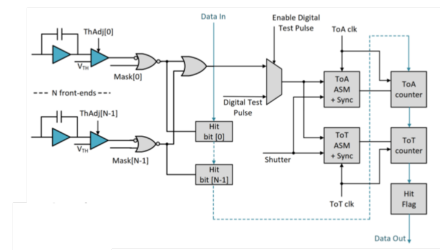
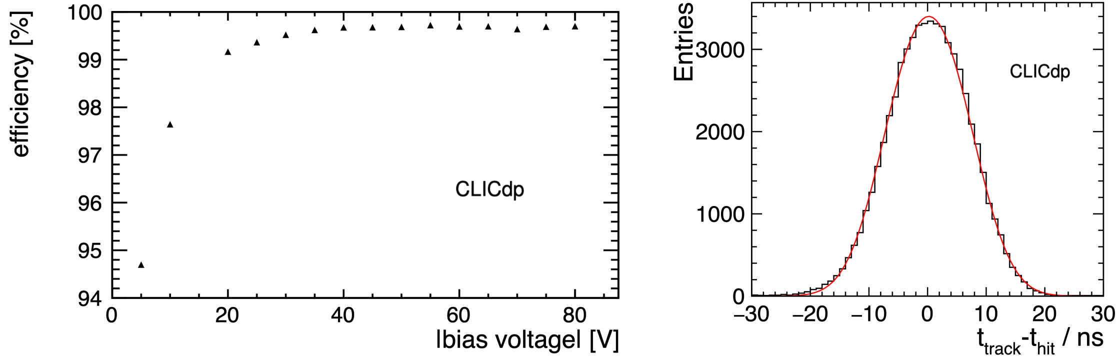


Figure 12: Schematics of the CLICTD pixel front-end.



(a) Detection efficiency versus bias voltage at the nominal threshold of 1000e.

(b) Timing distribution after correction.

Figure 13: ATLASpix test-beam characterization results.

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3.4 Monolithic large fill-factor sensors

Large fill-factor Monolithic CMOS sensors implement the readout electronics in a large n-type well that acts as the collecting electrode. The ATLASpix simple sensor [21], originally designed for the ATLAS CMOS collaboration, is being characterized in test-beam to evaluate its performance with regard to CLIC tracking detector specifications. It consists of a large matrix of $16 \times 3.25\,\mathrm{mm}^2$ pixels with a pitch of $130 \times 40\,\mu\mathrm{m}^2$. Each pixel provides a $10\,\mathrm{bit}$ TOA and $6\,\mathrm{bit}$ TOT measurement on a clock of up to $160\,\mathrm{MHz}$. Data are readout through a $1.6\,\mathrm{Gbit/s}$ serial link. A prototype of the ATLASpix sensor with a substrate resistivity of $200\,\Omega\cdot\mathrm{cm}$ was thinned to a thickness of $100\,\mu\mathrm{m}$ and characterized in test-beam using the Timepix3 telescope.

Figure 13 shows the results for detection efficiency, spatial and temporal resolution of the ATLASpix prototype. Due to the low resistivity and thickness of the substrate, only a low amount of charge sharing was observed (approximately 10% multi-pixel clusters) and the spatial resolution in both directions is compatible with the pitch of the pixel. Good detection efficiency at perpendicular incidence angle was observed over a large range of bias voltages. The timing resolution was measured using a $16\,\mathrm{ns}$ binning. Correction for a time-walk and for the systematic delay of each row of the sensor was applied offline. A timing resolution σ_t of $7.2\,\mathrm{ns}$ (RMS) is achieved. Taking into account the TOA binning and the lack of time structure in the CERN SPS beam, a fit of a box function convoluted to a Gaussian function was performed. For a fixed box width corresponding to the TOA binning, an intrinsic resolution for the pre-amplifier and discriminator of $5.6\,\mathrm{ns}$ can be extracted.

4 Conclusion

The CLICdp vertex and tracker R&D focuses on identifying the most promising technologies for the realization of a detector meeting CLIC physics requirements. The CLICdp Timepix3 telescope

and the CARiBOu readout system where developed to efficiently perform characterization of the prototypes in test-beam and in laboratory. TCAD simulations, in combination with the Allpix^2 framework, have been developed and used to gain understanding of current and future prototypes. The CLICpix2 ASIC was developed, meeting CLIC specifications, and studied using planar and CCPD sensors developed by the collaboration. Monolithic sensors with small and large fill-factor electrodes were simulated and characterized and the obtained results show good agreement with the simulation. Further prototypes fulfilling further the CLIC vertex and tracker requirements are designed and being produced.

Acknowledgments

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