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TimePix3 performance in power pulsing operation

E. Perez Codina[1)*]

[*] *CERN, Switzerland*

Abstract

The physics aims at the proposed CLIC linear e^+e^- collider impose challenging requirements on the performance of the detector system. In particular for the vertex detector the principal challenge is building an ultra-low mass ($\sim$0.2% X_0 per layer) detector that can provide a single point resolution of a few micrometers as well as 10 ns time slicing capabilities. To reach such low material budget, CLIC uses an air-flow cooling system in the inner vertex region. This requires very low power dissipation, which is achieved by exploiting CLIC's low duty cycle ($\sim< 0.001\%$) and beam structure, allowing pulsed power operation of the pixel detector. Timepix3 includes power pulsing features, such as, in the analog domain, allowing to switch dynamically between nominal power and shutdown modes, and, in the digital domain, gating the clock of the pixel matrix. This contribution reports the performance of the Timepix3 chip in pulsed power operation, in terms of power saving, detection efficiency and noise performance. Measurements were performed in beam tests taking as reference tracks provided by a telescope, as well as in the laboratory using a radioactive source.

Poster presented at VERTEX (27th International Workshop on Vertex Detectors), Chennai, India, 21–26 October 2018
This work was carried out in the framework of the CLICdp Collaboration

[1] estel.perez.codina@cern.ch

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Timepix3 performance in power pulsing operation

E. Perez Codina[*†]
CERN, Switzerland
E-mail: estel.perez.codina@cern.ch

The physics aims at the proposed CLIC linear e^+e^- collider impose challenging requirements on the performance of the detector system. In particular for the vertex detector the principal challenge is building an ultra-low mass ($\sim$0.2% X_0 per layer) detector that can provide a single point resolution of a few micrometers as well as 10 ns time slicing capabilities. To reach such low material budget, CLIC uses an air-flow cooling system in the inner vertex region. This requires very low power dissipation, which is achieved by exploiting CLIC's low duty cycle ($\sim< 0.001\%$) and beam structure, allowing pulsed power operation of the pixel detector. Timepix3 includes power pulsing features, such as, in the analog domain, allowing to switch dynamically between nominal power and shutdown modes, and, in the digital domain, gating the clock of the pixel matrix. This contribution reports the performance of the Timepix3 chip in pulsed power operation, in terms of power saving, detection efficiency and noise performance. Measurements were performed in beam tests taking as reference tracks provided by a telescope, as well as in the laboratory using a radioactive source.

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[*]Speaker.
[†]on behalf of the CLICdp collaboration

1. Introduction

The Compact Linear Collider (CLIC [1]) is a future e^+e^- collider project at CERN, with collision energies between 380 GeV and 3 TeV. It has a duty cycle below 0.001%, with colliding beams consisting of bunch trains separated by 20 ms. For energies of 1.5 TeV and above, each bunch train contains 312 bunches spaced by 0.5 ns, thus each bunch train length is only 156 ns. The CLIC detector [2] requires high precision vertexing in order to achieve the CLIC physics goals. The low duty cycle and beam structure allows for power pulsing in the vertex detector. By applying pulsed power to the detector the power consumption can be significantly reduced and therefore the need for heat dissipation is reduced. As a consequence it is possible to use air cooling in the vertex detector. Air is blown through the spiral-shaped vertex endcap detectors and thus there's no need for cooling pipes. This approach reduces the passive material budget in the vertex detector. The low material budget minimises multiple scattering and allows excellent vertexing and flavour tagging performance. To study the feasibility of power pulsing in the CLIC vertex detector, power-pulsing capabilities have been implemented and studied in the Timepix3 ASIC, before CLIC specific front-end ASICs became available.

2. Power pulsing in Timepix3

Timepix3 [3, 4] can record the hit arrival time (ToA) and charge measurement (ToT) simultaneously in each pixel without dead time (if the hit rate is below 40 Mhits/s/cm^2). The 14 mm$\times$ 14 mm chip consists of a 256×256 array of squared pixels, each of 55 µm^2 area. The pixel time stamp resolution is 1.56 ns, and the power consumption is less than 1.5 W/cm^2 (45 µmW/pixel) at a voltage of 1.5 V. The pixel columns are organised as double columns sharing the digital part of the pixels. The main building block is a structure of 4×2 pixels named SuperPixel. A double column is formed by 64 SuperPixels and the full pixel array is formed by 128 double columns.

The Timepix3 chip allows power pulsing of either the analog domain or the analog and digital domains simultaneously. In the analog domain, the three most power consuming bias lines in the front-end (the preamplifier and two of the discriminators) are multiplexed between the ON and OFF states, and are configurable through three independent DACon and DACoff values (see Table 1). In the digital domain, the system clock and the pixel matrix clock are gated (the clock

DAC Name	Length [bits]	DAC Range	DAC LSB
Ibias_Preamp_ON	8	0 to 5.1 μA	20 nA
Ibias_DiscS1_ON	8	0 to 5.1 μA	20 nA
Ibias_DiscS2_ON	8	0 to 3.4 μA	13 nA
Ibias_Preamp_OFF	4	0 to 300 nA	20 nA
Ibias_DiscS1_OFF	4	0 to 300 nA	20 nA
Ibias_DiscS2_OFF	4	0 to 200 nA	13 nA

Table 1: Range of the configurable DACs in the analog domain.

is not distributed to the pixel matrix) during the power-off state. In the CLIC use-case the power pulsing is enabled and disabled cyclically. In the present study only three parameters, illustrated in Figure 1, determine the power pulsing cycle: shutter open time (time during which the shutter is

open), power off time (time during which the power is off) and the delay (which is assumed to be the same before and after the shutter open time).

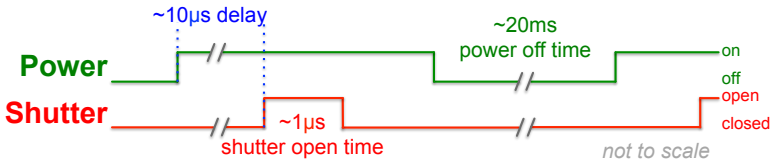


Figure 1: Illustration of power pulsing simplified configurable times. Quoted numbers are example times according to CLIC parameters.

In the analog domain, the transition from the low-power to the operational state (and vice-versa) happens consecutively in a fraction of columns at a time. This prevents peaks in power consumption during the transition. The number of double columns powered on/off simultaneously (1 to 8 double columns, equi-spaced in the pixel matrix) and time between powering on/off one double column and the next (0.05 to 10 µs) are configurable. The total time needed to power on or off the whole pixel matrix will depend on the power on/off scheme and on the system clock, as illustrated in Table 2. In the present study the power on and power off schemes are set to be the same. The default scheme is the fastest, which switches the whole matrix on/off in 0.8 µs.

Time [µs]		Number of simultaneous columns			
		2 columns	**4 columns**	**8 columns**	**16 columns**
Clock Divider	**/2**	6.4	3.2	1.6	0.8
	/4	12.8	6.4	3.2	1.6
	/8	25.6	12.8	6.4	3.2
	/40	128	64	32	16
	/50	160	80	40	20
	/100	320	160	80	40
	/200	640	320	160	80
	/400	1280	640	320	160

Table 2: Time (in µs) needed to power on and off the whole pixel matrix for a system clock of 40MHz, considering the different power on/off scheme configurations.

When the different super columns are turned on (from power off to power on state) it takes some time for the outputs of the front-end amplifiers to settle into a steady signal. During that time the output may cross the threshold discriminator level, injecting noise hits into the digital part of the detector. To avoid recording these noise hits, the shutter shall be opened after all the pixels are no-longer noisy. Since the super columns are turned on at different times, the delay between the power-on signal and the shutter-open signal should take into account both the matrix power-on time and the pixel stabilisation time, as illustrated in Figure 2.

3. Power consumption

For the power consumption measurements a chipboard is used, which allows the chip to be powered externally, and the intensity measurements are performed using the same low voltage

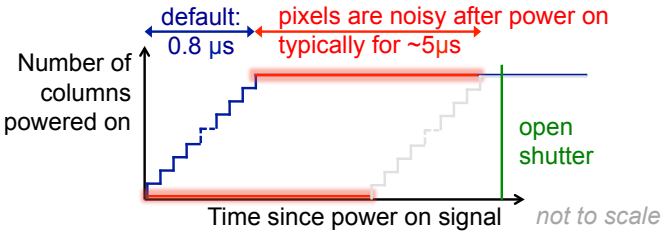


Figure 2: Illustration of power-on time (in blue), stabilisation time (in red), and shutter open time (in green).

power supply used to externally power the chip. The power consumption of the analog and digital domain is measured simultaneously in the two channels of the power supply. The power pulsing cycle is set to be long enough (power-off time = shutter-open time = 1 s, and delay = 10 µs) to be able to read in the power supply the power consumption in the power on and in the power off states. The setup for the power consumption measurements is illustrated in Figure 3.

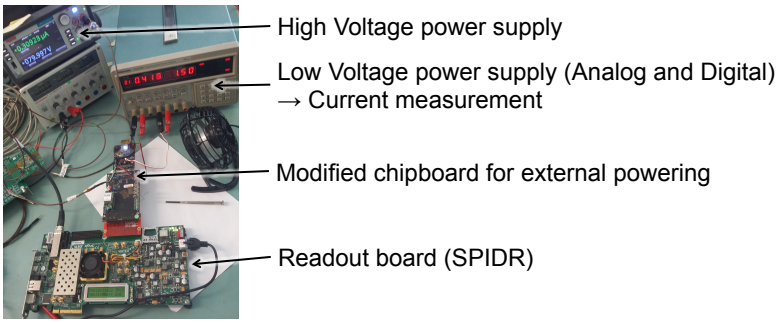


Figure 3: Laboratory setup for the power consumption measurements.

The measurements are performed both with the chip configured in the analog power pulsing mode and in the the analog and digital power pulsing mode. The three DACoff parameters are set to the same default value of DACoff=8. The analog and digital power consumption measured are shown in Table 3.

V_{Analog}=$V_{Digital}$=1.5 V DACoff=8	**No Power Pulsing**	**Analog Power Pulsing**		**Analog + Digital Power Pulsing**	
		on state	**off state**	**on state**	**off state**
I_{Analog} [mA]	400	399	92	399	92
$I_{Digital}$ [mA]	372	371	219	371	97

Table 3: The analog and digital intensity measured in each power pulsing mode for the on and off states.

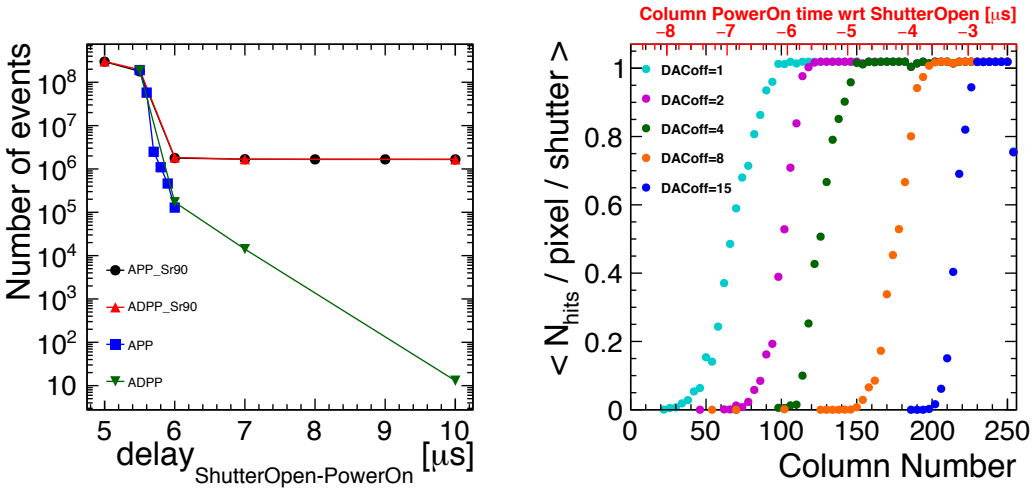
The power consumption is reduced by a factor of approximately 4 when the analog and digital power are in the off state.

4. Delay time optimisation

An important measurement for the characterisation of the chip under pulsed power operation

is the pixel noise stabilisation time, because it determines the delay time needed between power on and shutter open signals during data taking.

The time needed for the full chip to stabilise after the power on signal is estimated by performing a scan in the delay time and measuring the number of hits. For this, the chip is equalised and the threshold is set high enough that without power pulsing no noise hits are expected. The duty cycle is set to approximately 50%, and the number of hits received during 100 s is measured as a function of the delay time. Results are obtained for both Analog Power Pulsing (APP) and for Analog and Digital Power Pulsing (ADPP). Two series of measurements are performed, with and without a ^{90}Sr electron source placed above the sensor. The results are summarised in Figure 4(a).



(a) (b)

Figure 4: (a) Number of noise hits versus delay time between power on and shutter open. Results shown for Analog Power Pulsing (APP) and Analog+Digital Power Pulsing (ADPP), both with and without the presence of a Sr90 electron source. (b) Fraction of noisy pixels versus column number (1 bin corresponds to 4 columns). The delay time is 8.6 µs and the matrix is turned on 1 double column at a time, such that the whole matrix takes 6.4 µs to be fully powered. The top axis indicates how long before the shutter-open signal has a particular column been turned on.

The measurement with the ^{90}Sr source shows a stabilisation of the hit count at around 6 µs after the power has been switched on. At shorter delay times, the detector is dominated by noise effects. Without using the ^{90}Sr source, the number of noise hits is monotonically decreasing and is close to zero for a shutter open delay of 10 µs. Similar results are obtained for both APP and ADPP operation modes.

Measuring precisely the stabilisation time independently of the power-on time is possible thanks to the flexibility given by the power-on scheme. In this measure the power-on scheme is set to switching on one double column every 0.05 µs (clock divider = 2), and the delay time is set such that when the shutter opens some of the columns (those that are turned-on last) are still noisy while others are already stabilised. For this measure the delay parameter is set to 8.6 µs. The position of the columns in the chip defines when the columns are turned on after the power-on signal. By measuring the number of hits in each column it is possible to extract the time needed for all the pixels in a column to stabilise. With a single measurement, the equivalent of a delay

scan in 0.05 µs steps is performed. The measurement is repeated for several values of the DACoff parameter. The results are presented in Figure 4(b).

For the default DACoff=8 value, pixels are noisy for approximately 5 µs after they are turned on. The stabilisation time depends on the DACoff value. The larger the voltage difference between V(DACoff) and V(DACon), the longer it takes a pixel to become stable. Therefore there is a compromise to be made between power saving and delay time. In the use-case of CLIC (considering 10 µs power on delay time, 1 µs shutter open and 20 ms power off time) it is more convenient to use the lowest DACoff value due to the low duty cycle.

5. Performance

Studies of the Timepix3 performance under pulsed power operation mode were performed in beam test experiments at CERN using a 120 GeV pions. Results from beam test measurements obtained using the Timepix3 telescope as reference system for particle tracking show a stable hit efficiency and ToT distribution under power-pulsed operation. For these measurements the delay between the transition to power-on and the shutter opening is fixed to 10 µs. Both power pulsing modes (APP and ADPP) exhibit similar results.

6. Conclusions

The power pulsing functionality in the Timepix3 ASIC is highly configurable and therefore can be adapted to a wide variety of use cases. With the default parameters, the analog and digital power pulsing can reduce power consumption by a factor of about 4 during power-off state. The pixel stabilisation time has been measured to be about 5 µs, which needs to be added to the matrix power-on time to obtain the minimum delay needed between the power-on signal and the shutter-open signal. For each use-case the DAC values in the off state should be optimised to reach a compromise between the delay time and the power saving in the power-off state. In the CLIC vertex detector case, the duty cycle is so low that the total power consumption is minimised by using the lowest possible DAC values in the off state.

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