AIDA-2020-SLIDE-2019-003

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

Presentation

CALICE/ILD SiW-ECAL a 26 Layer Model and 1st Tests of a Long Slab

Boudry, Vincent (LLR) *et al*

23 November 2018

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

This work is part of AIDA-2020 Work Package **14: Infrastructure for advanced calorimeters**.

The electronic version of this AIDA-2020 Publication is available via the AIDA-2020 web site <http://aida2020.web.cern.ch> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-2020-SLIDE-2019-003>

CALICE/ILD SiW-ECAL
a 26 Layer Model and 1st Tests of a Long Slab

M. Anduze, V. Boudry, J.C. Brient, O. Korostyshevskiy,

F. Magniette, J. Nanni, H. Videau

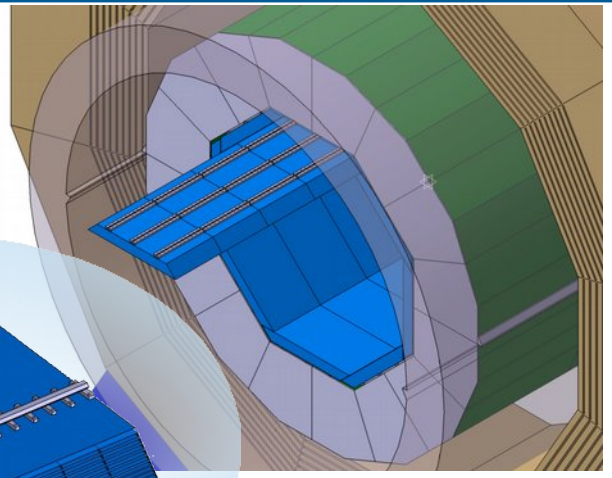
École polytechnique, Palaiseau

LCWS 2018
23.11.2018, Arlington (TX)

TNA support + WP14

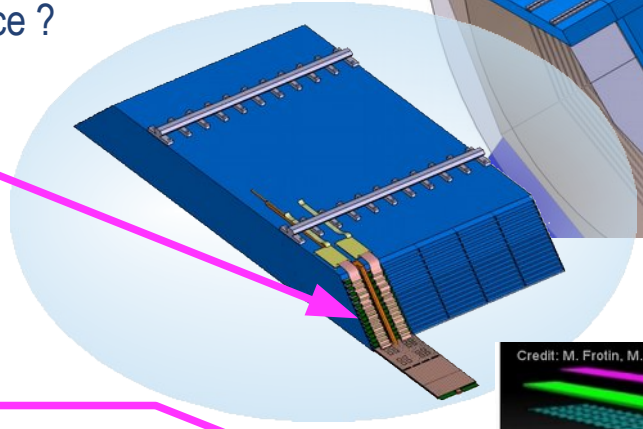
Introduction

SiW-ECAL ~ 30% of ILD costs (ILD Models of SiW-ECAL: **LoI, DBD**)
and most sensitive calorimeter (1/3 – 2500 mips, auto–trigger, high density)



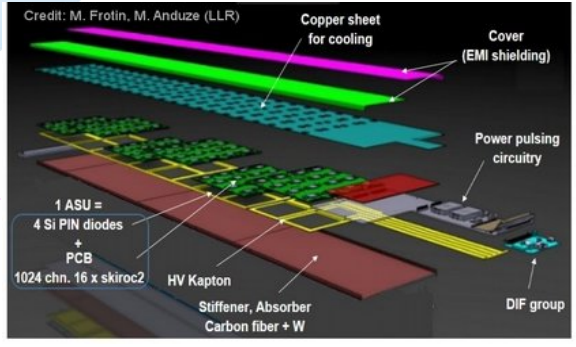
1) How to reduce costs without impact (too much) performance ?

- R_{INNER}^{ECAL} = 1842mm ↘ 1462 mm: in simulations
- **30 → 26 layers**
  - 8'', **725**µm wafers



2) Recent progress in feasibility studies:

- Base unit «ASU» ~ validated
  - almost validated **(see Adrián's talk)**: on beam test data: uniformity, noise, auto-trigger perf. Response low E and high E to be assessed
  - Updated version → **FEV13 design by Taikan**
- **1st prototype of a long slab (this presentation)**



Redefinition of dimensions

2 designs to be looked at:

- a "**baseline**" (or "large") with inner ECal radius at RECal =**1804mm**, (model close to the DBD)
- a "**small ILD**" model R_{ECal} ~1500 mm (all related quantities adapted ↔ R_{outer}[Endcaps])
  - Plus a model with slightly reduced number of layers = 26 layers (wrt 30).

Under work version of **ECal Technical Design Document** (TDD, 96 pages)
by Henri Videau (LLR), Marc Anduze (LLR) and Denis Grondin (LPSC) (+ ed. Daniel Jeans & Roman Poeschl) available on

https://llrbox.in2p3.fr/owncloud/index.php/s/eeVeAlyv8o27VRF

Small ILD with 26 layers → §5 of TDD.

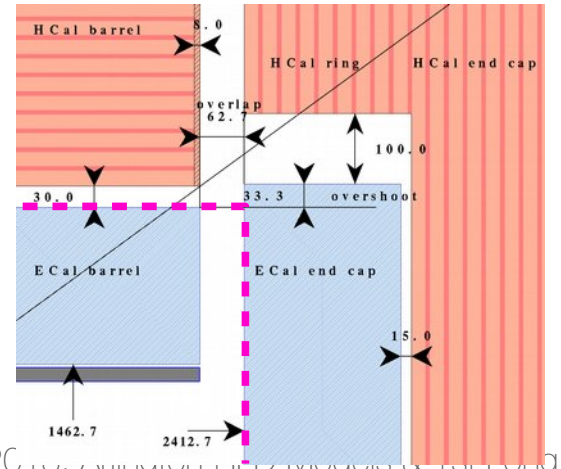
Dimension constructions (reminder)

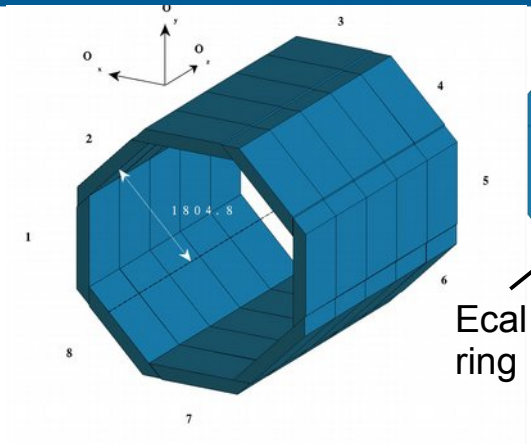
Barrel length fixed at **4700mm** in all models, *same as HCal or TPC*

- 8 staves ⊃ 5 CF/W modules ⊃ 5 alveoli columns
- 1 alveoli width = ~ 2 × wafers width + walls + clearance ~ **187.4mm**

Endcaps

- $Z_{front}^{EndCcaps} = Z_{outer}^{BarrelL}$ + overlap (62mm for Services + Security)
- $R_{INNER}^{EndCaps}$ fixed at 400mm ⇒ ECal ring
- $R_{OUTER}^{EndCaps} = R_{INNER}^{EndCaps} + n$ alveoli (+ wall, clearance)
- $R_{OUTER}^{Barrel} = R_{OUTER}^{EndCaps}$ – overshoot



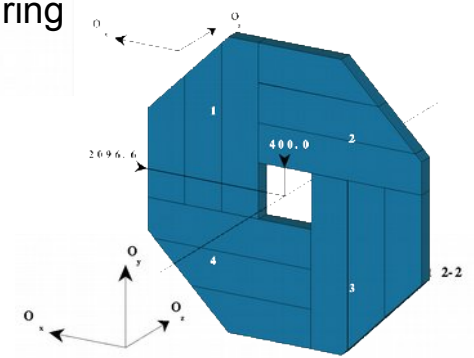


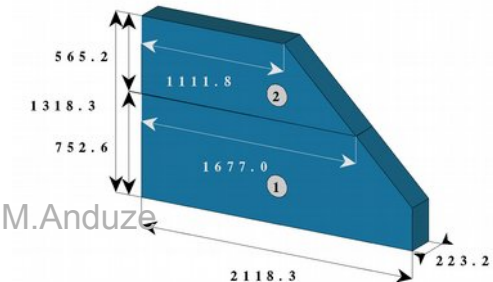
Baseline

- Endcap quadrant with 3 modules of 3 alveoli

Small

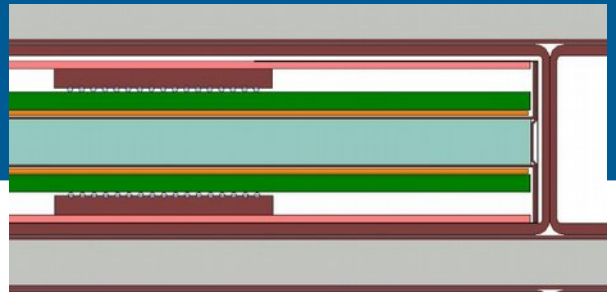
- Endcap quadrant with 2 modules of 4 and 3 alveoli





© M.Anduze

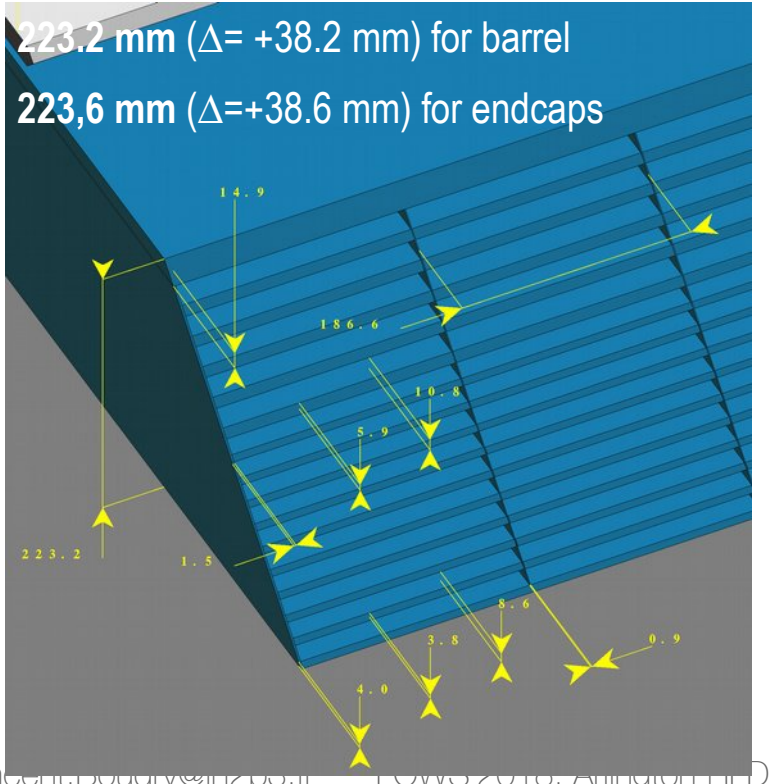
ECal thickness

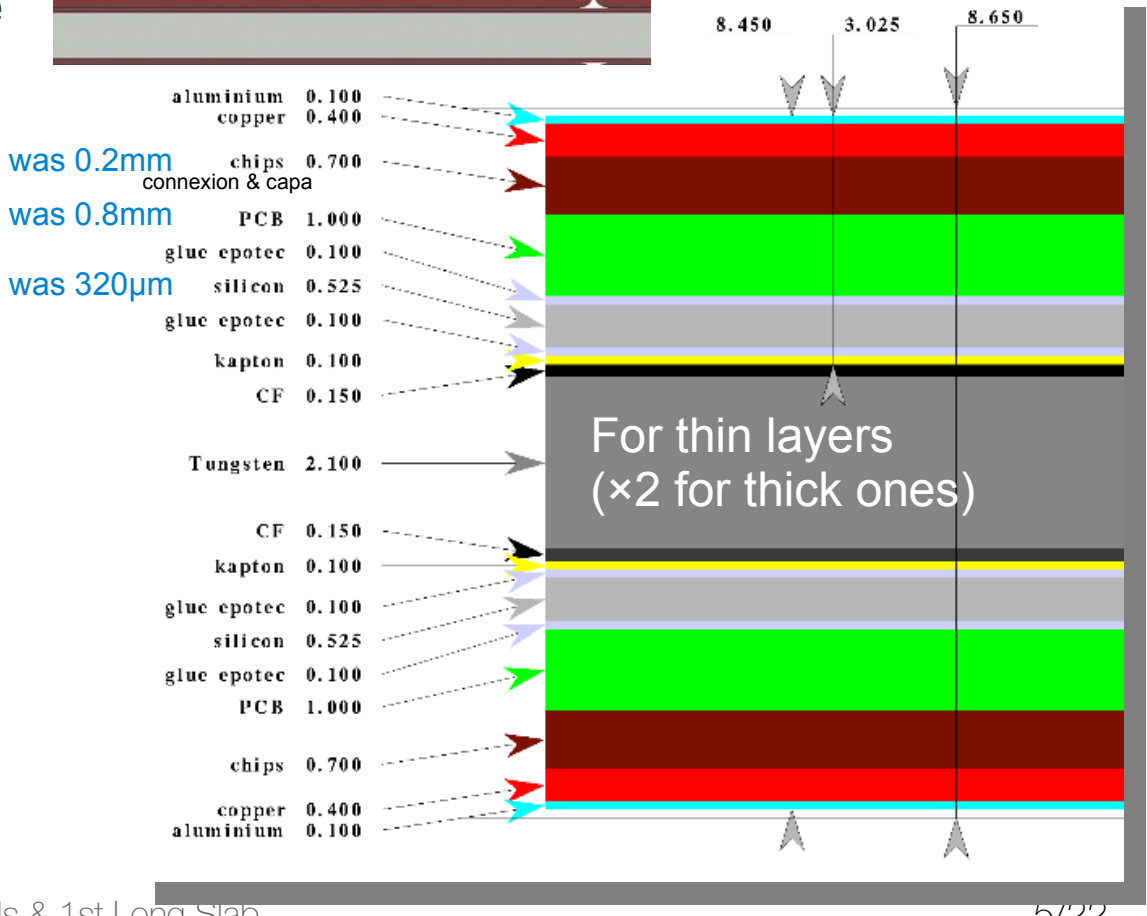


DBD thickness: **185 mm**, “hopelessly aggressive”

More realistic calculations

- **223.2 mm** (Δ= +38.2 mm) for barrel
- **223,6 mm** (Δ=+38.6 mm) for endcaps





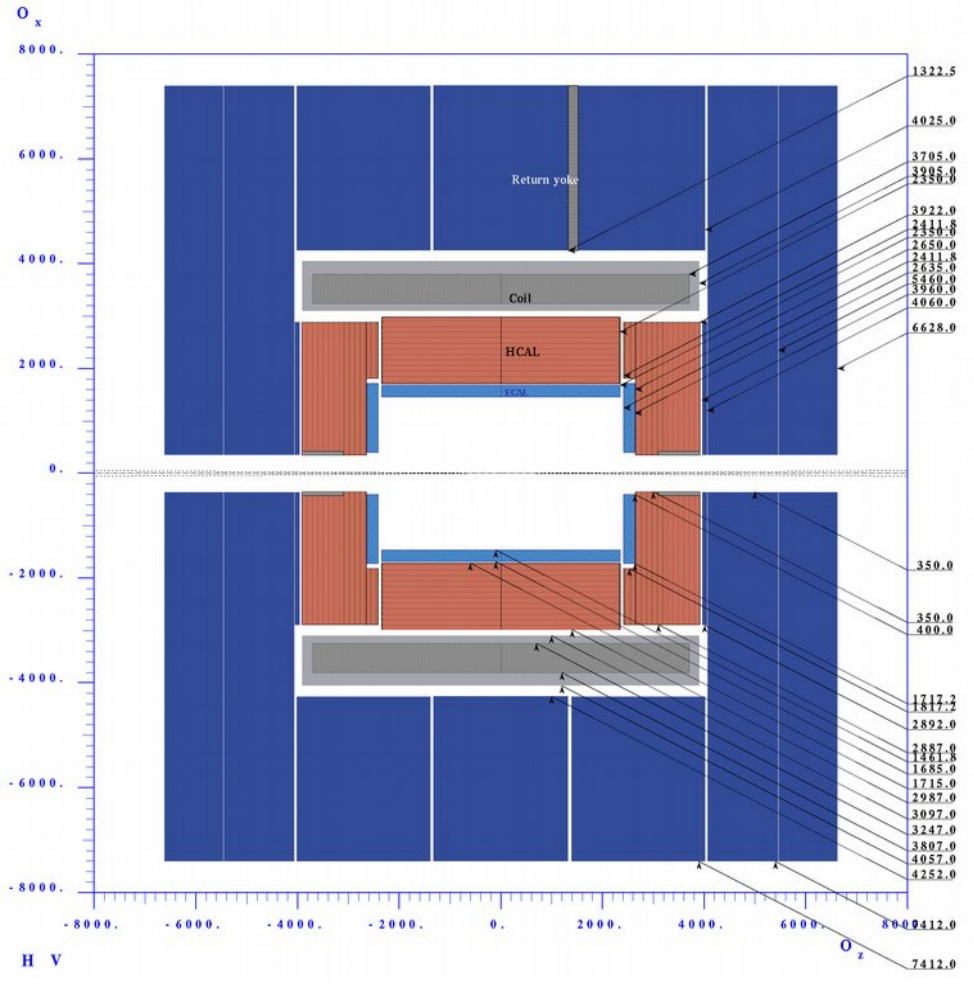
Small ILD

Same recommendations as for baseline:

- recalculated $R_{INNER}^{HCAL, BARREL}$ as 1500 + 185 + 30 = 1715mm

Small ILD ECal dimensions:

- $R_{INNER}^{ECal, BARREL} = R_{INNER}^{HCAL, BARREL} - 30mm - 223.2\ mm =$ **1461.8mm**
- $Z_{FRONT}^{ECal, EndCaps}$ = **2411.8 mm** (unchanged from baseline)
- $R_{OUTER}^{ECal, EndCaps}$ = **1717.2 mm**
  - 2 modules per quadrant of 4 (inner) and 3 (outer) alveoli
  - The overshoot of the end-cap to the barrel is then 32mm



Going to 26 Layers: performances

Going from 30 to 26 layers

- Reduction of cost; increase of Energy resolution
  - keep 24X_0 (84mm) of Tungsten

Increasing the Si thickness to 725µm

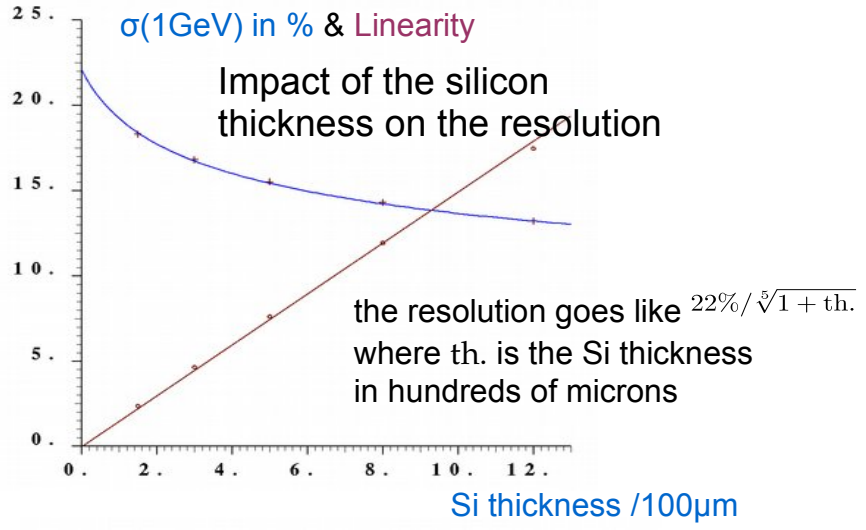
Energy resolution σ(E)/E:

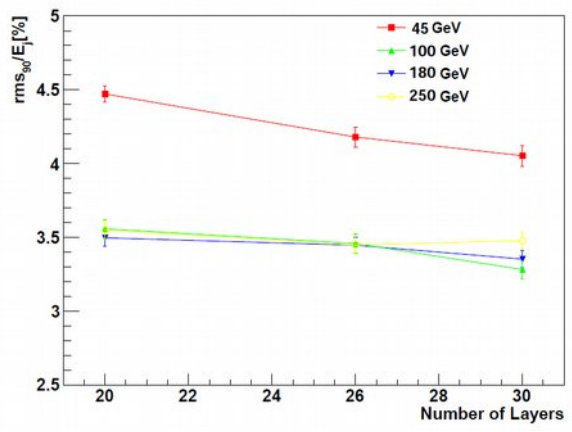
- for 26 layers w.r.t. 30: ↗ +8.5%
- with 725µm w.r.t 500µm : ↘ –6.6% (-8.7% wrt to DBD 300µm)

} *near compensation*

Study needed on dead zones (larger GR...), separation, resolution and efficiency performances at low energy.

- eg: JER : $\sigma(E_J)/E_J$ +6% for 26 layers (500 µm) to be redone...
  Shown @ 6th ILD Optim meeting (16/07/2014) [link]



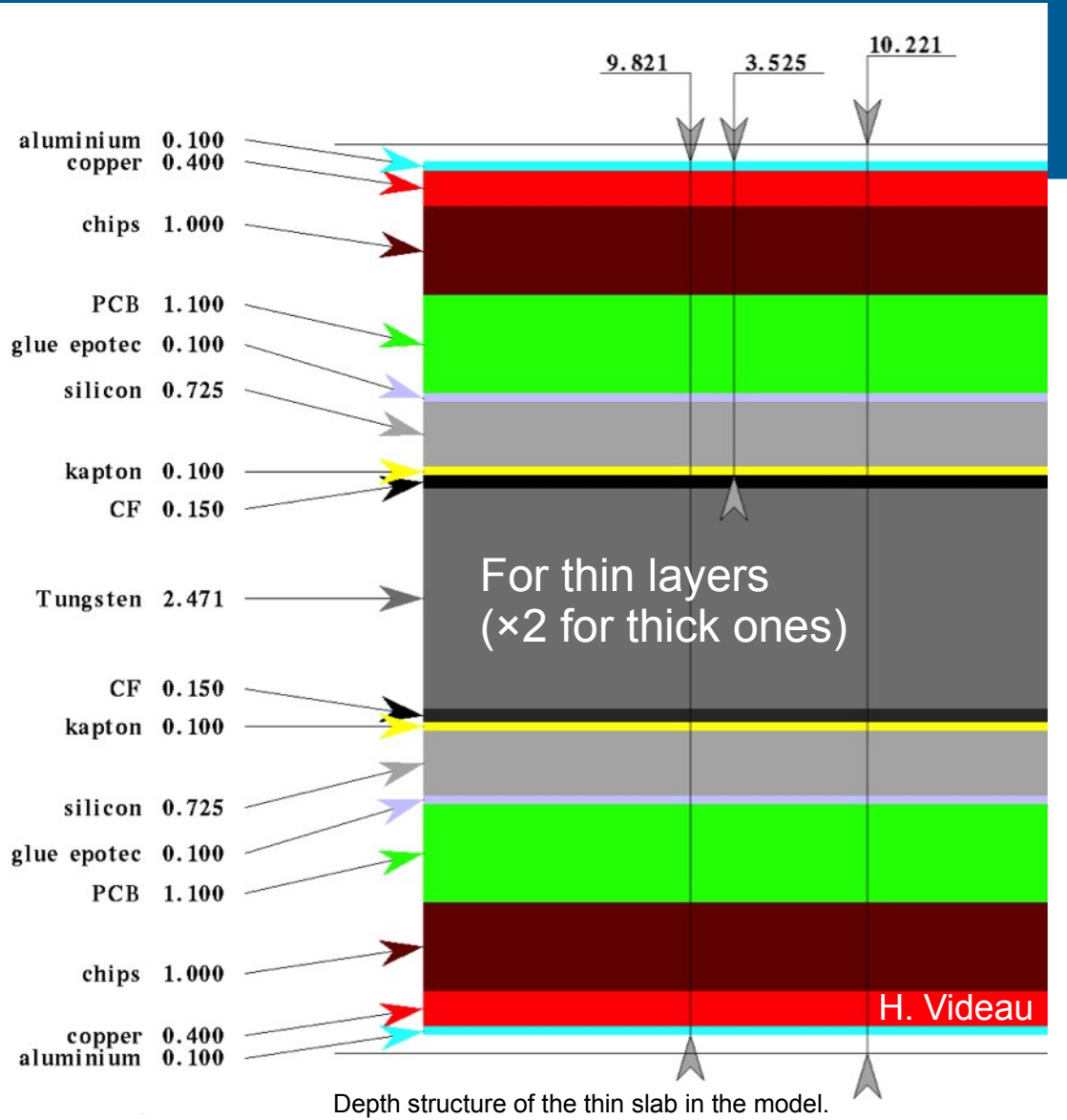


26 layers: dimensions

ECal thickness:

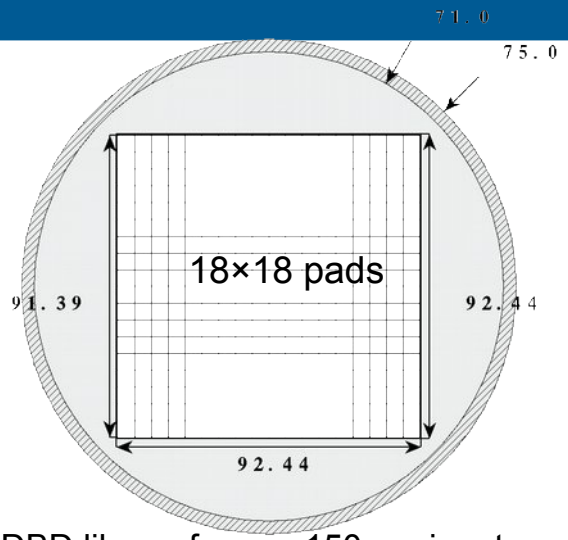
- 26 layers = 18 ‘simple’ layers with 2.47mm of W
  + 8 ‘double’ layers with 5.6mm
  shared between structure and slabs (4.94mm of W)
  - → 211.9 mm (wrt to 223.9 for 30 layer model)
- → relaxed constraints on
  - clearance margin inside alveoli : 2×0.1mm→**2×0.2mm**
  - chip packaging : 0.8mm → **1.0mm**
  - PCB thickness : 1.0mm → **1.1mm**

Total: 223.2mm → **222.2mm** + 1mm clearance

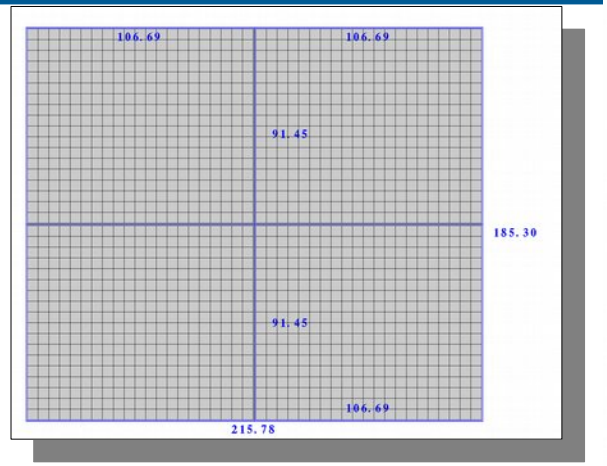


Depth structure of the thin slab in the model.

150 mm (6’’) Wafers

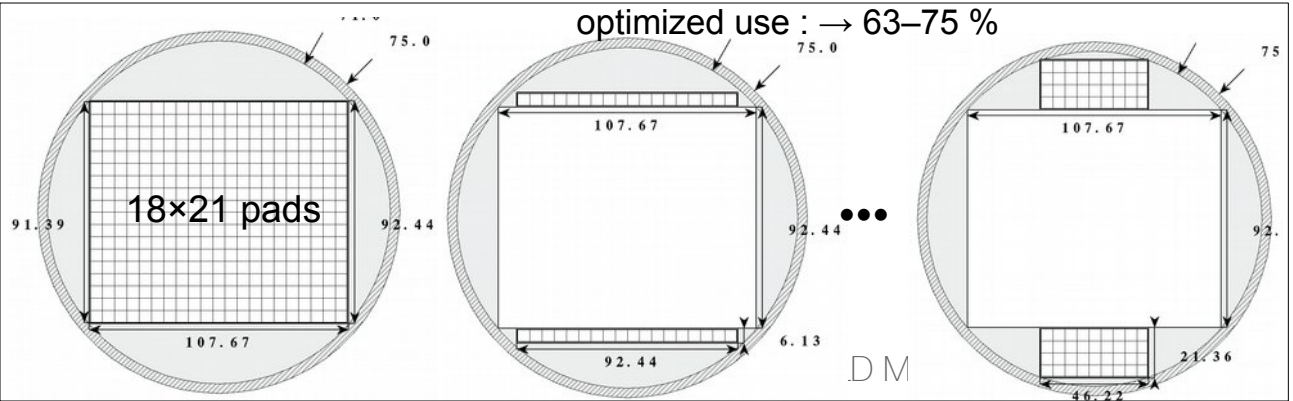


DBD like wafers on 150mm ingot
54 % use of surface

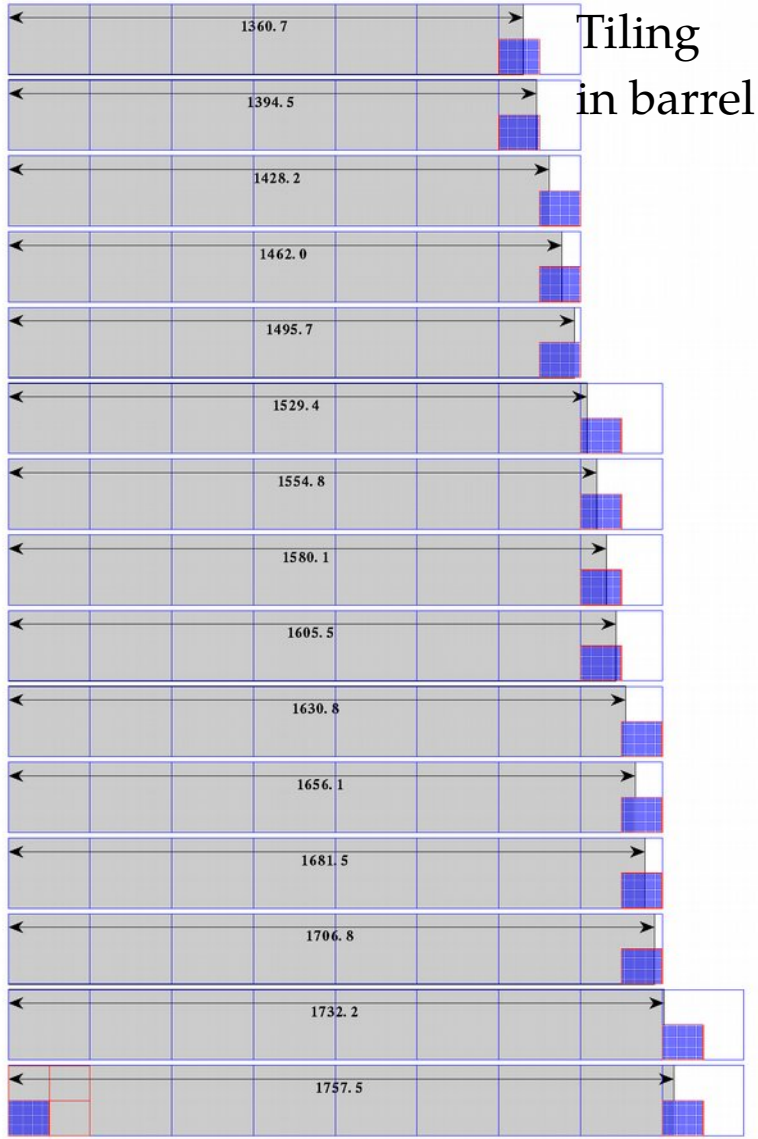


Pad size = 5.08mm
(prototype = 5.5mm)

optimized use : → 63–75 %



Tiling
in barrel



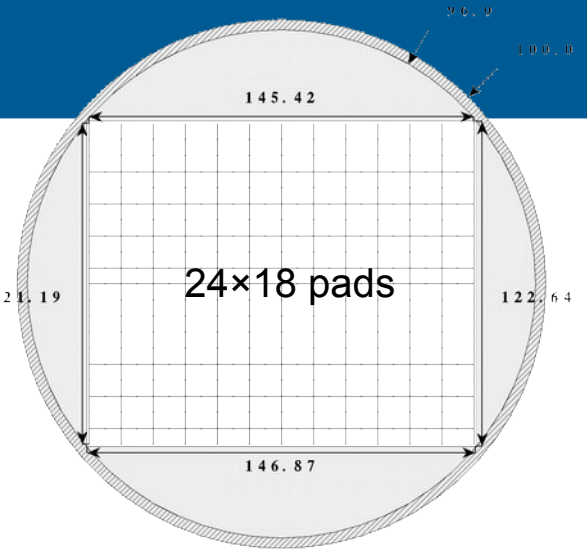
Going to 200mm Wafers…

From CMS HGCAL development & Hamamatsu contacts
future is 200mm (8") ingots, 725µm thickness

Mechanical constraints → ~187 mm alveoli, ~12 cm wafer

→ 1.5 Wafers ⊗ cell # mult. of 3 ⊗ cell width ~5 mm ⊗ paving with ~64ch ASICs

→ **30** or 36 cells in width



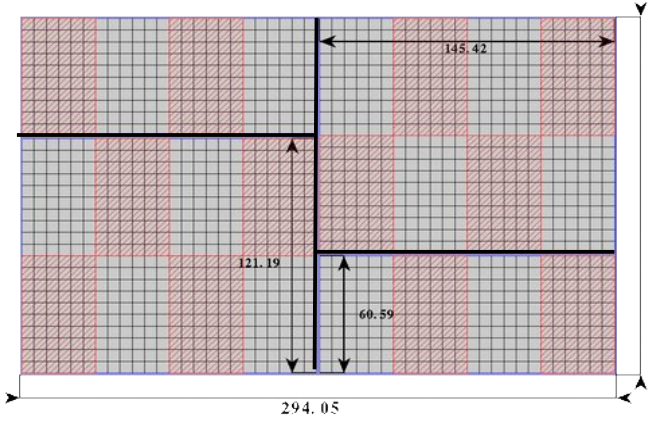
wafers on 200mm ingot ; 63 % use of surface

Optimised ReadOut electronics

- 6×6mm² , ASICs of 60ch.

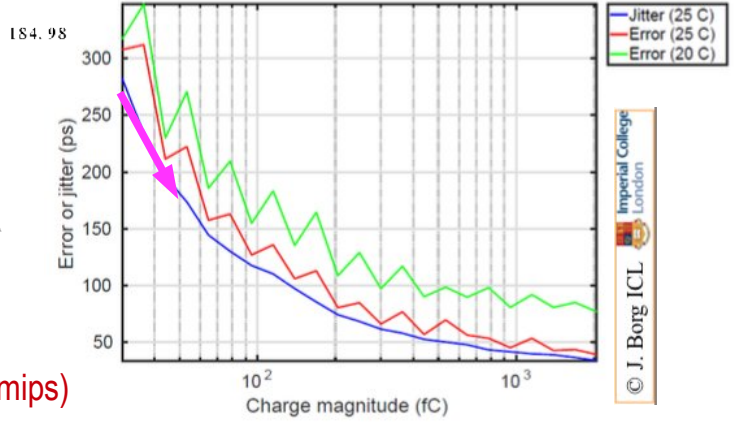
  wrt 5×5mm² (⚠ ≠5.5² of prototypes)

  30% less electronics
  consumption
  cost

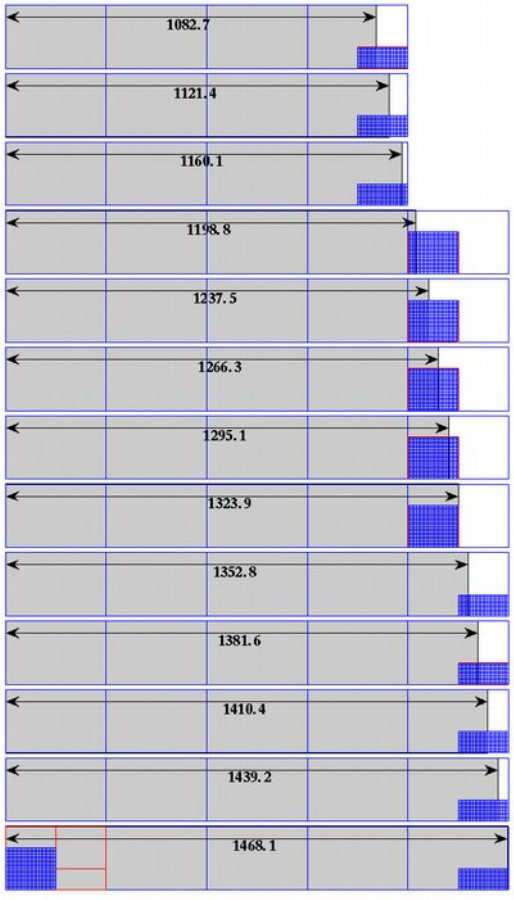


- ASU: 1440 pads, 24 ASICs
- Noise ~ C ~ width²/th. ~ cst, Signal ~ th ↗, S/N ~ ×1.5; depl. Voltage ~ th² (×2)

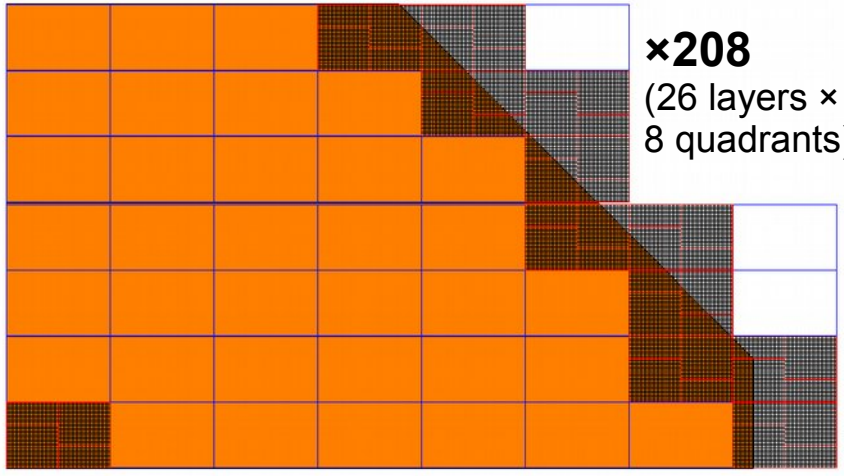
  ⇒ Improved timing perf (esp. for mips)



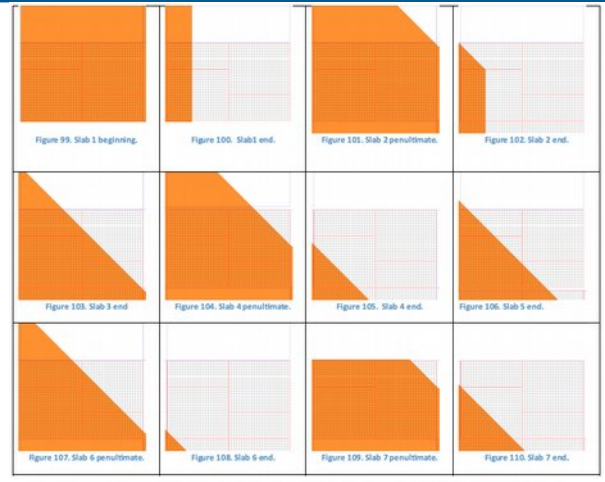
Tiling with 200mm (8’’) wafers



×400
(2 sides × 5 columns ×40 modules)

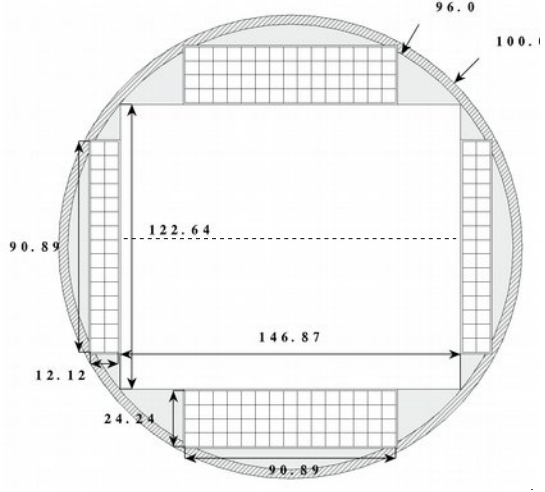


×208
(26 layers × 8 quadrants)

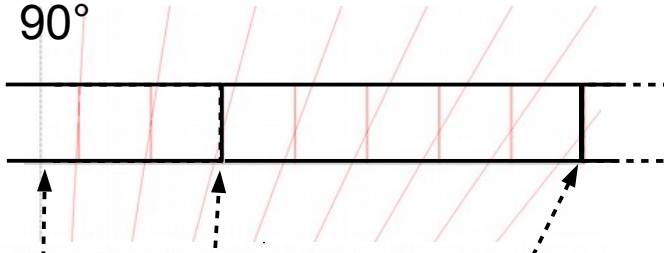


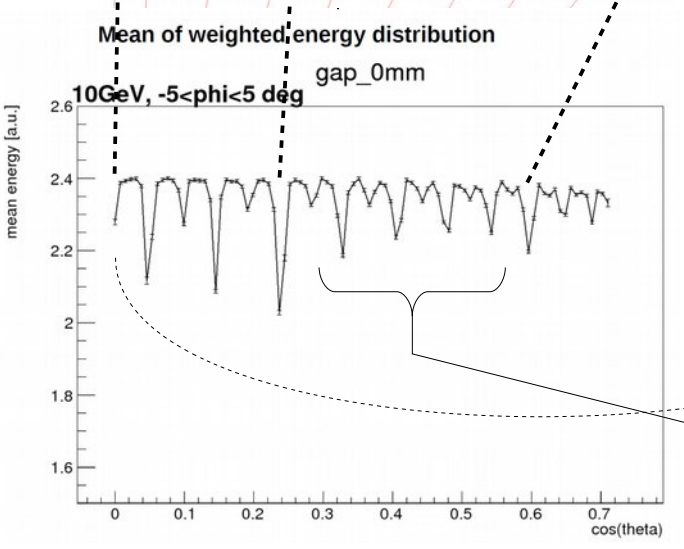
Matching of large and small rectangles, triangles and diamonds to be detailed for optimal use

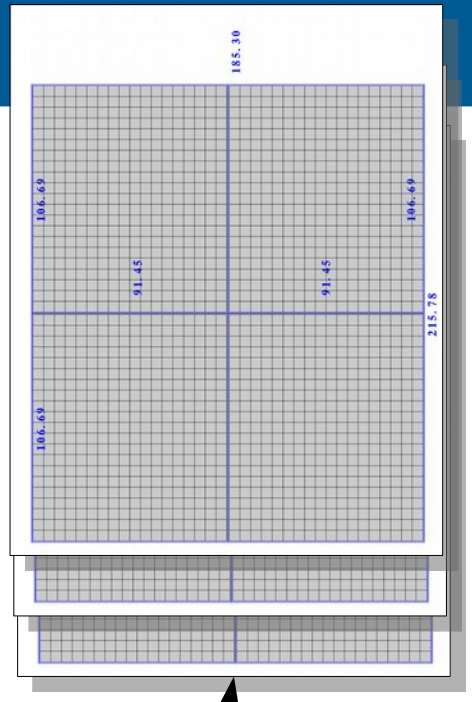
add’l small rectangles:
87 % use of surface
(83 % for an hexagonal shape)



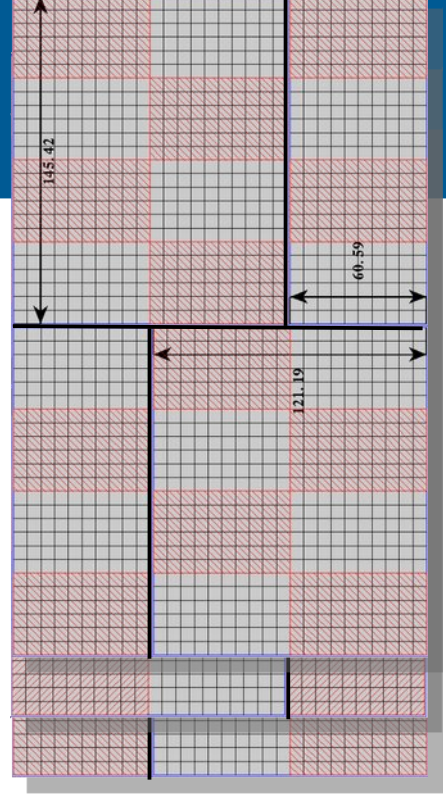
Reduced gaps



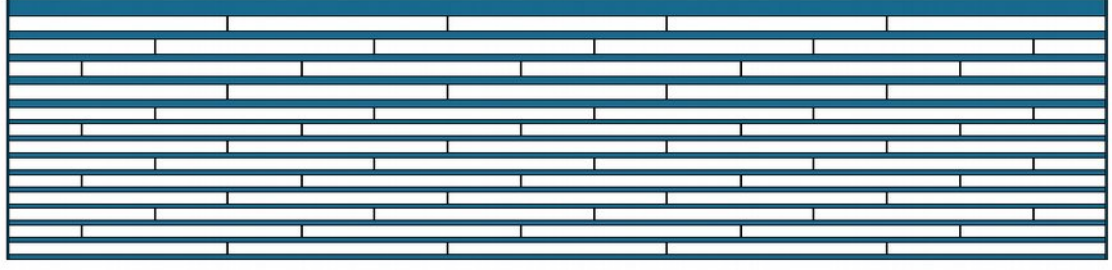




Reduced alignment of inter-wafer gap

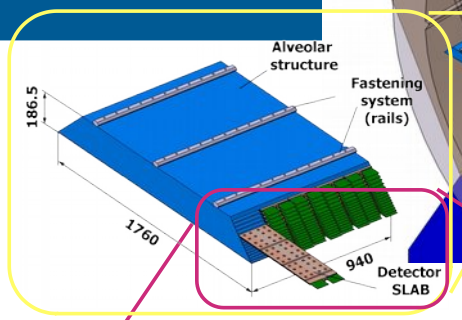


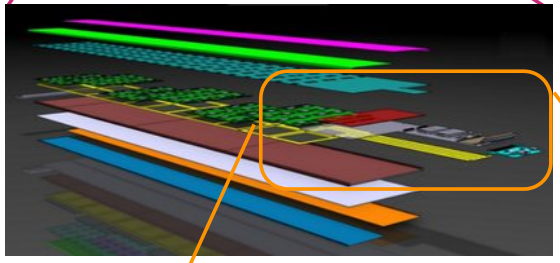
Possible *additional* reduction of inter-slab alignments



Prototypes

ILD & SiW-ECAL barrel





Copper (cooling)

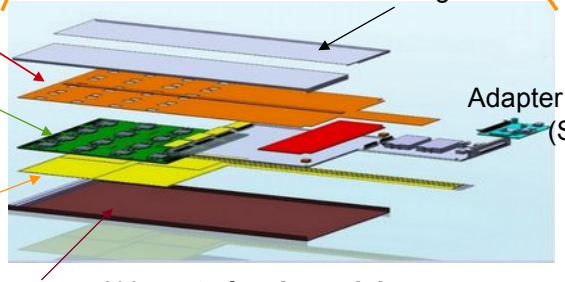
PCB (FeV)
16 SK2 ASICs
1024 channels

Shielding

Adapter board (SMB)

Wafer (4)

U Cradle
(Carbon Fi ~~+W~~)



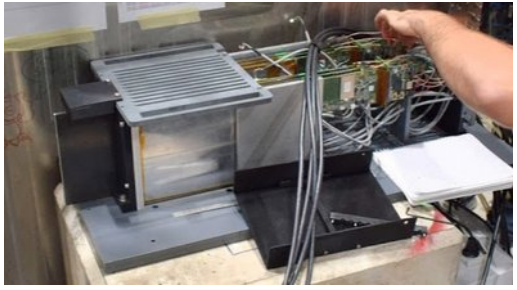
U layout of a **short slab**

LLR + LPNHE + LAL + Kyushu

2018

SLAB « long » (≤12 ASU)

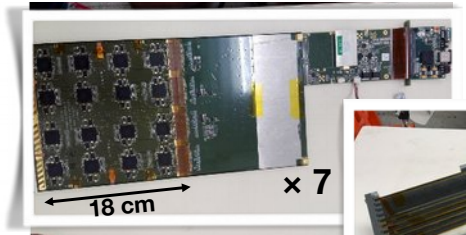
- Partie électronique + Baby W. (Signals, Power P.,)
  ⇒ Design Realistic SLAB

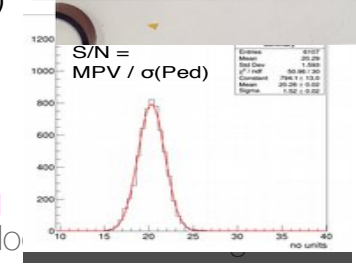


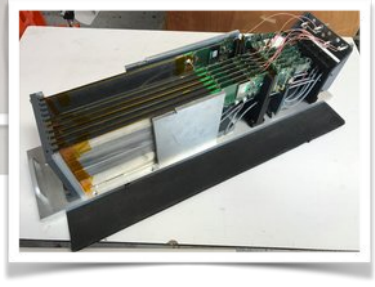
2018

Prototype technologique (1 ASU)

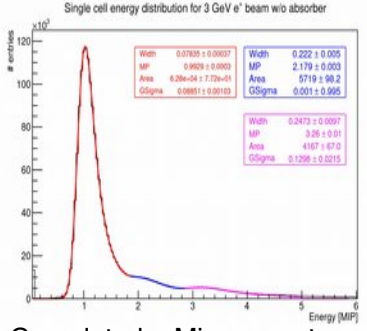
Tests au DESY (8 layers)
& CERN (10 layers ⊃ 4 FEV13, 650µm)







$S/N_{Trig} \sim 12$



Cumulated « Mip » spectrum in 3GeV e-

1st "electric long slab"

M. Anduze, F. Magniette, J. Nanni,
Realisation: G. Fayolle

Scale to support electronics

- Support of interface boards + 12 ASUs (DBD)
- 2+6+4 ASUs = ~3.2 m
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the botton

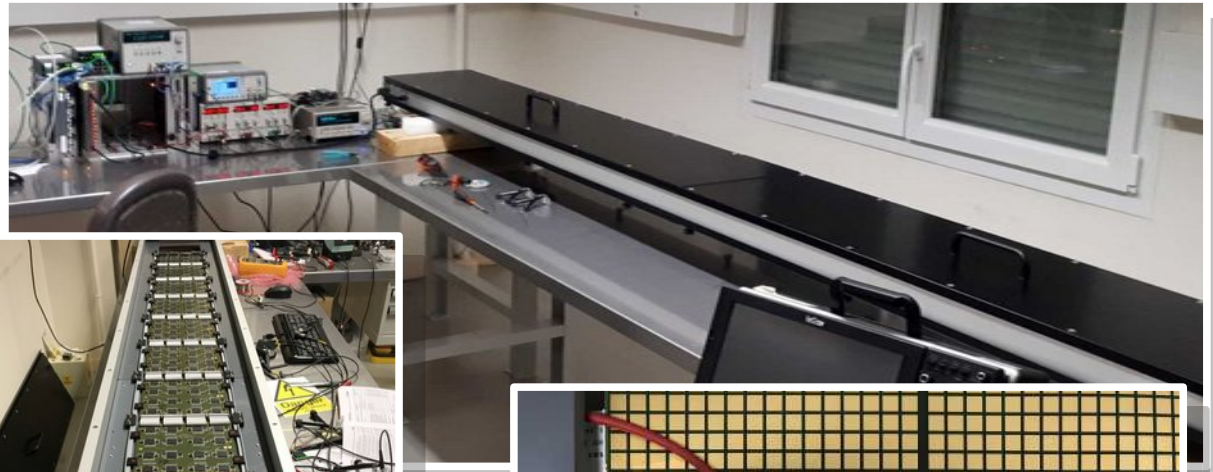
Mechanical characteristics

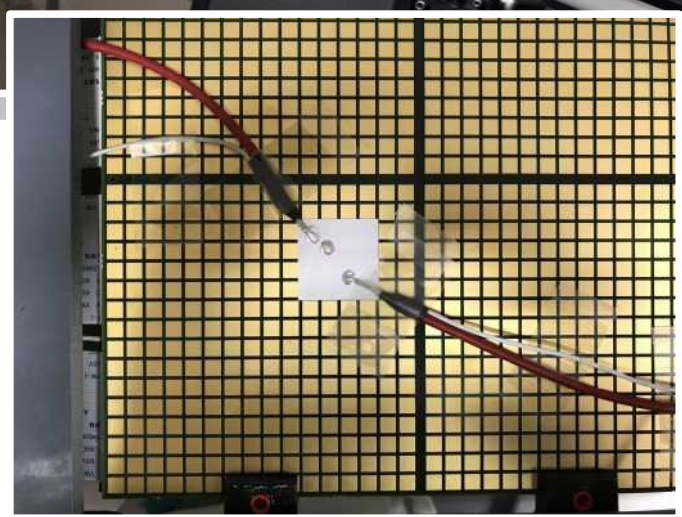
- Movable: table and to beam test
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm per ASU
- No electrical contacts scale / cards

Shielding

- vs Light and CEM

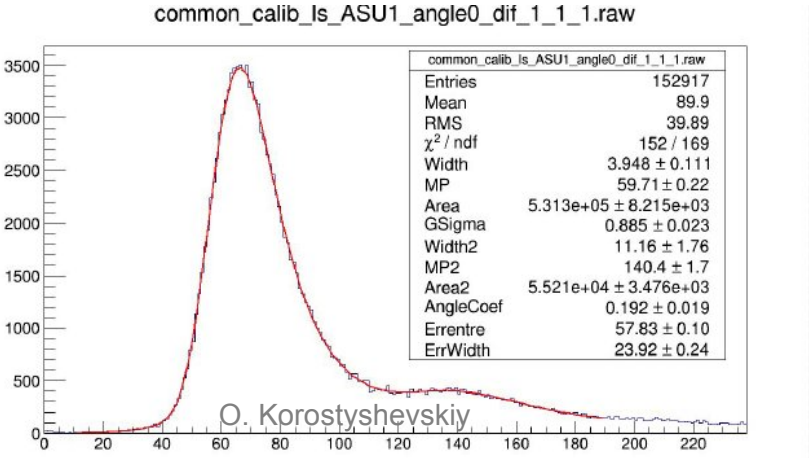


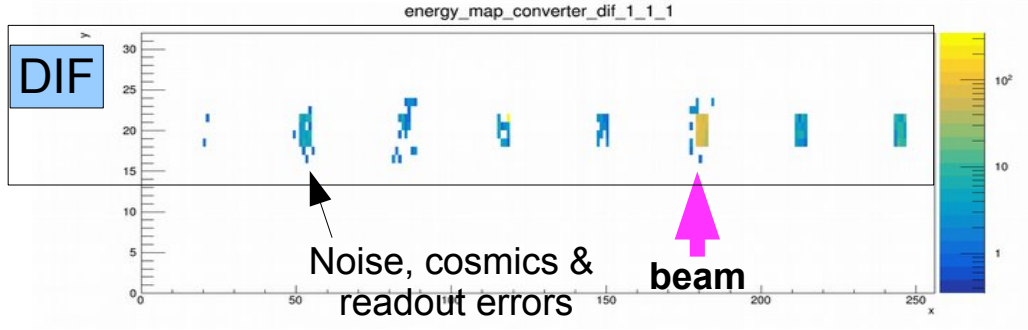


DESY-2018 beam test

2 weeks beg of July: full test of all prototypes:

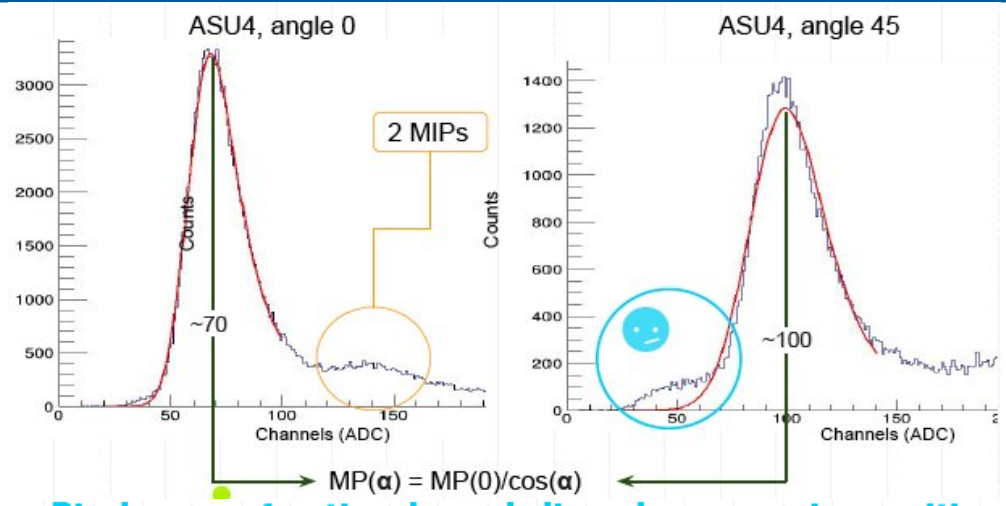
- Electric long slab: **8** FEV11 + baby-wafers (320µm 2×2cm²):
- RC Filtering of HV between (every second) boards required
- Very clean response to “mip” (punch through e-)

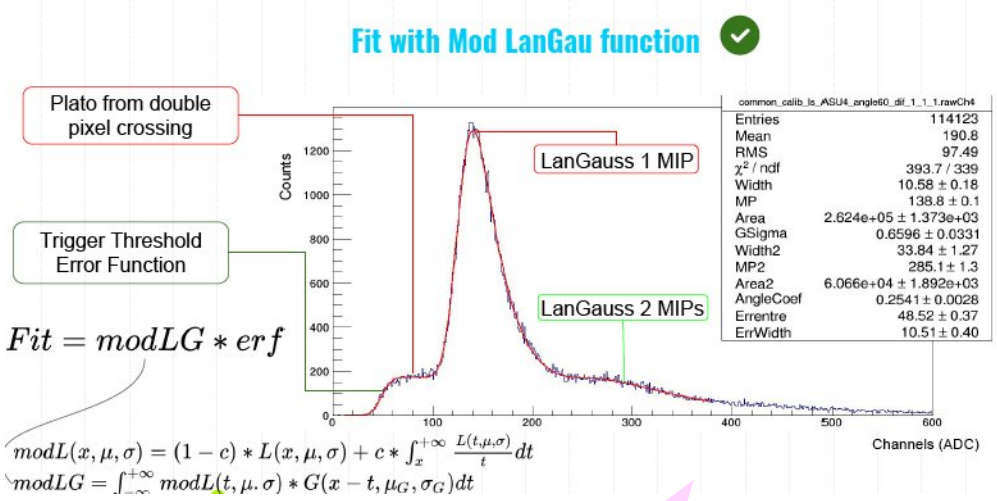




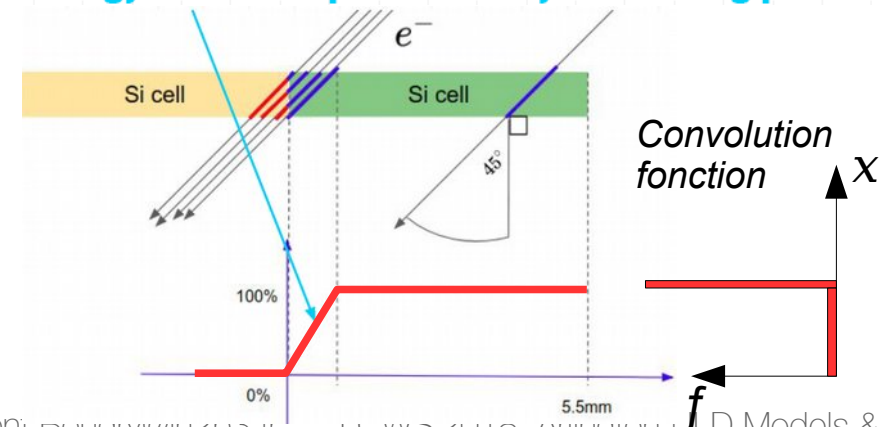
Mip analysis

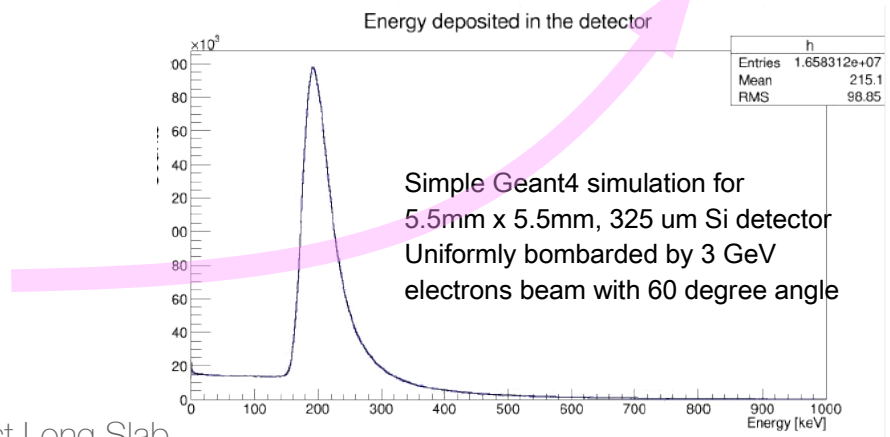
O. Korostyshevskiy





Pixel energy fraction depends linearly on crossing position



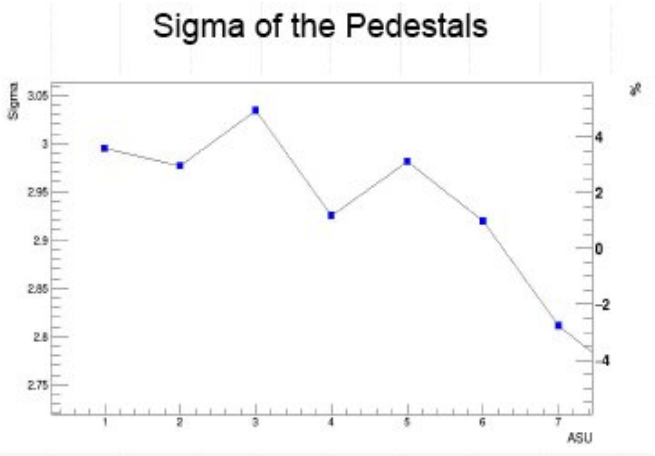


Simple Geant4 simulation for
5.5mm x 5.5mm, 325 um Si detector
Uniformly bombarded by 3 GeV
electrons beam with 60 degree angle

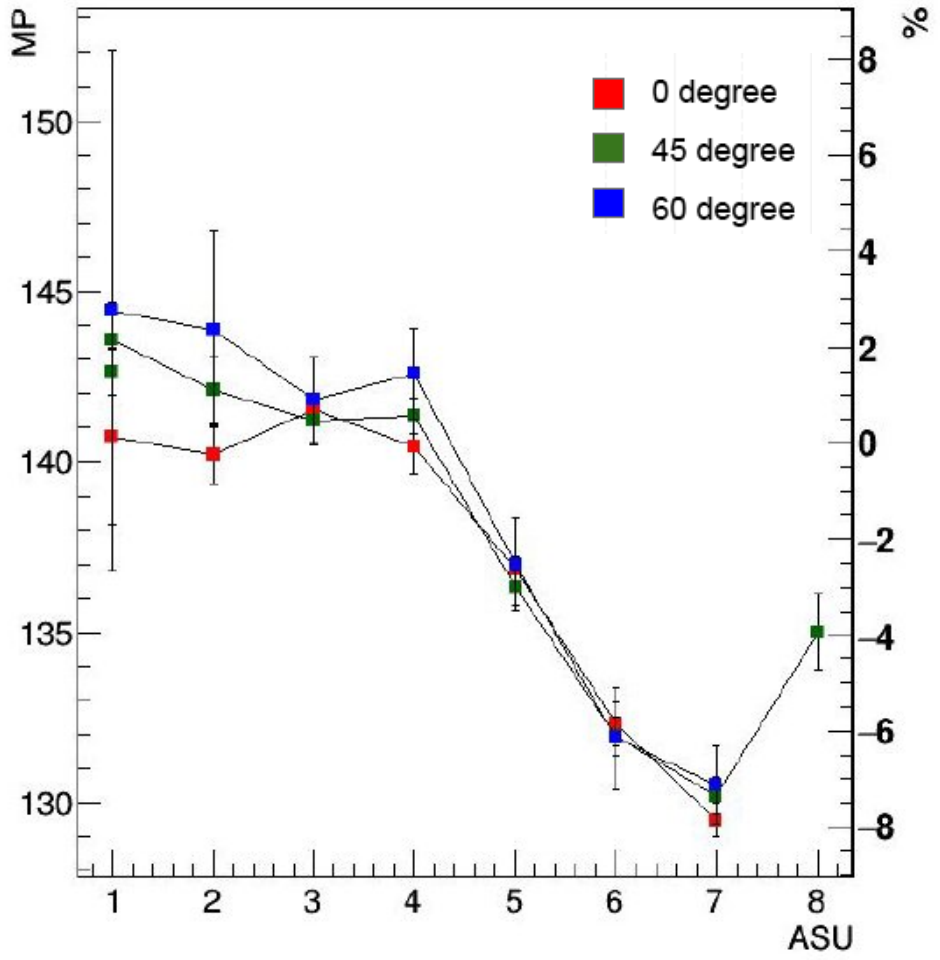
MIP response vs position

mip MPV *cos(θ) vs ASU#

- OK for 4 1st ASU's
- Small drop ~of signal ~2%/ASU for ≥ ASU#5
- Also hints similar drop on σ_{ped}



⇒ Voltage & Gain drop ?
Power pulsed mode with ballast et end of slab
(or just random build-up effect from chip variability ?)



Conclusions & prospectives

3 models described in detail for the ILD SiW-ECAL: ***baseline***, ***small***, **small with 26 layers**:

- 725µm thickness with 200mm (8") wafers ; 5.08 → 6mm cell size
  - ~ identical photon resolution expected
  - 13% gain cost on Silicon surface, PCB, and 40% on electronics (and power consumption) wrt DBD
  - Improved S/N ratio & timing, less channeling @ 90°

⊗ Feasibility improved:

- **Single ASU** + 1st connexion: S/N ratio, Stability, Uniformity between elements; **assessed**
  CALICE technical prototype (11 working ASU as of now)
  - Wafer of 325µm, **650µm tested** → 725 µm ? Hamamatsu ✔ Others: LFoundry(SMIC), Infineon, Elma, On-Semi
  - Wafer production: learn from HGCAL, statistics from current wafer batch ?
- **Long SLAB**: 1st readout over long chain: design R&D, power distribution, grounding; connexions between ASU's
  - ⇒ adjustment on HV & LV distribution, clock distribution needed ⇒ realistic (⊃ mech. constraints) design in 2019 ?

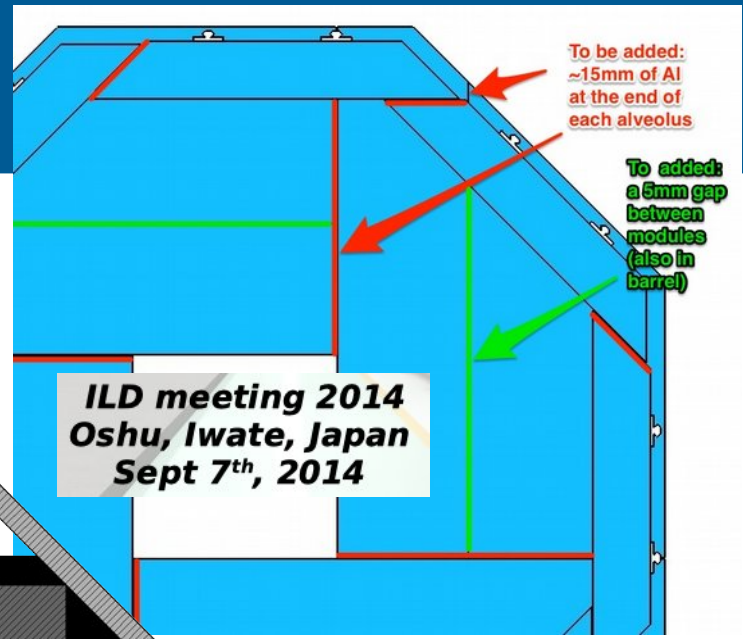
Back-up

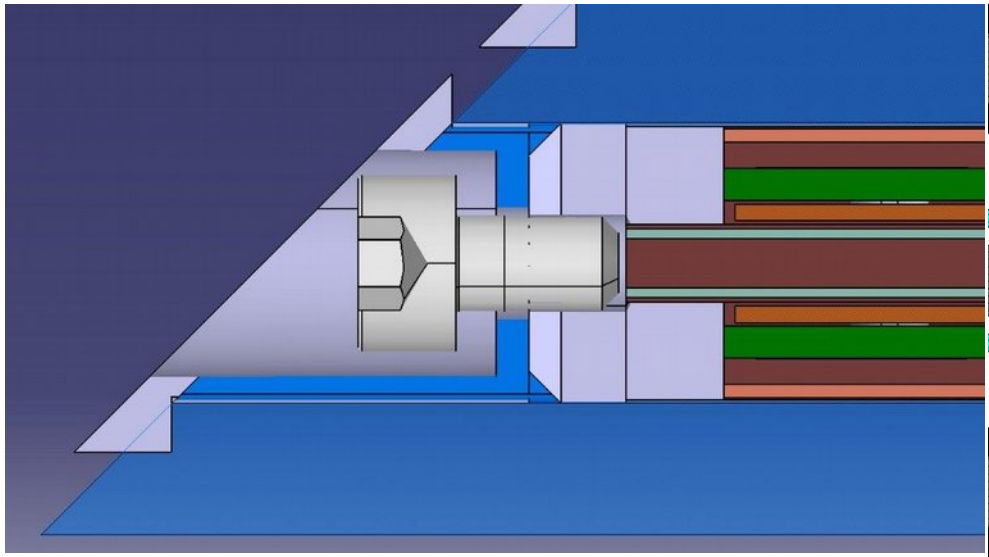
Slab plug

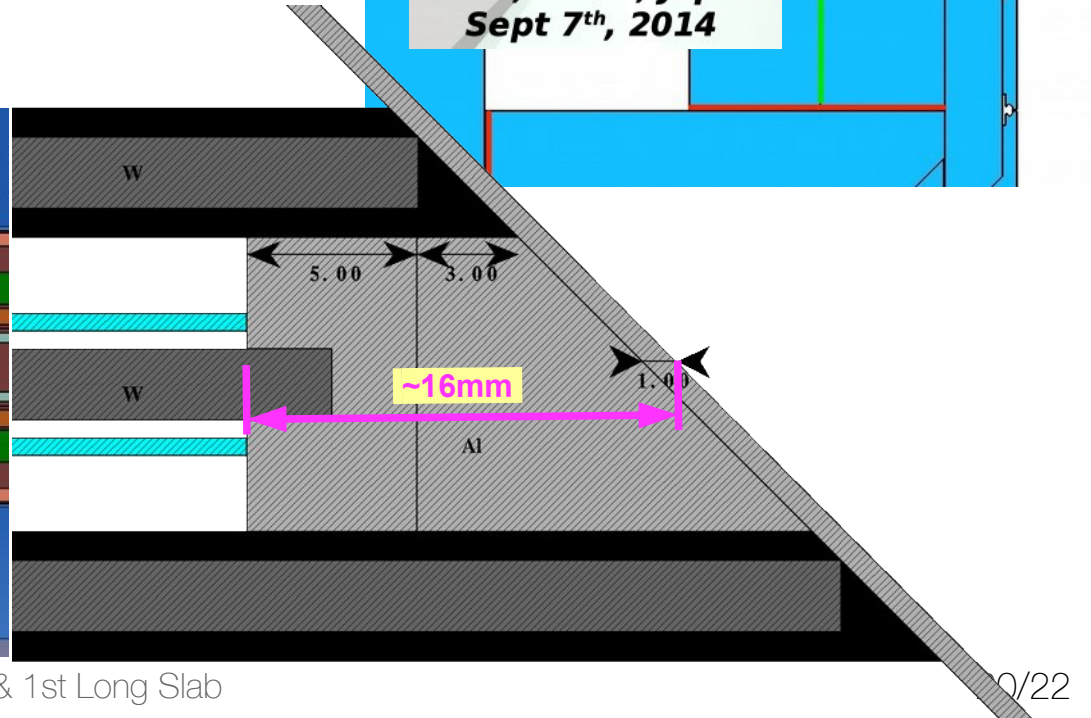
The slab plug is identical for both models.

On top of the TDD model an aluminium plate of 0.7mm has been added (simulation)

Example of realistic design (M.A.)





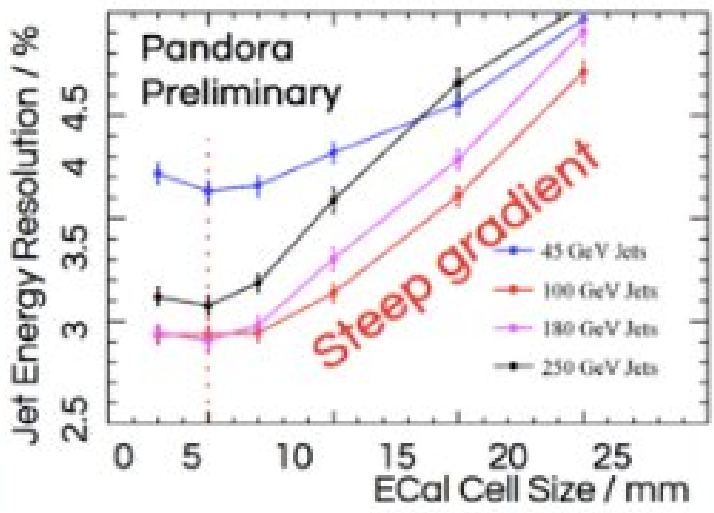


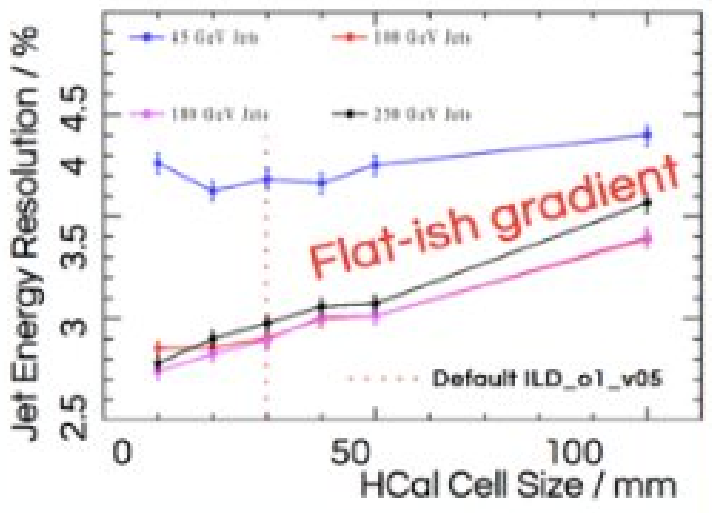
Sketch for a Historical Picture of the Progress of the ILD Silicon ECAL

Milestone	Date	Object	Details	REM
1st ASIC proto	2007	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	2010	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	2012	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	2015	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV10 & 11	7 units	
pre-calo	2017	FEV10 & 11	7 units	S/N ~ 20, 6–8 % masked
1st technological ECAL ?	2018	SLABvFEV10 & 11 & 13 SK2a+ COB + Compact stack	SK2 & SK2a (⊃timing)	Improved S/N Timing...

Optimal cell-size (DBD)

* Detector optimisation studies (Cambridge/DESY):





*See optimisation studies slides for reconstruction details.