VeloPix Readout and ASIC

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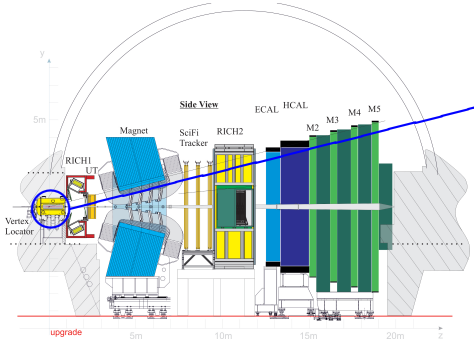
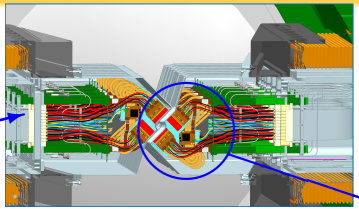
On behalf of the LHCb Velo Upgrade group

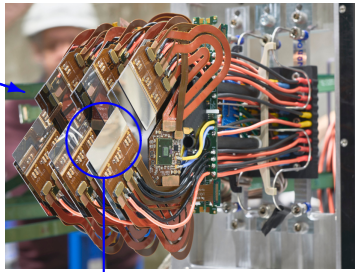
9th International Workshop on Semiconductor Pixel Detectors
for Particles and Imaging (PIXEL)

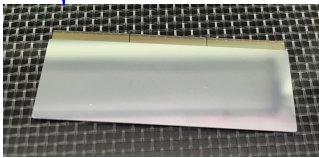
Taipei – December 12th, 2018

LHCb Velo Upgrade









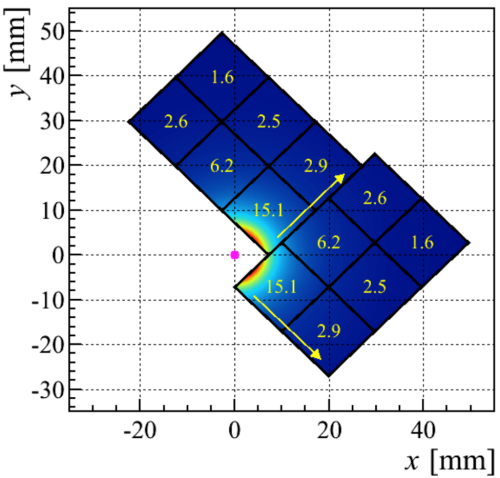
- Forward arm spectrometer dedicated to study of b- and c-hadron decays
- Vertex Locator (VELO) specialised in identifying secondary decay vertices
- Upgrade between 2019 and 2021 to triggerless read-out at 40MHz
- Replace VELO with new silicon pixel detector

See Also:
Talk The LHCb VELO Upgrade (D. Murray, Monday 10th, 14:10)
Poster Microchannel CO_2 cooling for the LHCb VELO Upgrade (O. De Aguiar Francisco)

Requirements for the new Read-Out ASIC

- Radiation Hardness
  - Closest active element is 5.1 mm from interaction region
  - Expected total ionising dose 400 Mrad
  - ... and 8×10^{15} 1 MeV neq/cm^2
  - Non-uniform fluency ($\propto r^2$)
  - Redundancy against single event effects
  - Operate with leakage current of 7nA/pixel at end of life
- High Data Rate
  - Average (Peak) rate of 600 (900) MHits/s
  - Hottest ASIC has rate of 15.1 Gbit/s
  - Timing resolution: 25 ns
  - Fast discharge to baseline: 16k e^- in 400 ns
- Hit efficiency of $> 99\%$
  - Qualified up to 1000 Volt bias current (in vacuum)
  - Signal-to-noise threshold: $\approx 1000\, e^-$
    (Sensor generates $\approx 7000\, e^-$ at end of life)
- Power consumption < 3 Watt

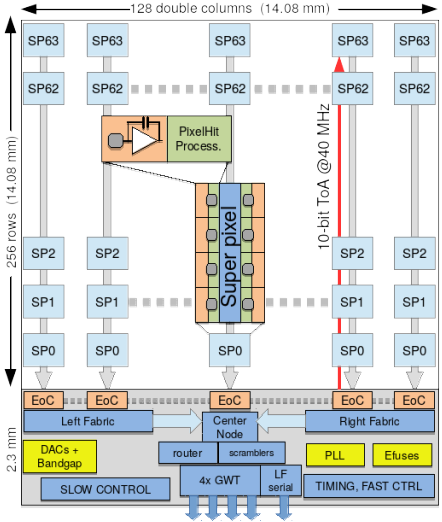
Data rate per ASIC (Gbit/s)



Introducing: The VeloPix

- Derived from TimePix/MediPix family
- 256×256 pixel matrix, with pixel size of $55 \times 55 \mu m^2$
- Implemented in 130nm CMOS
- *Super-Pixel* blocks
  - 8 pixels share common functionality
  - 30% reduction in data volume
- Column-wise read-out of super-pixels
- Routed to 4 high speed 5.12 Gbit/s serialisers
- Data-Driven Readout
  - Binary mode
  - Hits are time-stamped
  - Output is not time-ordered
- Power consumption ≈ 1.5 Watt

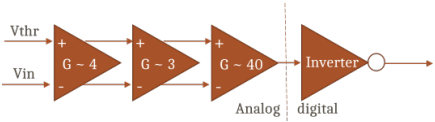
Design Overview

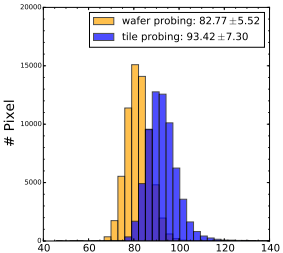


Pixel Block: Analogue Front-End

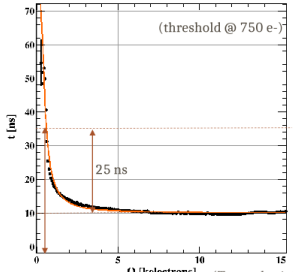
Main Components:

- Preamplifier with Krummenacher feedback loop for leakage current compensation
  - Average pixel noise at wafer probing [without sensor]: 83 e^- [ENC]
  - Average pixel noise at tile probing [with sensor]: 94 e^- [ENC]
- 3-tier cascade signal-to-noise discriminator
  - 2 low gain stages + 1 high gain stage
  - Designed to minimise time walk (signal must arrive within 25 ns)





pixel noise distribution



timewalk: signal arrival time as function of amount of electrons deposited

Pixel Block: Digital Front-End

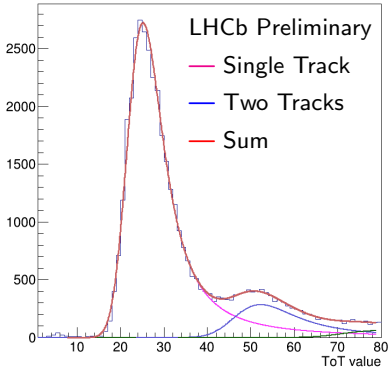
Main Components:

- Synchronisation logic to match discriminator output to 40MHz clock
- Linear feedback shift register
  - accessible through slow control interface
  - 6bit logic for every pixel
  - Three operation modes:

Configure: Specify Pixel configuration:
Test Pulse (1b) – Mask (1b) – Discriminator Setting (4b)

Hit counter: Binary read-out.
For example: used during threshold equalisation

TOT counter: Constant discharge current.
Monitoring charge collection and radiation damage



preliminary TOT scan result from testbeam

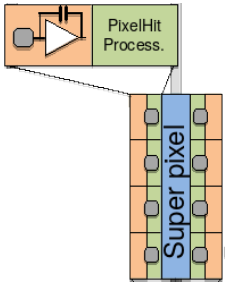
Super Pixel Concept

Super Pixels:

- Due to detector layout and pixel size, 55% of tracks have cluster size > 1 pixel
- Advantageous to combine information: Super Pixel
  - Groups 8 pixels together in 2×4 grid
  - Sharing address and time stamp information saves 30% data volume
  - 23bit Super Pixel Packet (SPP)

23b SPP	=	6b Address	9b Time Stamp	8b Hitmap

  - Sharing common logic blocks leads to more compact chip design



Column Bus Read-out:

- Super pixels are read-out top-down via shared bus
  - Node-based architecture
  - It takes at least 64 clock cycles for top SPP to reach End-of-Column
- Increased throughput, less power, less time-critical
- Increased latency: Readout time depends on position in column
- Arbiter allows fair-sharing of column bus
- Each super pixel as a FIFO buffer 2 events deep to minimise data loss
- Data transfer rate down the bus is 13.3 Mpackets/s

End-of-Column Fabric

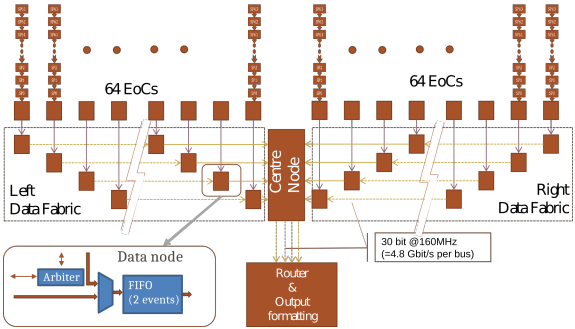
- Data from 128 columns needs to be merged into 1 output stream
- End-of-Column node adds 7bit column address to 23bit SPP

30b SPP	=	7b EoC Address	6b SP Address	9b Time Stamp	8b Hitmap

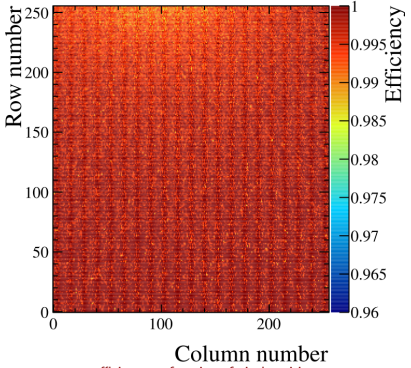
- 8 transfer lines transport SPPs to central router
  - Node-based architecture
  - A line connects to every 4th EoC node
  - Runs at 160 MHz, or 38.4 Gbit/s per line
- Router links all 8 lines to all 4 serialisers
  - When full bandwidth is not needed, serialisers can be disabled
- Output frame:

$$128\text{bit} = 8\text{bit header} + 4\times\ (30\text{bit SPP})$$

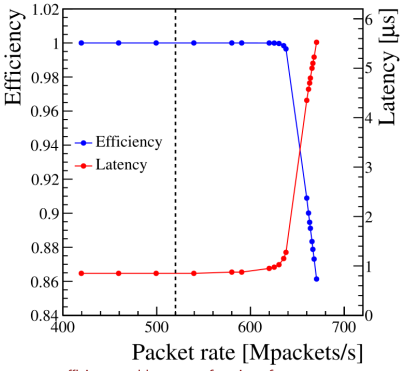
- Custom design "GWT" serialisers
  - "Gigabit Wireline Transmitter"
  - 5.12 Gbit/s throughput
  - Circuit runs at 320 MHz
  - Lower power consumption
  - Scramble data to balance 0's and 1's in stream



Data Rate Performance Studies



efficiency as function of pixel position



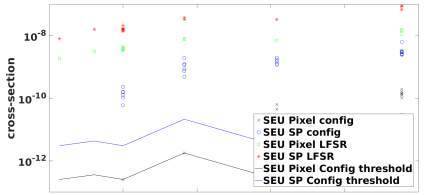
efficiency and latency as function of output rate

Simulation Studies

- Hottest ASIC can have local losses up to 1.6% in top of column
- Packet latency is less than 1 μs
- This is less than 512 clock cycles (max 9bit time stamp)
- Steep decline in performance when exceeding maximum bandwidth

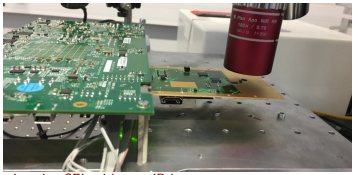
Radiation Tests

- State registers have triple redundancy against single event upsets (SEU)
  - . . . but data registers do not
- Extensive testing at Louvain [BE] heavy ion facility
- Also found single event latch-ups (SEL) in prototype design
  - Understood and corrected
- Total ionising dose tested up to 400 Mrad
  - No changes in operation observed

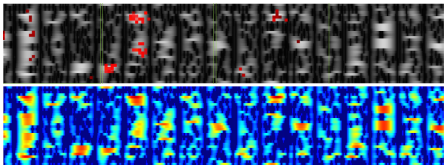


SEU probability split by register type

SEL in Prototype Design:



triggering SEL with near-IR laser



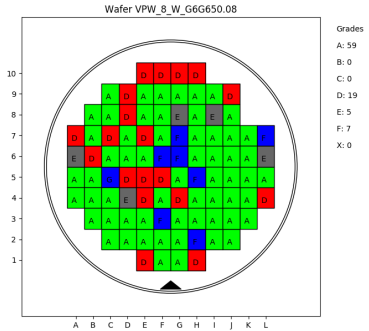
Observed SEL (Red points)
3μm Scan with near-IR laser

SEL susceptibility:
CAD prediction based on
Distance between contacts

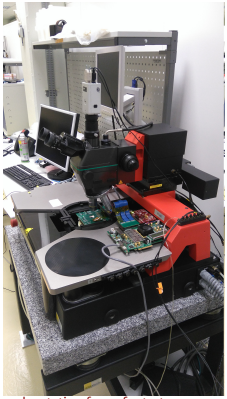
- SEL occurrences match regions with large distances between contacts
- This has been corrected in final VeloPix design

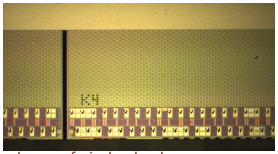
Production Steps

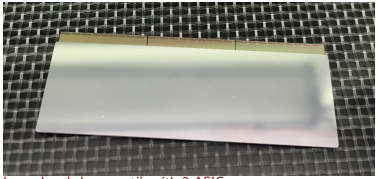
1. Wafer production
   - 91 ASICs per wafer
   - Yield = 60% (on 13 wafers)
   - 1 wafer tested per day
2. Bump-bonding [Advacam]
   - 3 ASICs are bump-bonded to single n-on-p sensor [Hamamatsu]
   - All wafer tests are repeated
   - Yield = ≈ 100% (on 170 Tiles)
   - First I/V scan to 1000 Volt (in vacuum)
   - Yield = ≈ 90%
3. Tiles are glued onto module and ASICs wire-bonded to hybrids

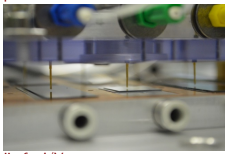


example wafer yield map

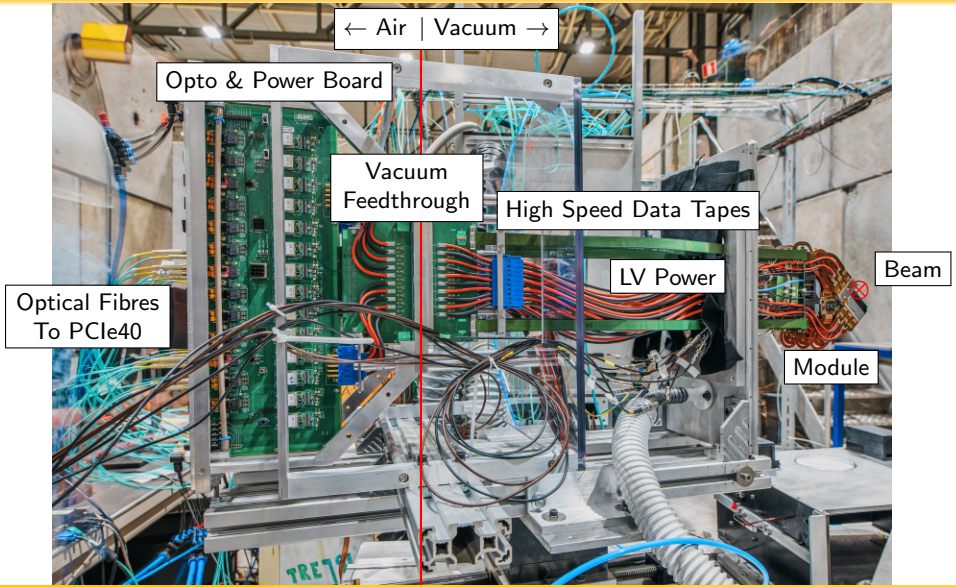

probe station for wafer test


close-up of wire-bond pads

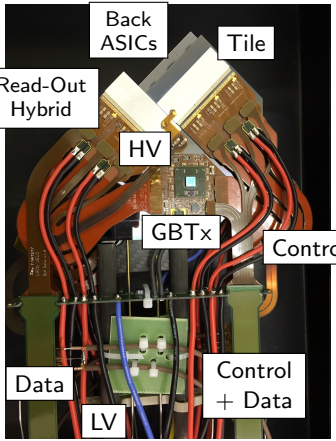

bump-bonded sensor *tile* with 3 ASICs


jig for I/V scan

Prototype Read-Out Chain at CERN North Area Testbeam

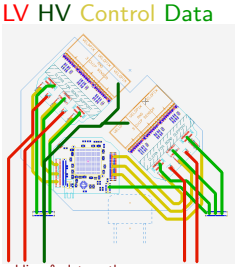


The VeloPix Module

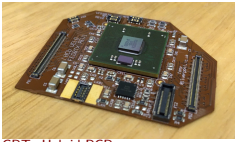


Components:

- Silicon microchannel substrate
  - Low material budget, match thermal expansion
- 4 n-on-p sensor *tiles*
- 12 VeloPix Asics
- 2 GBTx Hybrid PCBs for signal fan-out to VeloPix
- 2 bidirection slow control links (4.8 Gbit/s)
  - Configuration, Monitoring, Timing, Control
- 20 unidirectional high speed data links (5.12 Gbit/s)
- Double sided



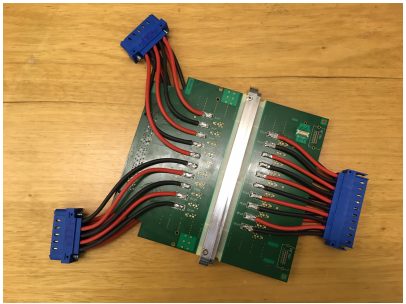
cabling & data paths


GBTx Hybrid PCB

From Module to Fibre

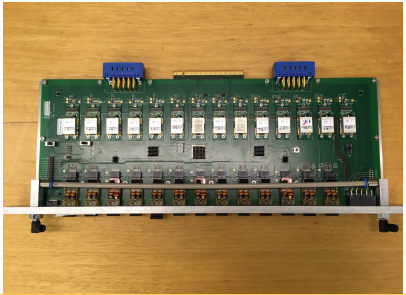
Vacuum Feedthrough Board (VFB)

- Transmits control & high speed signals, temperature monitoring, LV and HV between Module (vacuum side) and OPB (air side)
- High speed data tapes connect VFB with module



Opto- & Power Board (OPB)

- Provides low voltage to all components in read-out chain
  - Radiation hard FEASTMP DC/DC converters
- Converts signals: Electrical $\leftrightarrow$ Optical
  - 3 bidirectional links (VTRx)
  - 20 unidirectional links (VTTx)
- Controlled via GBTx and SCA
  - GigaBit Transceiver and Versatile Link Projects

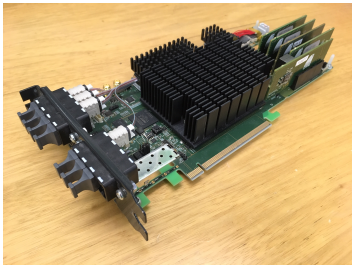


From Fibre to Event

The PCIe40 Read-Out Card

- Common off-detector hardware for data processing of all LHCb subdetectors
- Intel Arria 10 FPGA
- Two firmware flavours

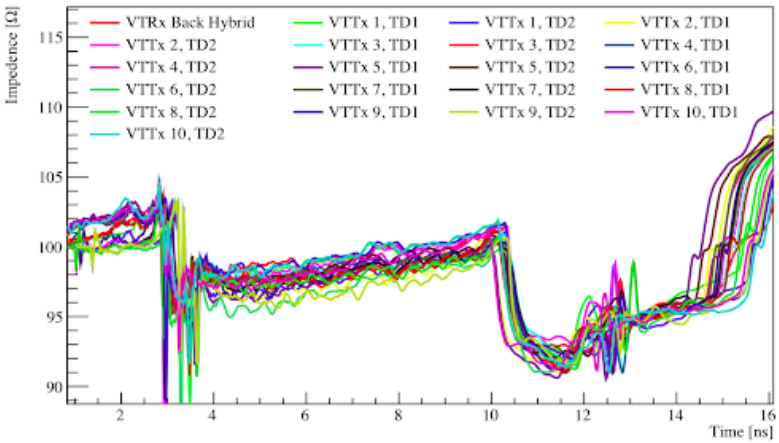
  Slow Control: 1 per 13 Modules (4 total)
  High Speed DAQ: 1 per Module (52 total)
- DAQ: Maximum throughput 100 Gbit/s



The VELO-Specific DAQ Firmware

- Unique data protocol (5.12 Gbit/s GWT link, super-pixel packages)
- Will do descrambling and time-ordering of SPP
  (based on LHC bunch crossing ID)

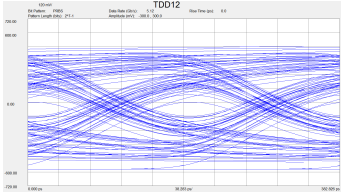
Transmission Line Impedance



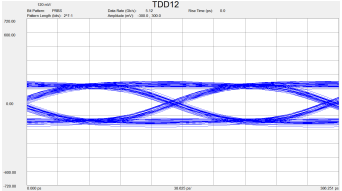
Data Tapes	VFB	OPB

Performance of the Data Links

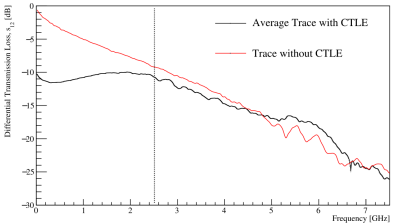
The Need for a CTLE Circuit:



eye diagram without CTLE [PRBS7 – data path only]

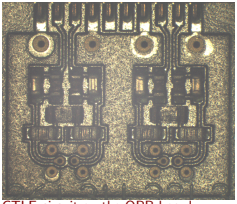


eye diagram with CTLE [PRBS7 – data path only]



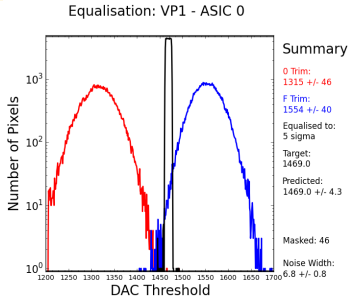
signal attenuation versus frequency

- Passive CTLE circuit added on data links to improve transmission quality
- More uniform attenuation up to Nyquist Frequency (2.56 GHz)
- At the cost of reduced differential swing
- Jitter from VeloPix leads to poor eye diagram
  - Improved design between prototype and final version
- BER on high speed data links lower than few 10^{-14}

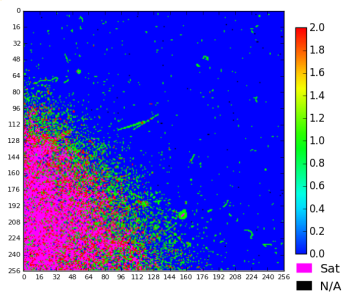


CTLE circuit on the OPB board

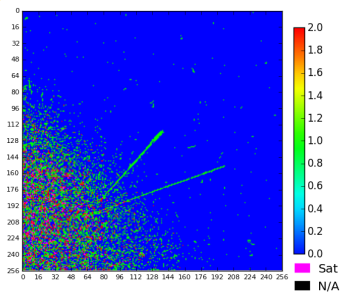
First Prototype Modules at CERN North Area Testbeam



example threshold scans for equalisation of pixel matrix



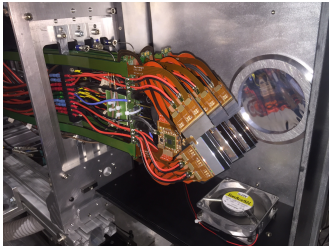
first data with proton beam over slow control link



first data with proton beam over GWT link

Testing the DAQ Chain:

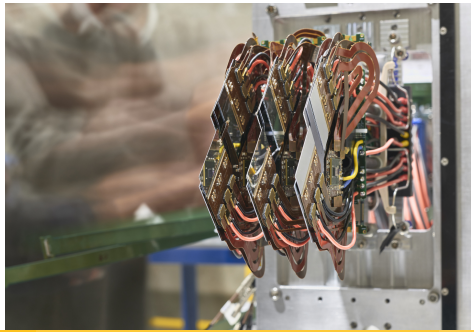
- Demonstrate control and configuration of VeloPix
- 3 modules running synchronously with TimePix3 telescope
- Successful test of the DAQ read-out chain
- Correlations in time and space, but further analysis ongoing



test setup with beam window

Summary

- VeloPix: Radiation hard, high data rate silicon pixel ASIC for the upgraded LHCb Velo detector
- Key numbers:
  - $55 \times 55 \mu m^2$ pixel size
  - 400 Mrad total ionising dose
  - 15.1 Gbit/s output rate
  - 25ns time-stamping resolution
- High speed read-out chain has been validated, ready to start production



Glossary

CTLE:	Continuous Time Linear Equaliser	
EoC:	End-of-Column	
GBTx:	Gigabit Transceiver FPGA	[GBT Project]
GWT:	Gigabit Wireline Transmitter (Serialiser)	
HV:	High Voltage	
LET:	Linear Energy Transfer	
LV:	Low Voltage	
OPB:	Opto- & Power Board (part of VELO read-out chain)	
PCB:	Printed Circuit Board	
PCIe40:	Custom 40MHz read-out card based on PCI express transfer bus	
SCA:	GBT – Slow Control Adaptor/ASIC	[GBT Project]
SEL:	Single Event Latch-up	
SEU:	Single Event Upset	
SPP:	Super-Pixel Packet	
TOT:	Time-over-threshold	
VELO:	Vertex Locator	
VFB:	Vacuum Feedthrough Board (part of VELO read-out chain)	
VTRx:	Versatile TransReceiver (electrical-optical conversion)	[Versatile Link Project]
VTTx:	Versatile Twin-Transmitter (electrical-optical conversion)	[Versatile Link Project]