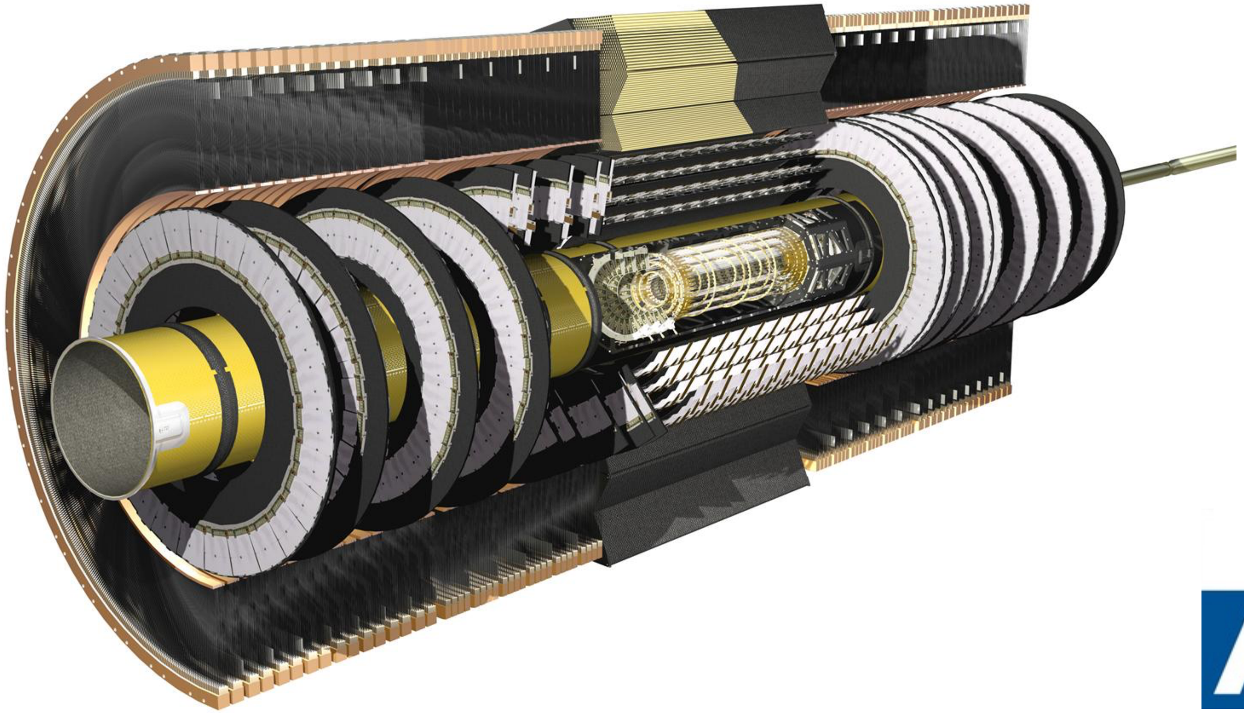
Operational Experience of the ATLAS SCT and Pixel Detector

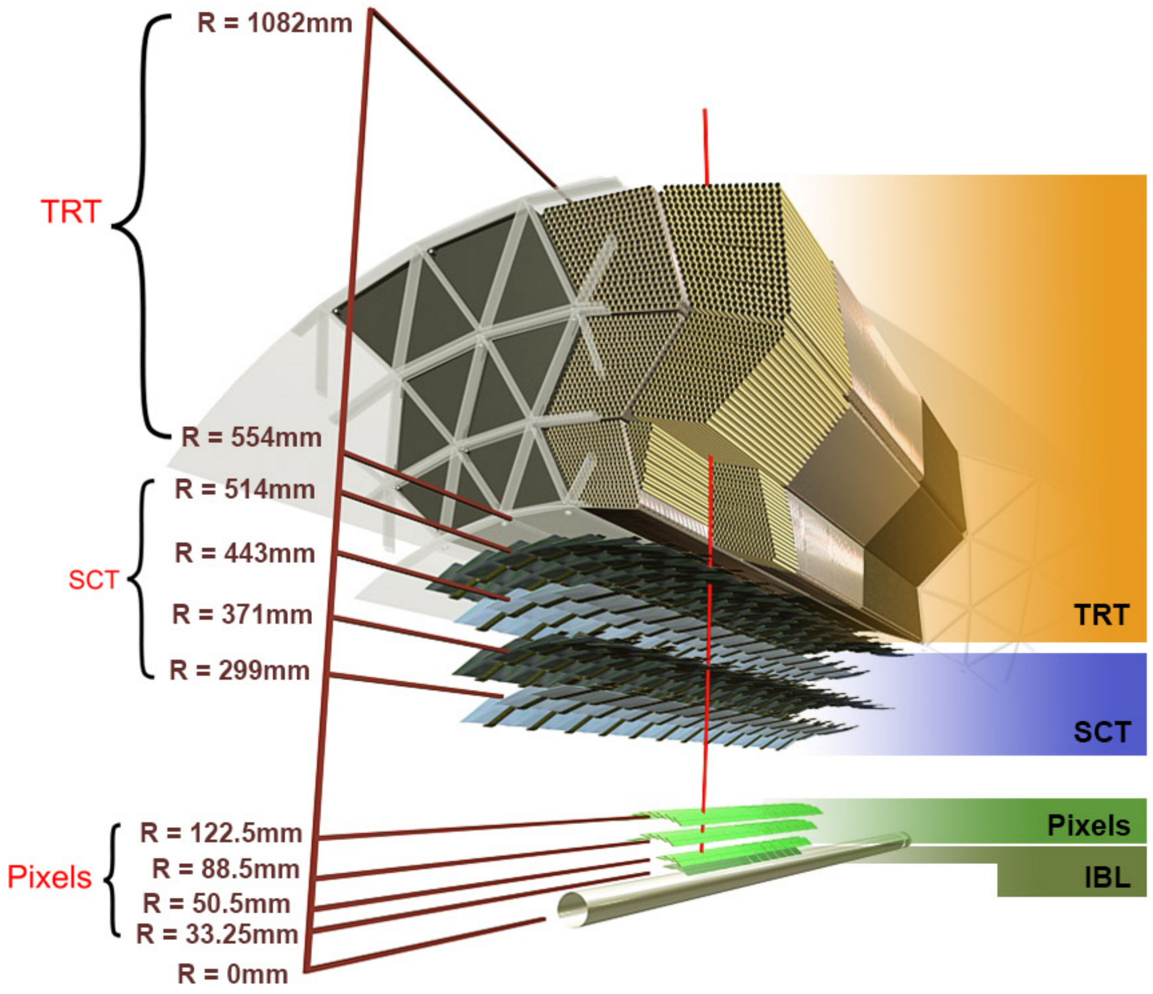
Hard working operations team



Kathrin Becker (Freiburg) on behalf of the ATLAS collaboration

Vertex 2018, October 22, 2018

The ATLAS Inner Detector

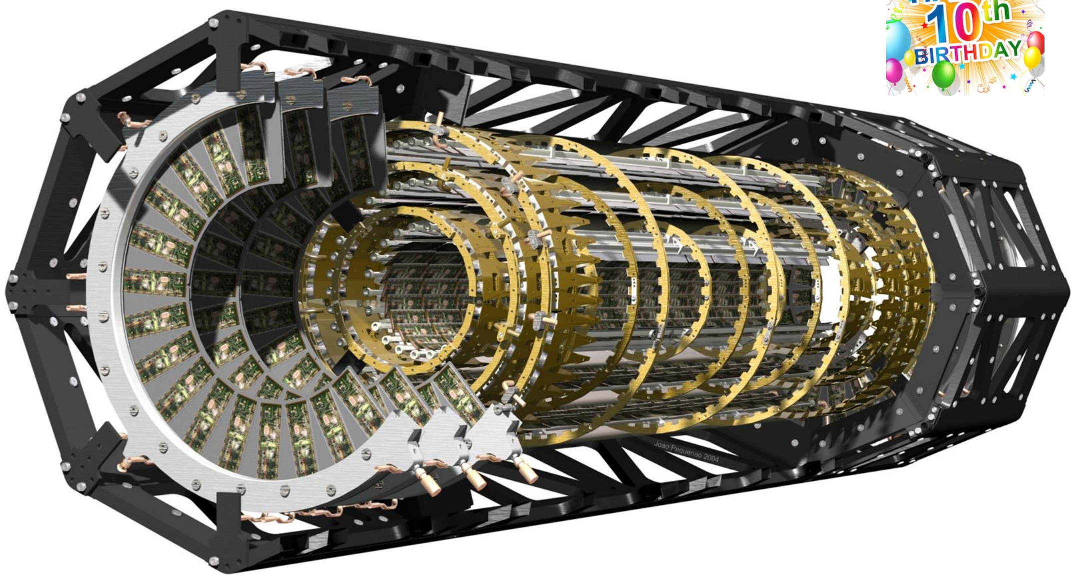


- *Transition Radiation Tracker (TRT):*
  - 350000 channels
  - 130 µm resolution
  - 4 mm element size
- *Semi Conductor Tracker (SCT):*
  - 6.3 million channels
  - 17 x 570 µm resolution
  - 130 µm x 12 cm element size
- *Pixel detector/Insertable B-Layer (IBL):*
  - 92 million channels (80/12)
  - 10 x 115 µm / 8 x 40 µm resolution
  - 50 µm x 400 µm/250 µm element size

Focus on Silicon detectors

The Pixel Detector

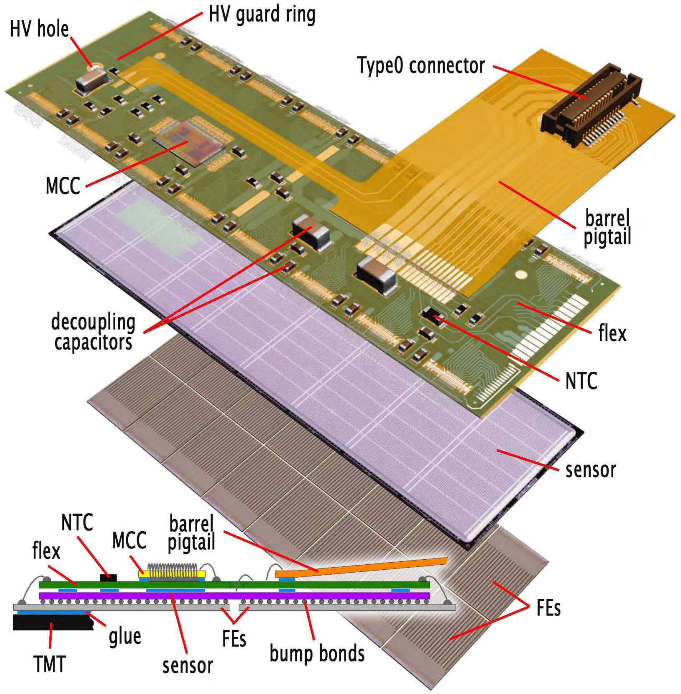
- 3 hit system up to angular coverage of $|\eta| < 2.5$
- 3 barrels and 2 x 3 endcap disks
- C_3F_8 evaporative cooling
- 1.7 m^2 of silicon
- 1744 pixel modules



Each pixel module consists of:

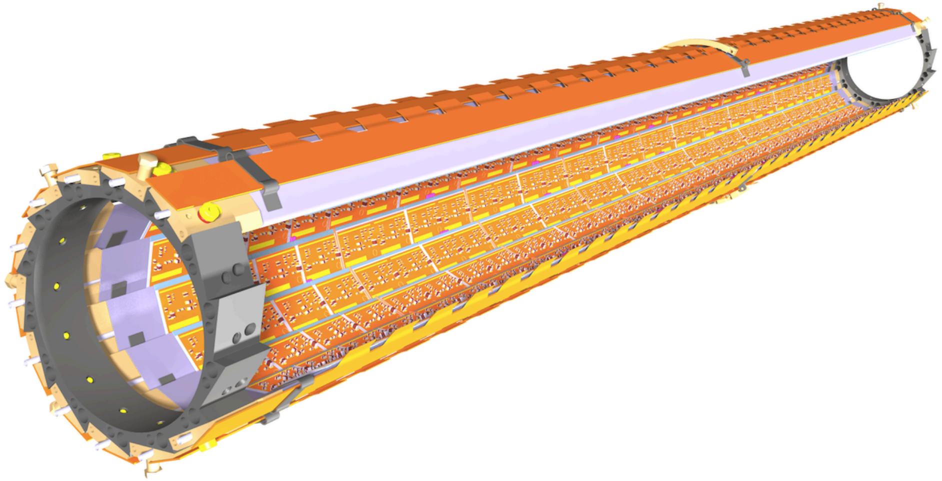
- 1 planar n-on-n sensor 60.8 x 16.4 mm active area, 250 µm thick, 46080 pixels
- 16 FEI3 front-end chips plus one controller (0.25 µm CMOS)
  - Front-ends are bump-bonded to the sensor.
  - Charge measurement using 8-bit ToT information.
- 1 flex that provides electrical connections
- Data rate per module: 40/80/160 Mbps

Radiation-hard
1×10^{15} MeV n_{eq} cm^{-2}
50 Mrad



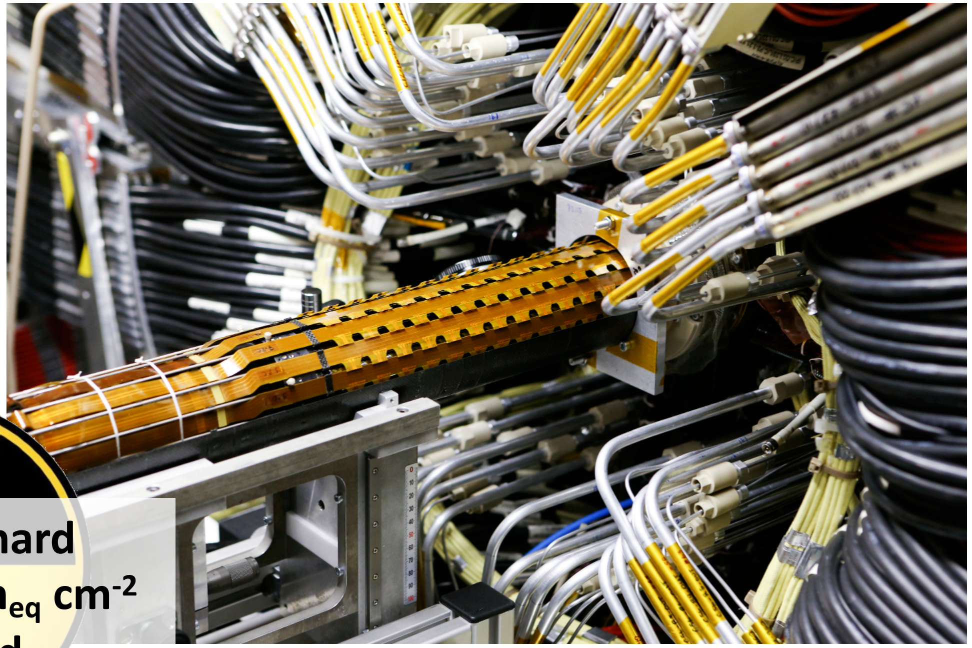
IBL – Insertable B-Layer

- Innermost layer of the pixel detector, coverage of |η| < 3
- New in LHC Run 2, installed in 2014
- 14 staves, 0.2 m^2 of silicon
- CO_2 evaporative cooling
- 280 IBL modules
- Planar sensors (central) and 3D sensors (forward)



Each IBL module consists of:

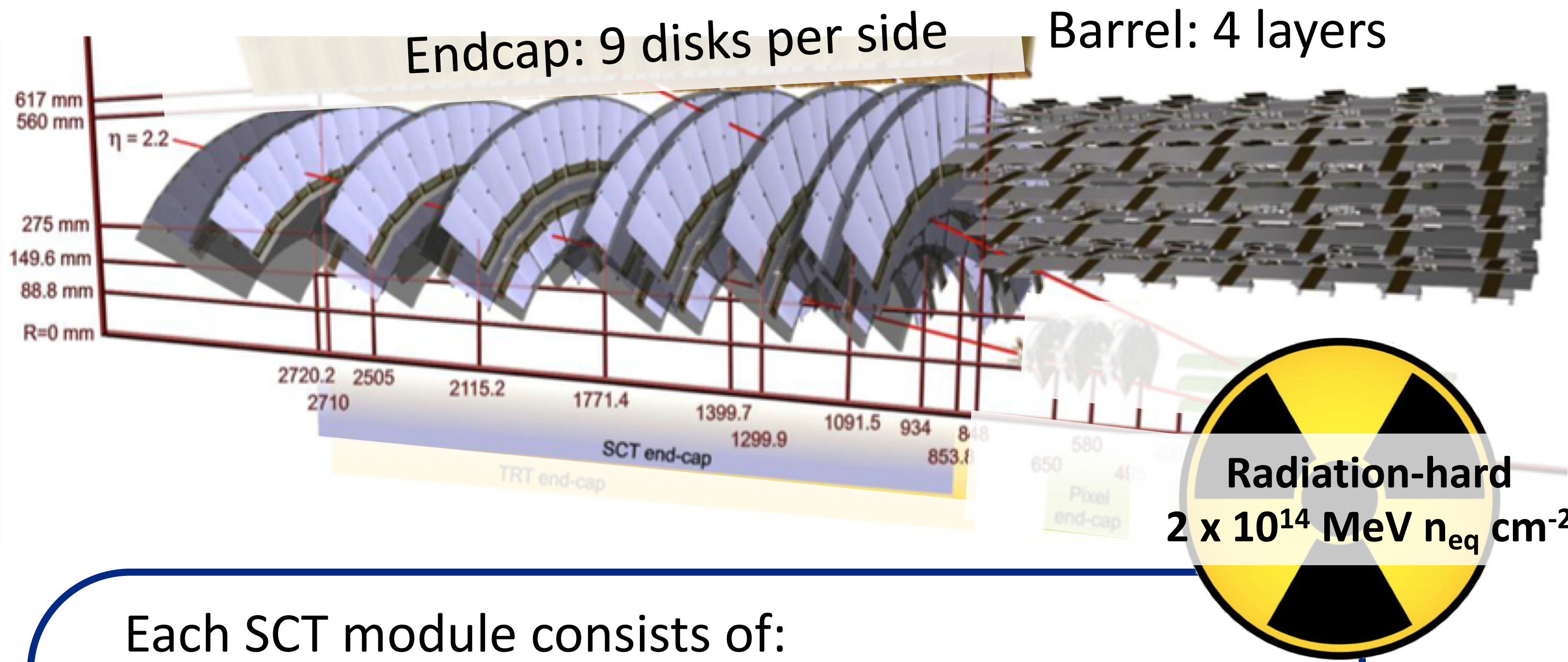
- Sensor:
  - Planar slim edge n-on-n sensor, 200 μm thick
  - 3D n-on-p sensor with 2 electrodes per pixel, 230 μm thick
- 2 or 1 FEI4 front-end chips (0.13 μm CMOS)
  - Front-ends are bump-bonded to the sensor.
  - Charge measurement using 4-bit ToT information
- 1 flex that provides electrical connections
- Data rate: 160 Mbps

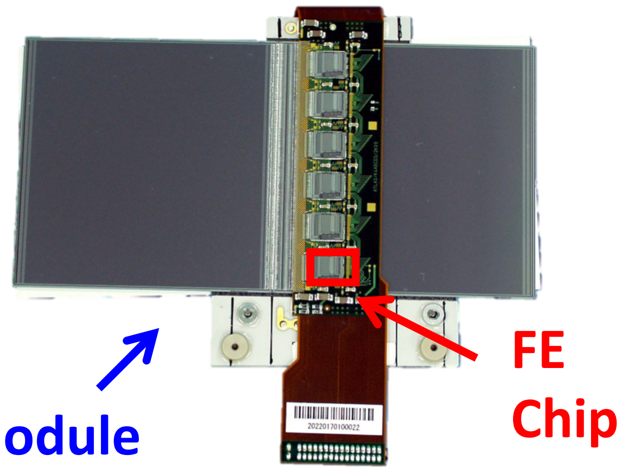


Radiation-hard
5 x 10^{15} MeV n_{eq} cm^{-2}
250 Mrad

SCT- Semi Conductor Tracker

- 8 hit system
- Angular coverage: $|\eta| < 2.5$
- C_3F_8 evaporative cooling
- 61 m^2 of silicon
- 4088 modules

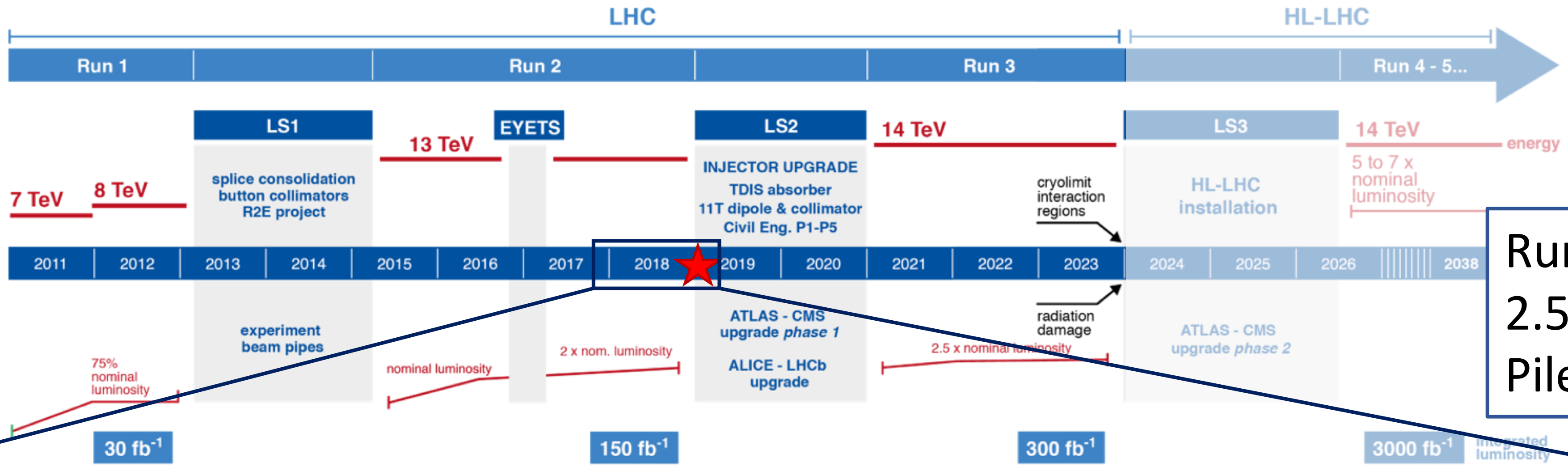




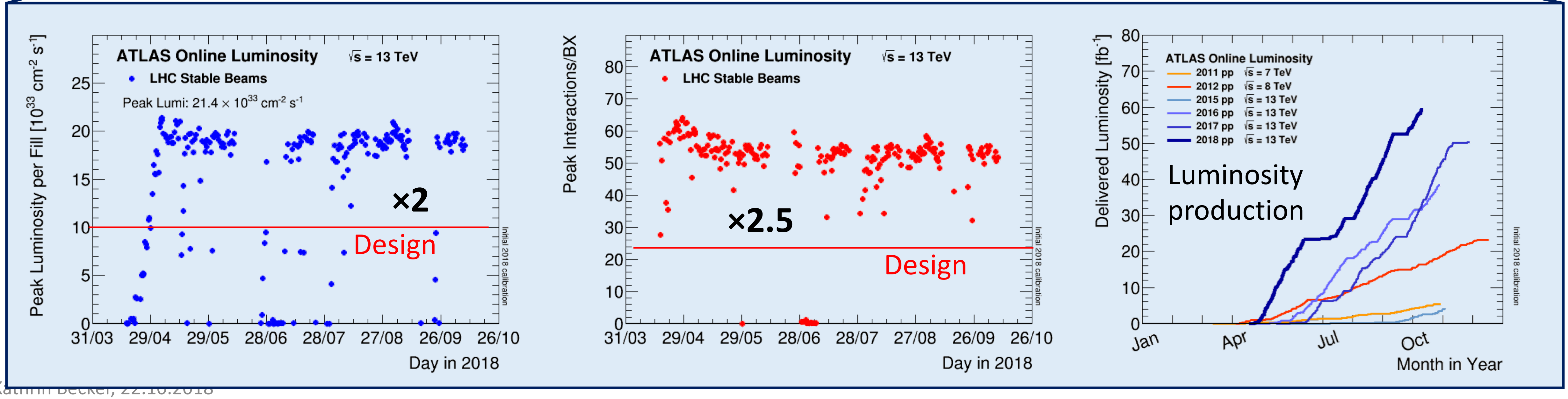
Each SCT module consists of:

- Two strip sensors crossing at 40 mrad
- Single-sided p-in-n sensor, 285 µm thick, 768 strips
- 2 x 6 ABCD front-end chips (0.8 µm biCMOS)
  - Binary readout: hit = signal > threshold
  - 3 consecutive time bins sampled per trigger
- Data rate: 40 Mbps

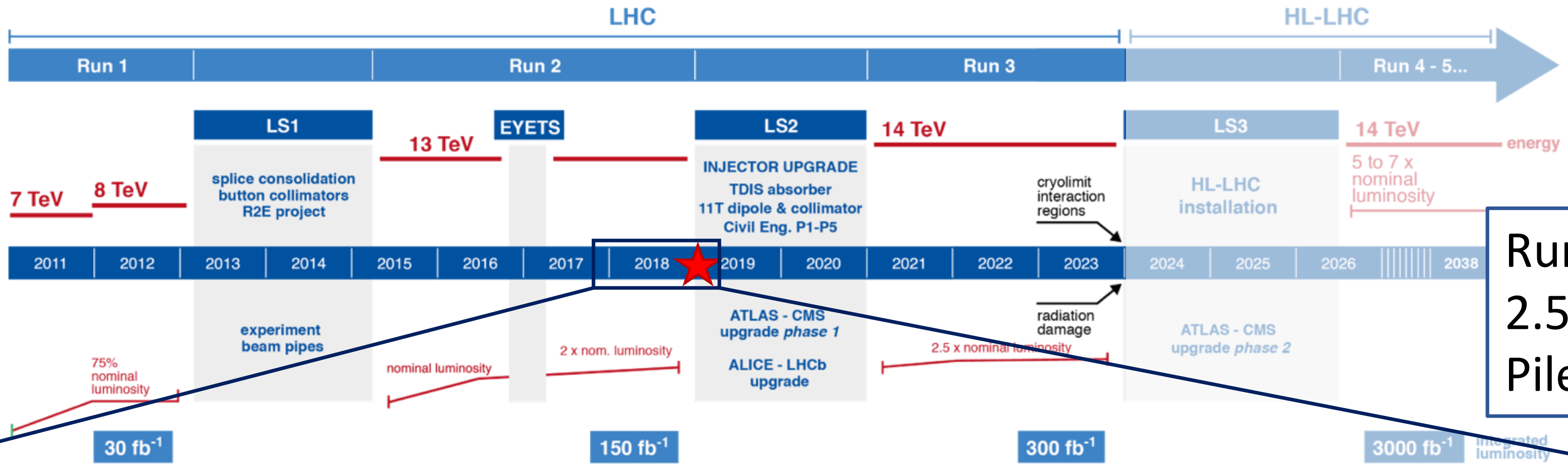
LHC Roadmap and Performance in 2018



Run 3 prediction:
2.5 x 10^{34} cm^{-2} s^{-1}
Pile-up: μ = 61.5



LHC Roadmap and Performance in 2018

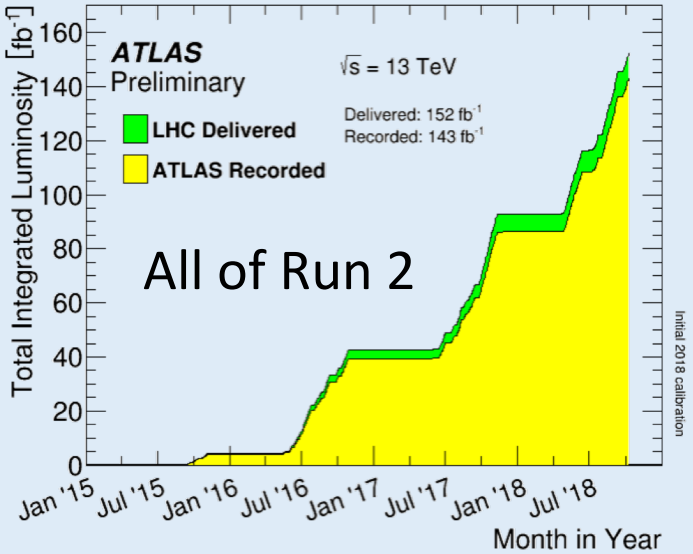


Run 3 prediction:
2.5×10^{34} cm^{-2} s^{-1}
Pile-up: $\mu = 61.5$

→ LHC performs superbly well above design specs

Operational challenges:

- Bandwidth: Tackled mainly in 2017
- Radiation dose:
  - Radiation damage
  - Impact of Single-event upsets (SEU)



ATLAS Silicon Trackers in 2018

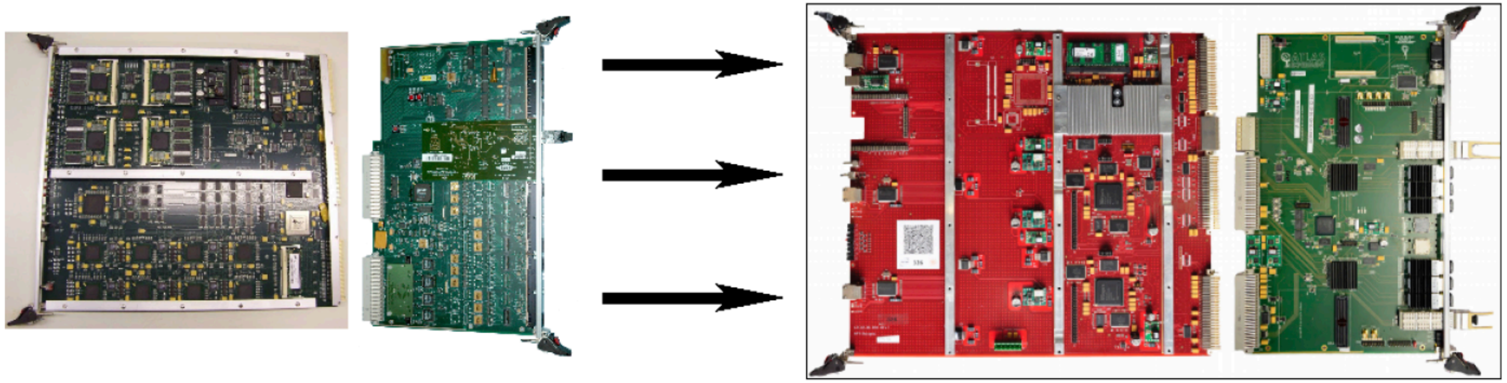
- Detectors in great shape, even after 10 years!
- Operational fraction:
  - IBL: 99.3%
  - Pixel: 94.9%
  - SCT: 98.6%

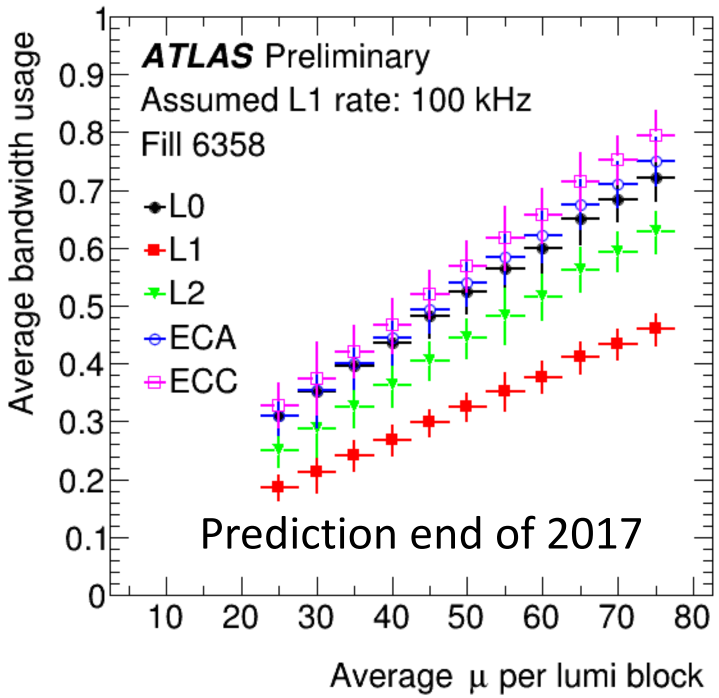
ATLAS pp data: April 25-September 10 2018											
Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
99.7	99.7	100	99.5	100	99.8	99.7	100	100	100	99.5

- 2018 has been the most intense luminosity production year yet…
  … Pixel/IBL and SCT have become even better!!
- Deadtime is at 0.15% for Pixel/IBL and 0.09% for SCT
  → Improved with respect to previous years due to continuous improvements in firmware and DAQ
- High quality data (99.7%)

→ Made possible by diligent efforts by the respective operation teams

Bandwidth extension - Pixel





Upgrade Pixel Readout to IBL Readout system

Layer	Old rate	New rate	Intervention
Layer 2	40 Mbps	80 Mbps	WS 2015/2016
Layer 1	80 Mbps	160 Mbps	WS 2016/2017
Layer 0	160 Mbps	160 Mbps	WS 2017/2018
Disks 1,3	80 Mbps	80 Mbps	WS 2017/2018
Disks 2	160 Mbps	160 Mbps	WS 2017/2018

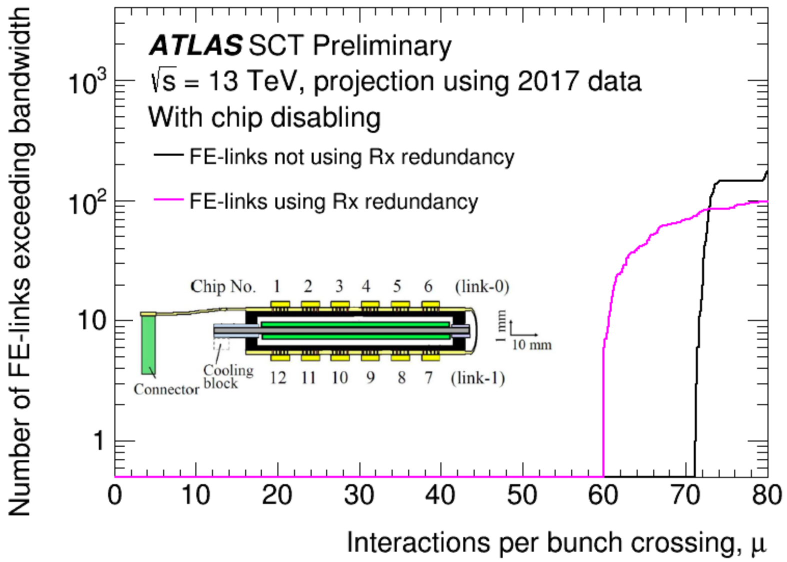
In 2018 unification of the Readout system brings operational advantages regarding maintenance and developments

All layers expected to have < 70% bandwidth usage at 100 kHz trigger rate for μ = 61.5!

→ Good for Run 3!

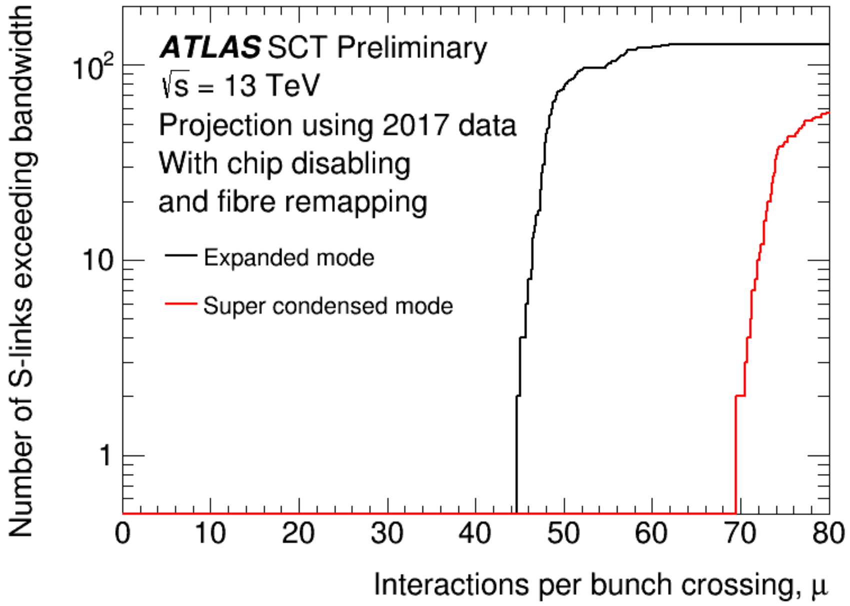
Bandwidth strategy - SCT

Redundancy = readout all 12 chips via one link



1. Front-end links limit

- If no redundancy in readout
  → safe for Run 2 and Run 3
- In case of redundancy apply chip masking to avoid module-wide error
  → avoid “double hole” impacting efficiency



2. S-Link

- Remapping fibres in 2017 to optimize bandwidth usage
- Running per default in Supercondensed mode
  → safe for Run 2 and Run 3
- Pile-up of 70 is a hard limit. Fine, if LHC does not over-perform in Run 3

Radiation Damage – Impact on Operations

- Leakage currents
- Depletion voltage
- Charge collection
- Noise & gain

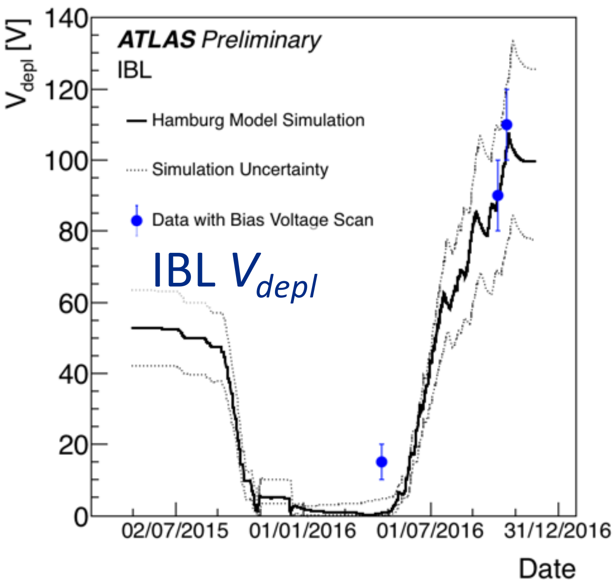
} Addressed via static configurations, e.g. determined by calibration or by collision data

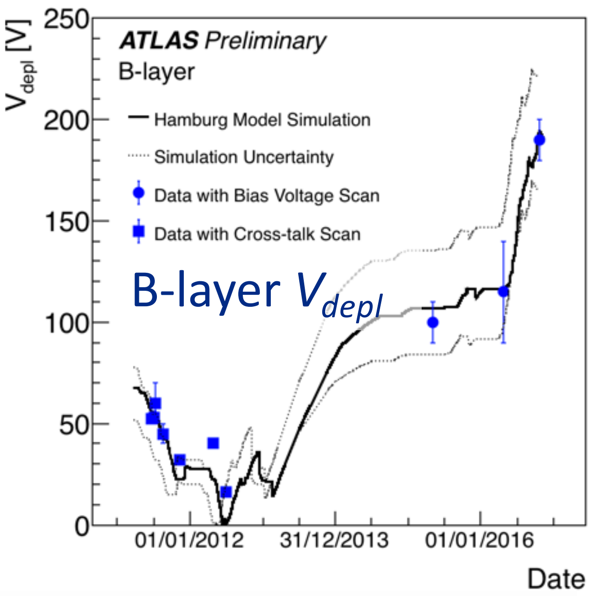
- Single Event Upsets (SEU)
  - Rate is function of instantaneous luminosity

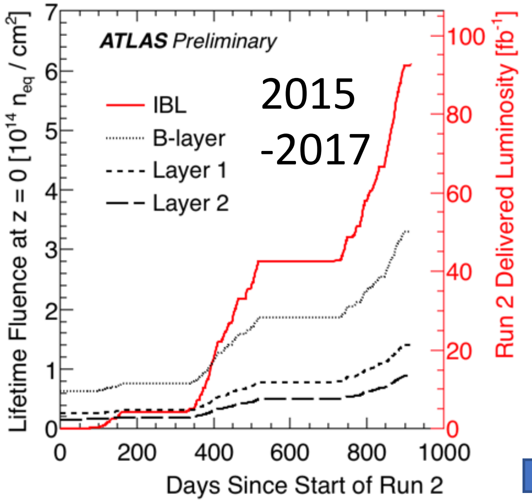
→ Addressed on-the-fly during an LHC run

Modelling of radiation damage

- Assess radiation damage of Pixel/IBL and SCT to project long-term health
- Increase in $\boldsymbol{V_{depl}}$ and $\boldsymbol{I_{leak}}$
- Good agreement with the "Hamburg" model and "Sheffield-Harper" model



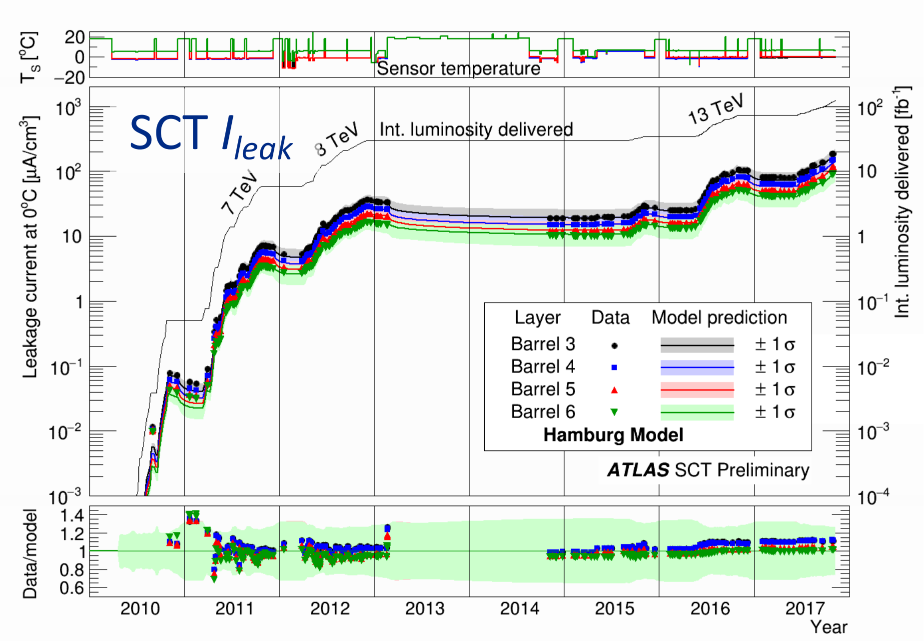




	End of Run 2 [MeV n_{eq} cm^{-2}]	Limit [MeV n_{eq} cm^{-2}]
IBL	~9 x 10^{14}	5 x 10^{15}
B-Layer	~4.5 x 10^{14}	1 x 10^{15}

B-layer extrapolated from 2017

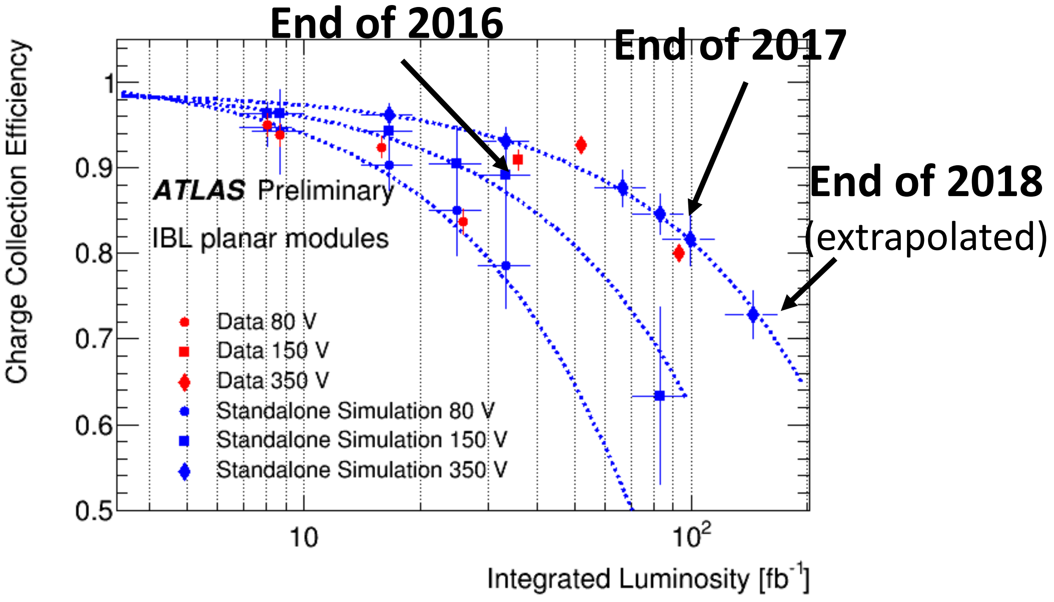
IBL has room until limit
B-Layer possibly already at >40% of its dose

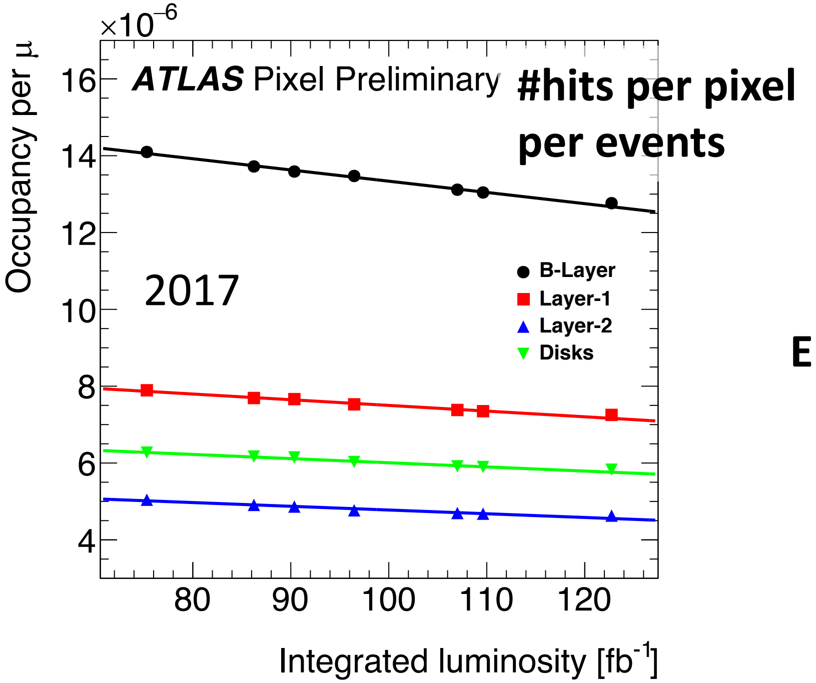


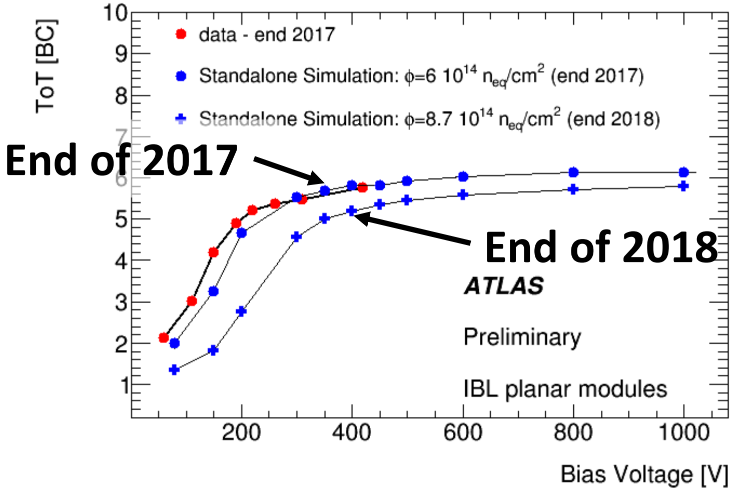
Radiation effects on charge collection

Pixel hit occupancy per unit of μ

- Observe decrease as function of integrated luminosity
- Caused by drop in charge collection efficiency and decrease of time over threshold (ToT)
- Cause is charge trapping in pixel sensor







Operational measures

- Increase the HV
- Decrease the thresholds
  → Interplay with bandwidth
- Set per production year

Changes in operational parameters

Run 2 Bias Voltage Evolution:

- **Ensure detectors are fully depleted**
- Regular increase in IBL and B-layer
- 2018: First increases for Layer-2, Disks and SCT Barrel 3

Layer	2015	2016	2017	2018
IBL	80 V →	150 V →	350 V →	400 V
B-layer	250 V →	350 V	350 V →	400 V
Layer-1	150 V →	200 V	200 V →	250 V
Layer-2	150 V	150 V	150 V →	250 V
Pixel disks	150 V	150 V	150 V →	250 V
SCT Barrel 3	150 V	150 V	150 V	150 V → 200 V

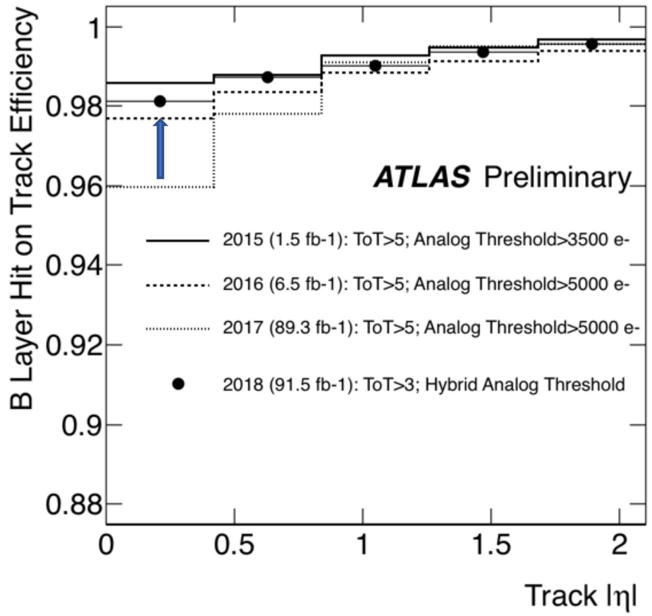
Layer	2017	2018
IBL	2500e, ToT>0	2000e, ToT>0
B-layer	5000e, ToT>5	4300e*, ToT>3
Layer-1	3500e, ToT>5	3500e, ToT>5
Layer-2	3500e, ToT>5	3500e, ToT>5
Pixel disks	4500e, ToT>5	3500e, ToT>5

* central eta: 4300e, forward eta: 5000e

Threshold evolution

- **Recover charge efficiency degradation**
- Threshold lowered for IBL, B-layer, and disks

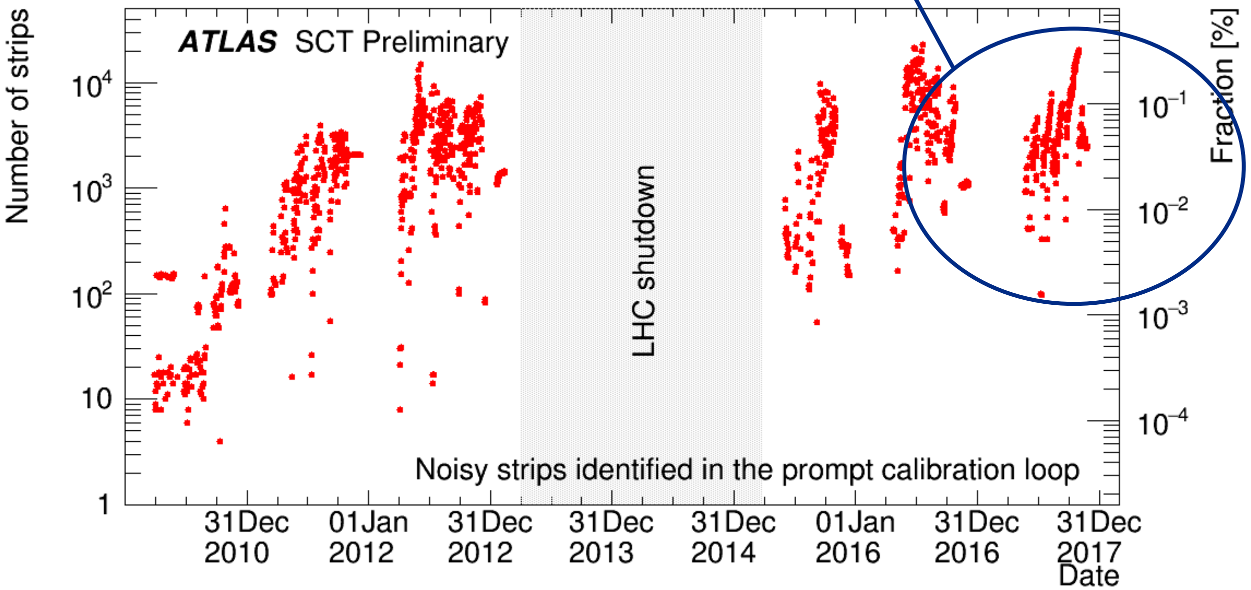
→ 2018 config as efficient as 2015 config

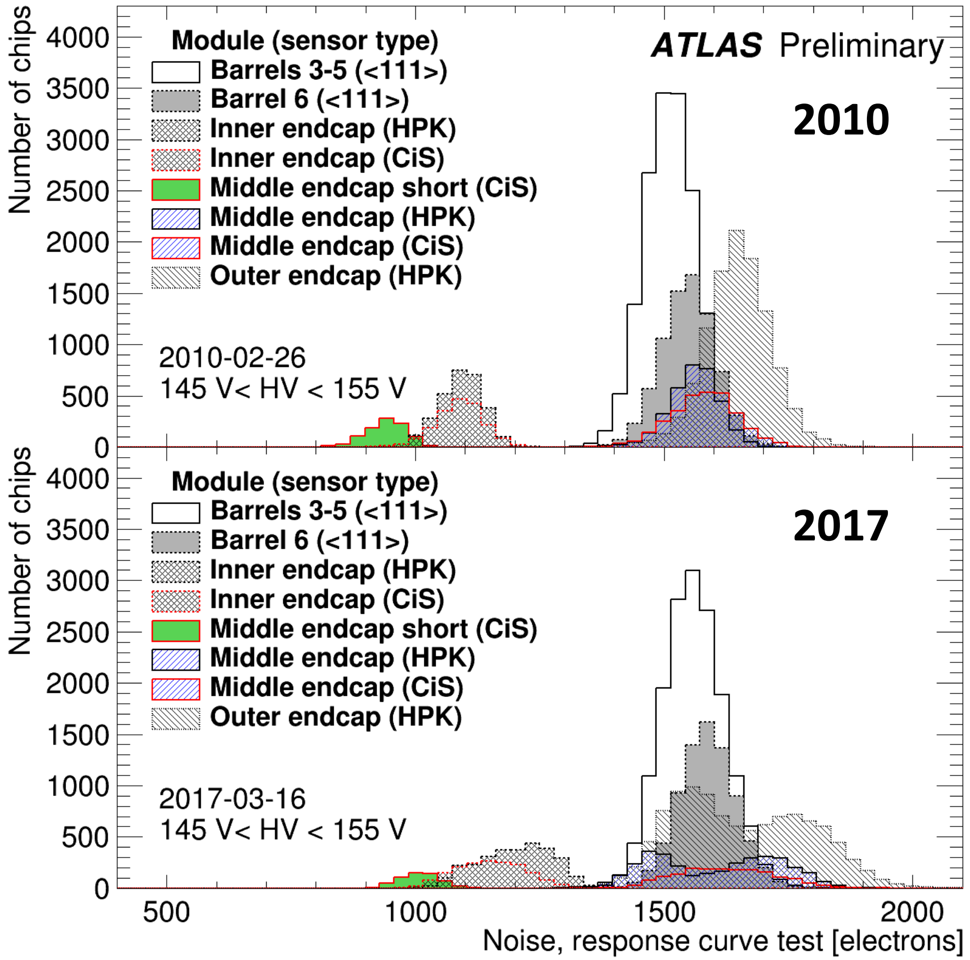


Noise – Example SCT

- Noise in SCT stable over the years
- Stability ensured by regular calibrations shifting the threshold

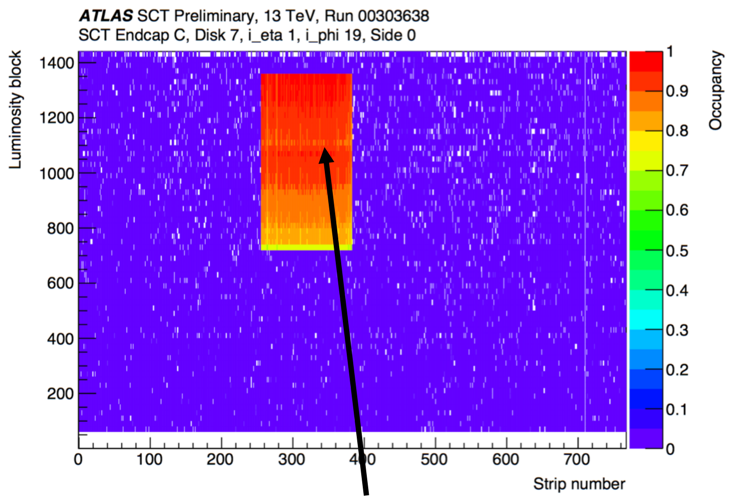
Frequent steps in noisy channel counts due to calibration results applied



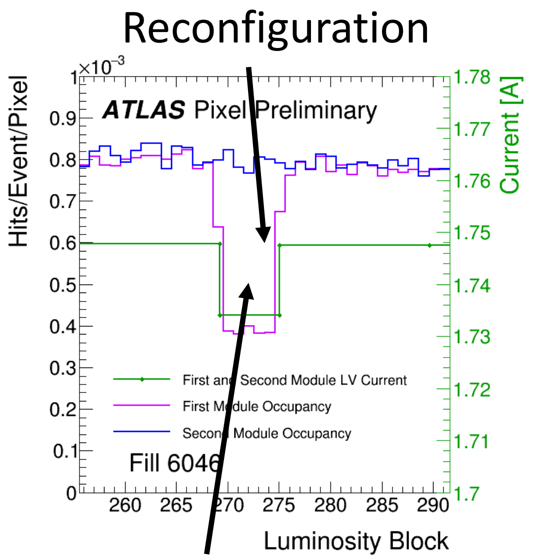


Single Event Upsets in front-end chips

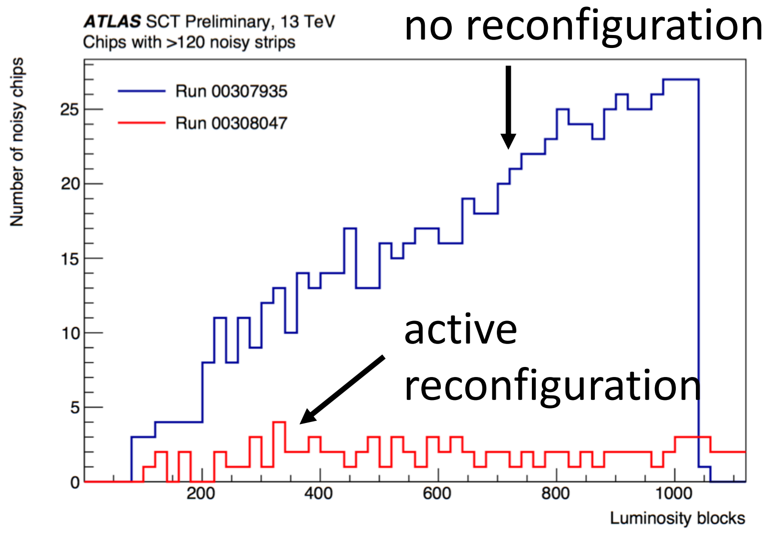
- Registers in Pixel/IBL have triple redundancy and majority logic to protect against SEU.
  SCT has no protection.
- SEU in front-end chip observed for IBL and SCT
  - SEU → change in configuration
  - Decrease or increase in occupancy
- Mitigation: Chip reconfiguration
  - SCT: every 90 lumiblocks (1 per hour)
  - IBL: every 5s at reset of L1 ID → no increase of busy time



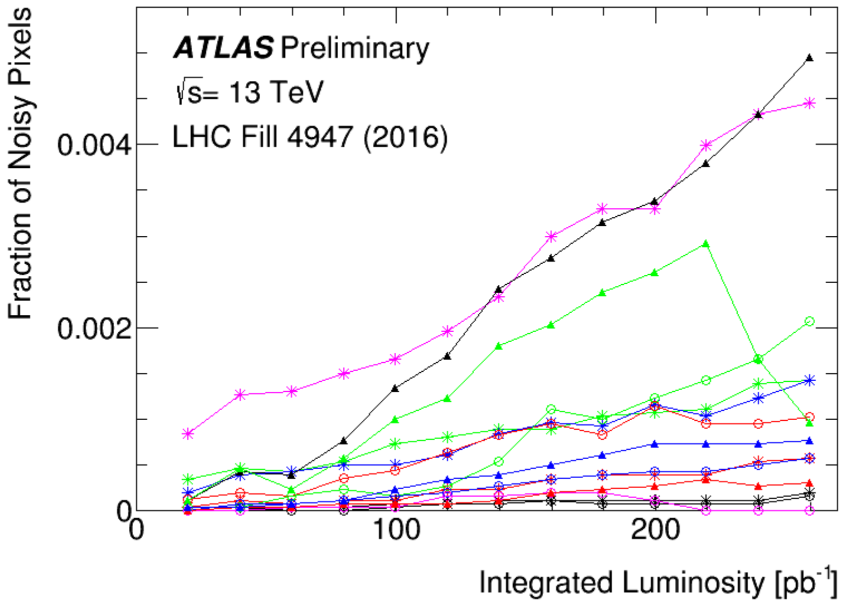
Noisy SCT chip due to SEU

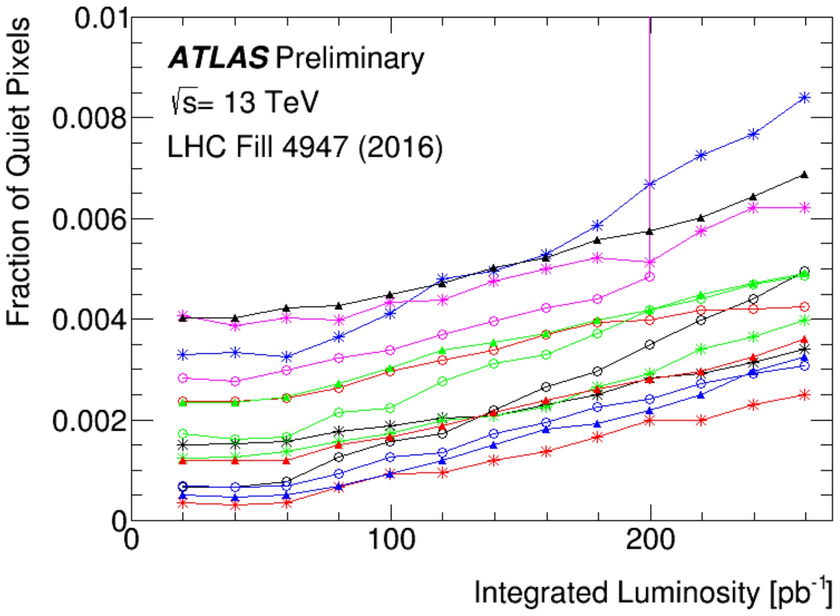


Quiet IBL chip due to SEU



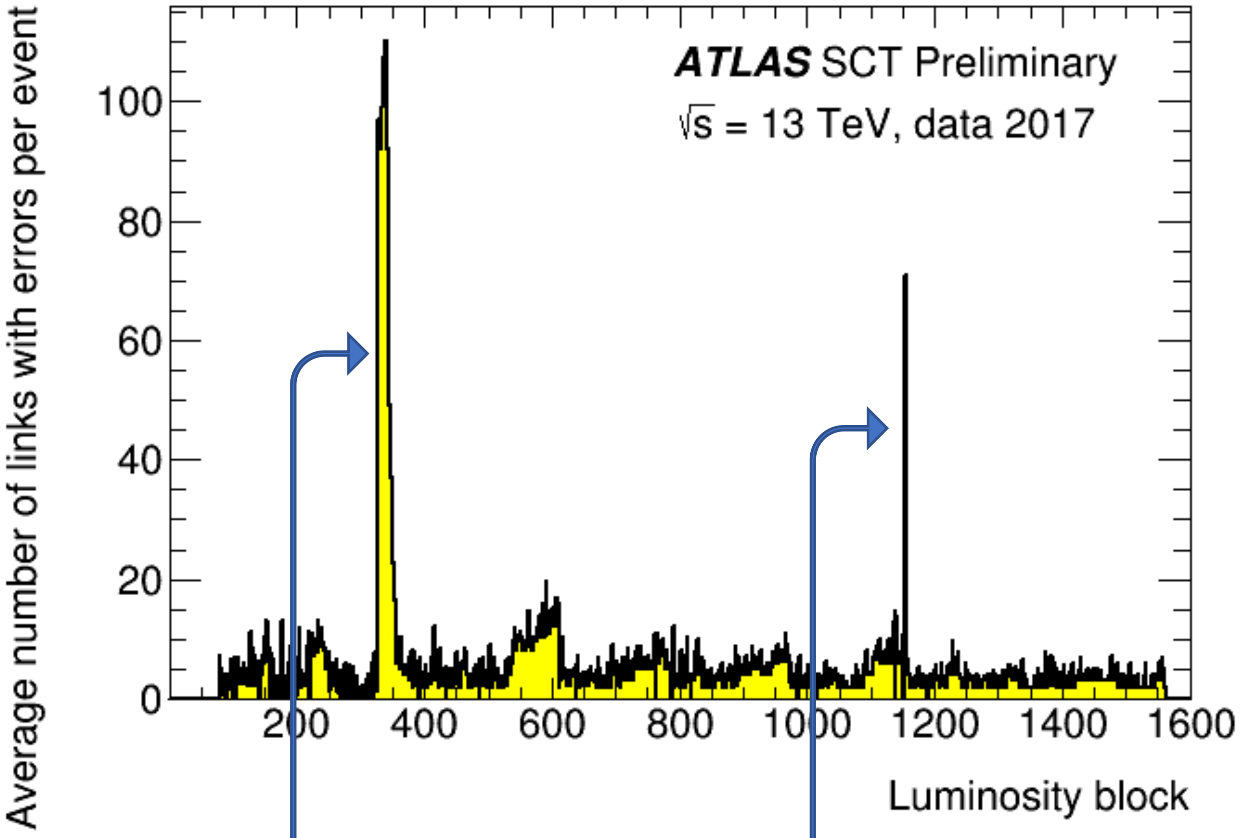
Single Event Upsets in single pixels





- SEUs can corrupt single pixel registers in IBL
- Produces quiet and noisy pixels → increases during data taking
- Method now developed that reconfigures pixel configurations together with frontend (every 5s)
- Not yet deployed but ready for Run 3

SEUs and Desynchronization – Example SCT



PS crate trip
→ no power to 48 modules

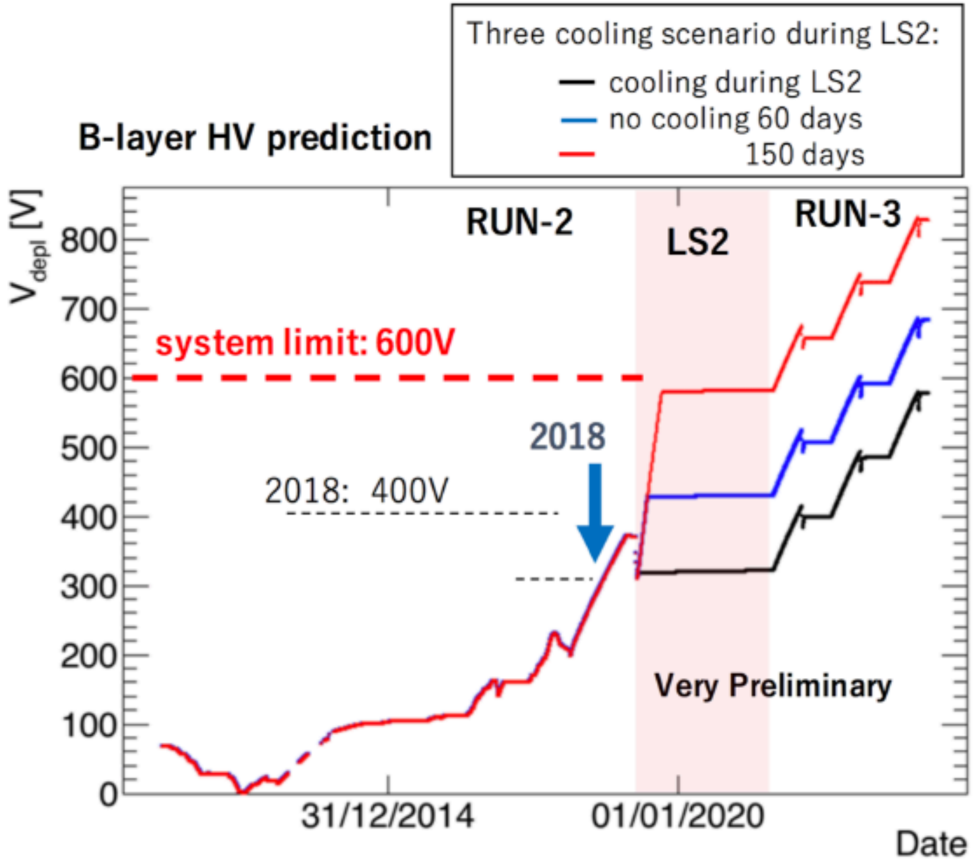
ROD reconfigure
→ no data from 36 modules

- Energy deposition in p-i-n diode causes bit flip of trigger
  → trigger lost, desynchronization of module
- Error flag assigned to module
  → watchdog then reconfigures the individual module and includes it back into data taking
- Module recovery restricts count of link errors to < 5 at any time
- (Of course, link errors are not just caused by SEUs)
- Similar measures in place for Pixel/IBL

Pixel reverse annealing

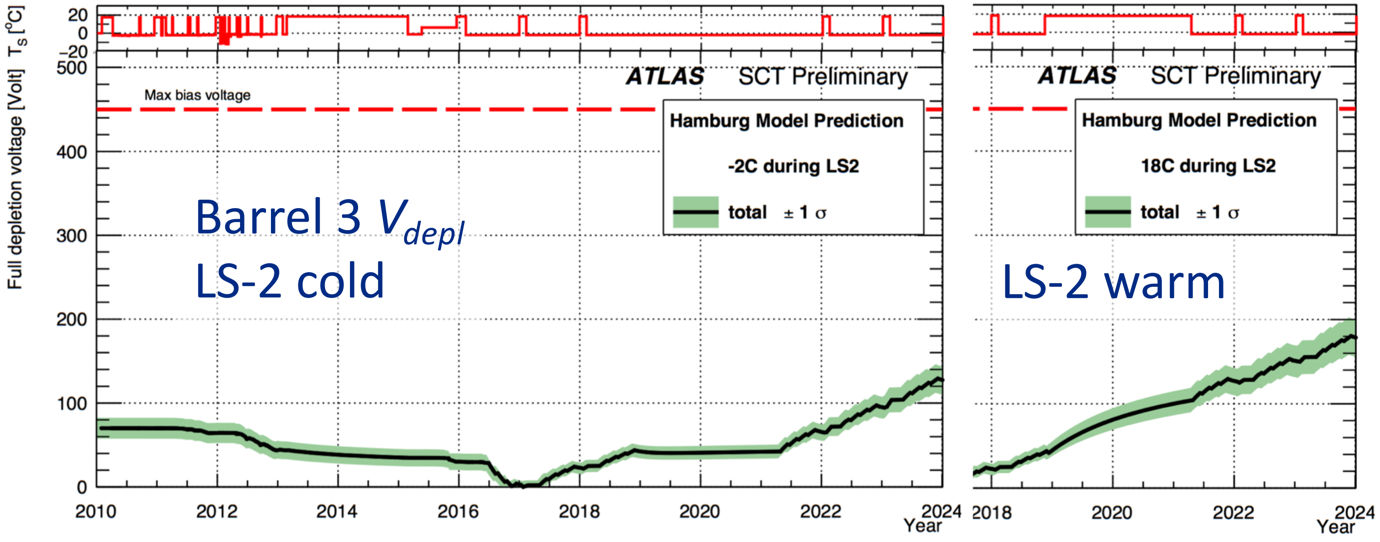
- Reverse annealing is a serious issue for the Pixel detector
- Already end-of-year shutdowns have effects
  → WS 2017/2018 only 10 warm days
- If Pixel Detector is **warm** during Long-Shutdown 2
  → depletion voltage will increase far beyond the operational limit of 600 V

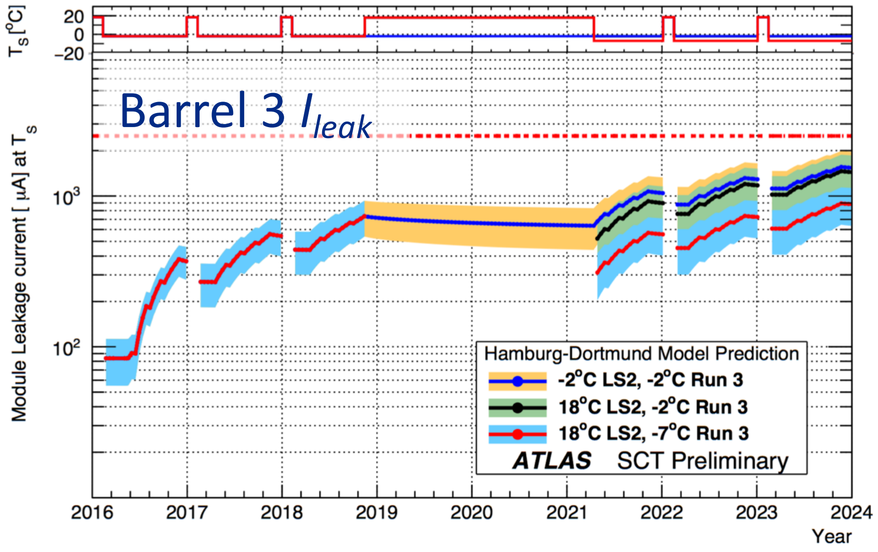
- It is crucial to keep the detector cold as long as possible in Long-Shutdown 2



Predictions for b-layer

SCT depletion voltage projection



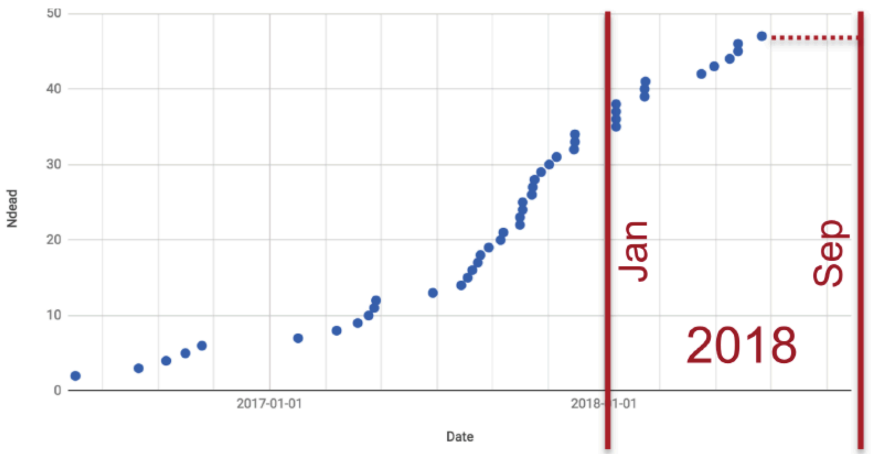


- Assuming 60 fb^{-1} per year in Run 3 (on the low side)
- V_{depl} larger for warm scenario and I_{leak} slightly smaller
- Cooler operation temperature would decrease I_{leak}
- Sufficient headroom for Run 3
- But: would like to keep detector cold during Long-Shutdown 2 to minimize HV in Run 3

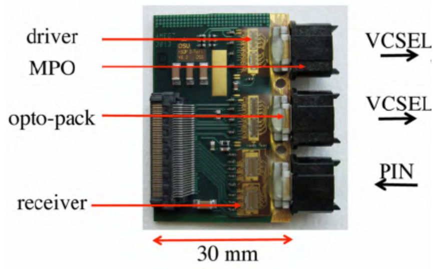
Plans for Long-Shutdown 2

- Pixel VCSELs on opto-boards have been dying since 2016, possibly due to humidity, 14 dark channels this year
  → All opto-boards will be exchanged to be safe for Run 3
  → Requires access to the detector
- SCT has seen faults in power supplies during Run 2 from the 48V power packs and the 48V/5V DC/DC converters
  → DC/DC converters could be reproduced and will be exchanged for the full system
  → Power packs (commercial) do not exist anymore, replacement system in development to be installed during 2020 for half the detector
- Improve calibrations to deal with increase radiation damage in Run 3

Disabled modules due to dead VCSELs



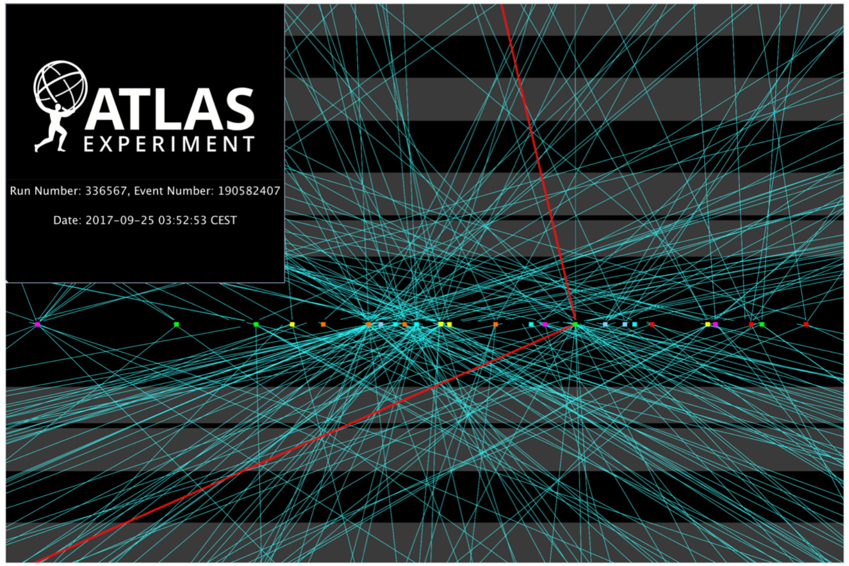
Opto-board



Artesyn PPMs
(out of production)

Conclusion

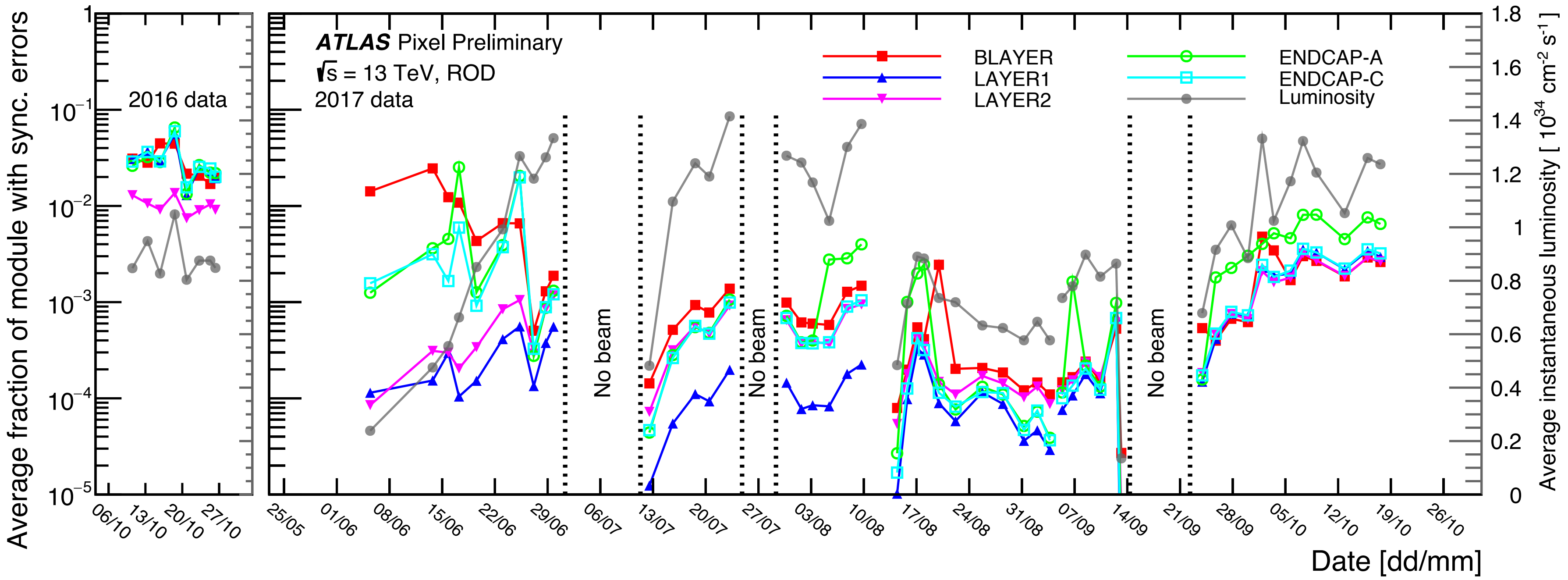
- Data taking of Run 2 is almost concluded. Pixel and SCT are more than 2/3 through their journey!
- Pixel and SCT are 10 years old and still in great shape.
- Radiation damage more and more visible
  - Increase of bias voltage to ensure full depletion
  - Changes in pixel threshold to ensure good charge collection efficiency
  - SEU effects well under control
- Run 2 operations have been a success
  - Upgrades on hardware and firmware of the readout as well as the DAQ system have improved deadtime and data quality



Thank you for your attention!

BACK-UP

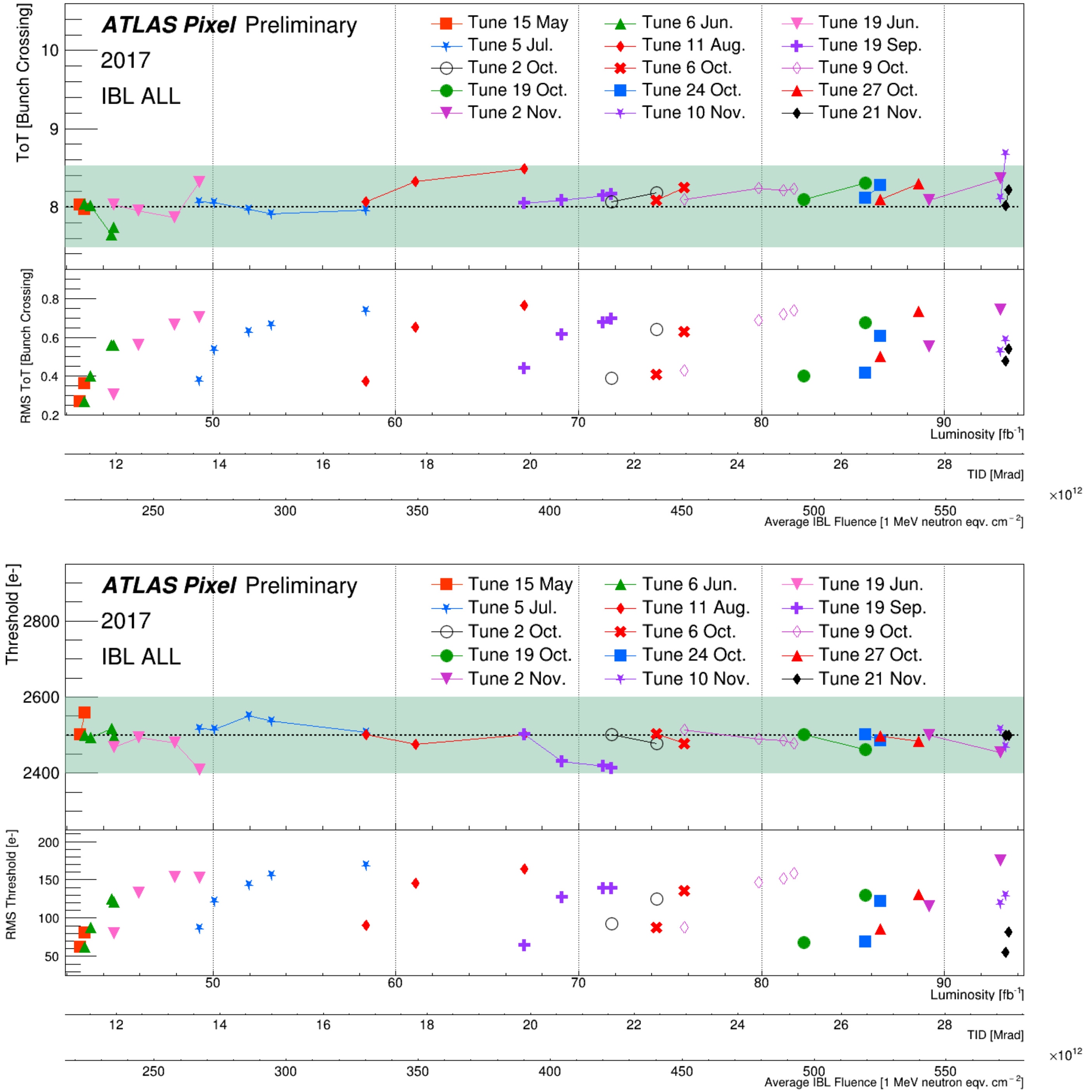
Desynchronisation – Pixel/IBL



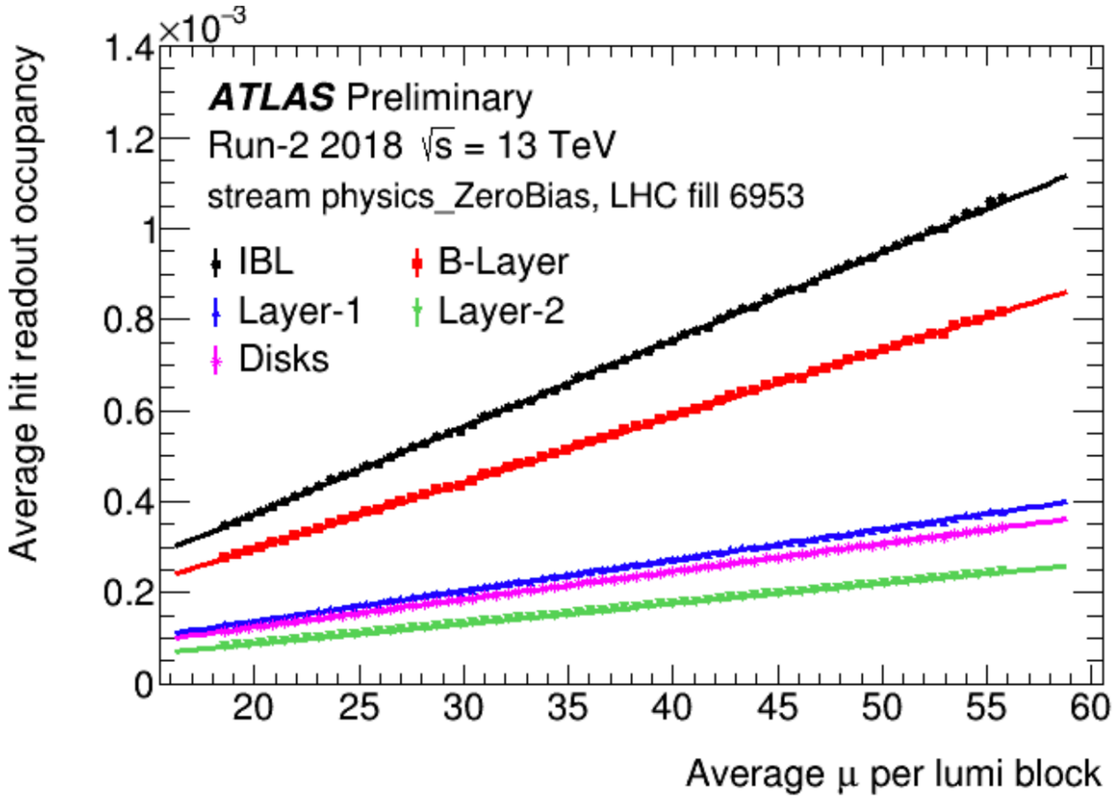
- Desynchronization under control (< ~1% level) despite higher luminosity in 2017

Calibration - IBL

- High luminosity impacts significantly Pixel and IBL response over time
- Regular monitoring and tuning of pixel detector allows to maintain running conditions and optimise performance.
- It involves pixel team as a whole to monitor and control evolution throughout Run 2.
- Run-3 conditions will be even more challenging. Experience and feedback from Run-2 will be useful.

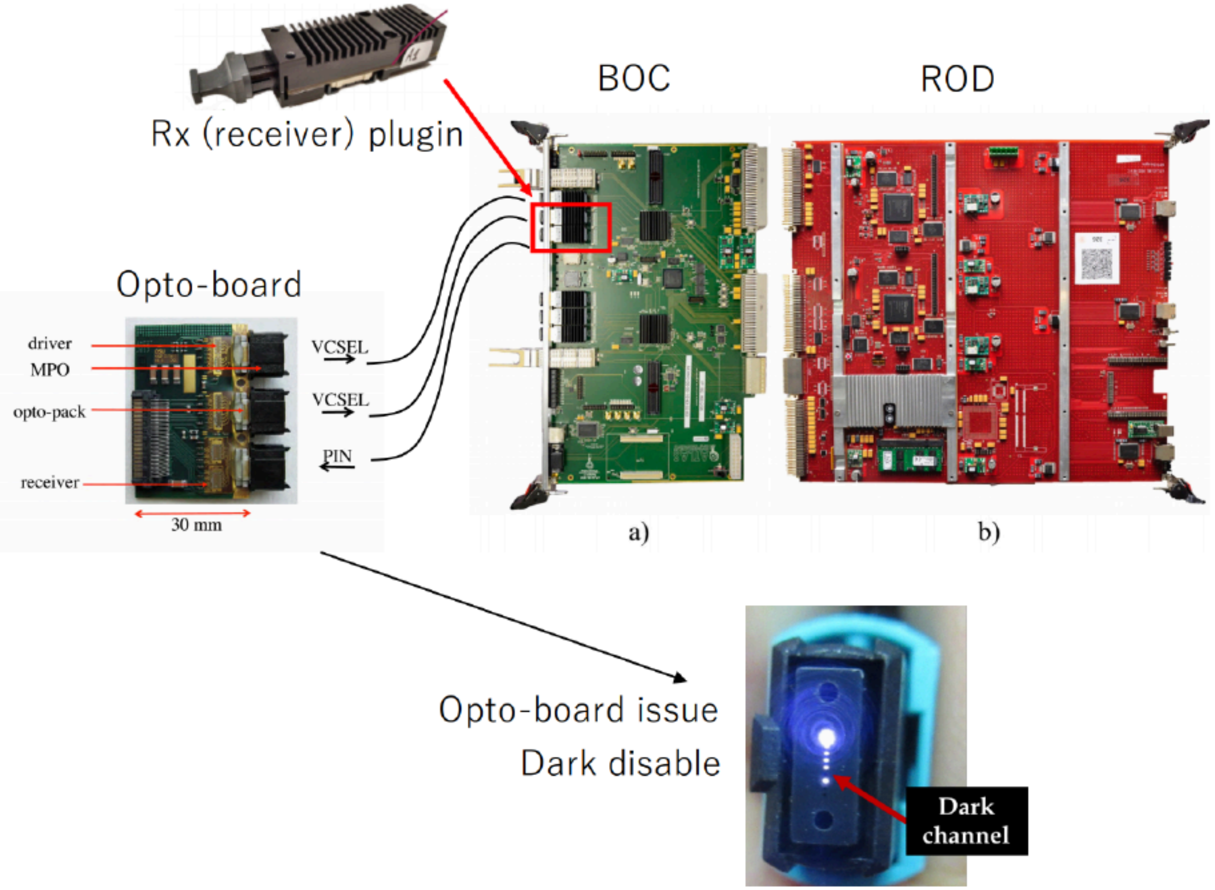


Occupancy vs pile-up – Pixel/IBL



- The occupancy is the number of hits per pixel per event, and mu is the number of interactions per bunch-crossing for events collected by a zero-bias trigger in 2018.

Pixel connection scheme



30 modules (dark channels) were recovered over YETS