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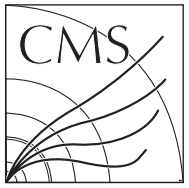

The Compact Muon Solenoid Experiment

Conference Report

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Service Hybrids for the Silicon Strip Modules of the CMS Phase-2 Outer Tracker Upgrade

L. Feld, W. Karpinski, K. Klein, A.J. Pauls, G. Pierschel, M. Preuten, M.P. Rauch, N.M. Roewert and M. Wlochal
on behalf of the CMS Tracker Group

Abstract

This paper describes prototyping work for service hybrids, flexible circuits that form an integral part of the silicon strip modules to be used in the CMS Phase-2 Outer Tracker. The service hybrid is responsible for power distribution, data serialization, and opto-electrical conversion. First prototype service hybrids, featuring the complete functionality, have been developed, produced, and characterized. In addition a first prototype of a test board, which allows to test all aspects of the complex service hybrids, as will be required during the production phase, has been developed. After a short introduction to the CMS strip modules the functionality of the service hybrid will be explained and the present prototype will be described, followed by selected test results. The test system concept will be introduced and first results will be presented.

Presented at *TWEPP2018 Topical Workshop on Electronics for Particle Physics*

PROCEEDINGS OF SCIENCE

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1. Physikalisches Institut B, RWTH Aachen University, Aachen, Germany

E-mail: katja.klein@cern.ch

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*Speaker.

1. CMS Tracker Upgrade and 2S Modules

The CMS collaboration foresees to replace the present tracker during the LHC Long Shutdown 3 (2024-2026) [1]. The new detector is required to cope with the conditions at the High Luminosity LHC (HL-LHC). Design goals are increased radiation tolerance and bandwidth, higher granularity, larger tracking acceptance, and delivery of tracker data to the first level (L1) trigger. The new tracker features a pixel detector and an Outer Tracker (OT). The OT will be equipped with 5616 pixel-strip (PS) modules at radii between 20 and 60 cm, and with 7680 strip-strip (2S) modules further outside. The focus of this work is on the 2S module, which features two strip sensors on top of each other. The design driver for the module concept is the desire to deliver tracker data to the L1 trigger. While the full tracker information cannot be read out at 40 MHz due to bandwidth limitations, the majority of the tracks are of low transverse momentum, p_{T}. By exploiting the p_{T}-dependent bending of the tracks in the magnetic field, low and high p_{T} tracks can be discriminated by their different hit patterns in the two closely spaced sensors within a module. This is performed at the module level, within the readout chip. Only hit patterns above a p_{T} threshold (called stubs) are forwarded to the L1 trigger. Upon reception of the L1 trigger signal, the complete event information is read out.

The 2S module (Fig. 1, left) exists in two variants, with different sensor spacing. The strip cell size is 5 cm by 90 μm. Each sensor features two rows of 1016 strips. The sensors are glued to support bridges made of aluminium/carbon fibre (AlCF). The sensors are wire-bonded on each side to the front-end hybrids (FEH), which carry eight readout chips (CMS Binary Chip, CBC) and one data concentrator chip (Concentrator Integrated Circuit, CIC) each [1]. The FEHs are folded around a spacer, and the signals from the bottom sensor are routed through the fold-over to the CBCs. Each module carries one service hybrid (SEH), responsible for power distribution, data serialization and opto-electrical conversion. This makes each module an autonomous unit.

2. Service Hybrids of 2S Modules

The SEH is a flex circuit that is glued onto a CF stiffener. Part of the circuit is folded around the stiffener. The SEH is connected on both ends with fine-pitch connectors via flexible tails to the

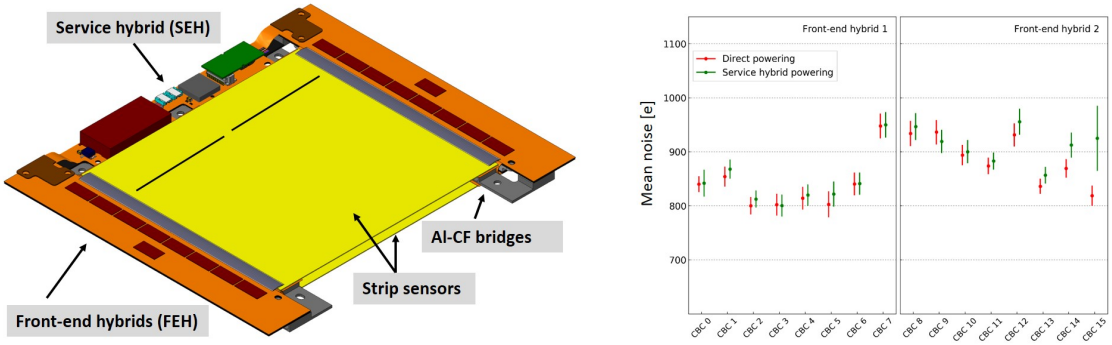

Figure 1: Left: drawing of a 2S module, showing also the service hybrid. Right: the noise of each CBC of a prototype module (Sect. 3), when powered either with a lab supply (red) or via the SEH (green).

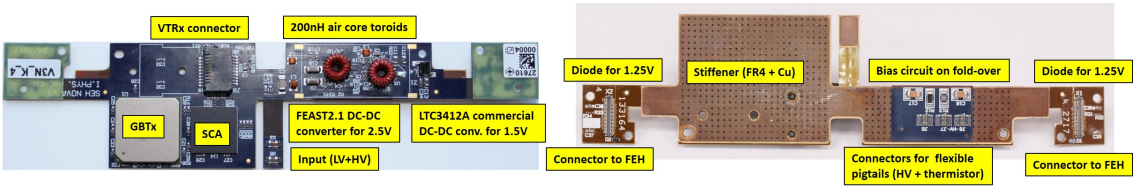

Figure 2: Top (left) and back (right) side of the service hybrid prototype, with all major components labelled.

FEHs. On the top-side of the board, four active components are mounted. Two point-of-load buck converters [2] provide the low voltages to the FEHs and to active components on the SEH. The DC-DC converters are covered by an electro-magnetic shield. The Low-power Gigabit Transceiver (LpGBT) receives the data from the CICs on the two FEHs, and forwards them to the Versatile Transceiver plus (VTRx+) module [3], a pluggable device that performs opto-electrical conversion. On the back-side (fold-over) the high voltage (HV) circuit is located. Small pluggable Kapton tails are used to deliver the HV (up to 800 V) to the sensors' backsides.

In the OT a two-step DC-DC conversion scheme is used. The first stage DC-DC converter (bPOL12V) receives about 11 V and converts this to 2.55 V, needed by the VTRx+. This voltage is then converted to 1.25 V, needed by the CBCs, the CICs, the LpGBT, and the VTRx+, by the second stage DC-DC converter (bPOL2V5). The advantage of DC-DC conversion is that the input current is reduced by the conversion ratio, r, which in turn reduces voltage drops and power losses on the supply cables by r and r^2, respectively. The bPOL12V and bPOL2V5 are radiation-tolerant buck converters developed by CERN. Power supplies will be located in the experimental cavern, and be connected to the front-end via about 40 m long cables. Sensing is not foreseen, to reduce the material budget and to avoid interference with the regulation of the DC-DC converters. Voltage drops of up to 4 V are expected.

The LpGBT receives data from each CIC via six differential lines at 320 Mb/s: five lines deliver the stub data, while the sixth line delivers the full readout data. These data are serialized and formatted by the LpGBT and forwarded to the VTRx+ at 5.12 Gb/s. The LpGBT generates a 320 MHz clock for the FEHs, and distributes control data (triggers, fast resets, etc.) via a 320 Mb/s fast control line. The LpGBT configures the CBCs, CICs, and the VTRx+ via the I^2C protocol. The Slow Control ASIC (SCA) block in the LpGBT receives a number of analogue inputs (e.g. input voltage, DC-DC output voltages, optical power) for monitoring, and sends hard resets to the CBCs and CICs. The LpGBT and the VTRx+ are under development at CERN.

3. SEH Prototyping

SEH prototypes have been developed and produced (Fig. 2). They feature the full functionality. However, since the active components are still under development, replacements were used. The FEAST2.1 DC-DC converter [4] is used in the first conversion stage, and a commercial buck converter represents the second stage. The LpGBT is replaced by the GBTx and the SCA, and the VTRx+ by the VTRx. Since 1.5 V is needed by the GBTx and SCA, Schottky diodes are used to generate 1.25 V from 1.5 V. The flex circuits have four copper layers of 17 μm nominal thickness. The boards can be used to read out the signal from the CIC, or directly from one CBC per side.

Since DC-DC converters switch high currents at MHz-frequencies, and since the DC-DC converters are placed very close to the sensors and FEHs, an electro-magnetic shield is necessary, to reduce radiated emissions. The shield is made of a 150 μm thick aluminium foil, which is folded into the shape of a box. It is soldered to ground pads at the four corners. Scans of the emitted field with a pick-up probe have shown that the emissions are drastically reduced. However, only tests with real modules can prove that the module performance is not deteriorated by either emitted or conducted noise from the DC-DC converters. A SEH prototype was used to power a prototype 2S module, and the module's noise was compared between direct powering from a laboratory power supply, and DC-DC conversion powering (Fig. 1, right). The module was not read out by the SEH in this case, but by a separate test board. Threshold scans were made and the module noise was extracted as the width of so-called S-curves. The noise of all 16 CBCs was within specifications. The noise for direct powering and DC-DC powering was identical within uncertainties for most CBCs, except for the two CBCs closest to the DC-DC converters. These showed an increase of the noise by up to 10 %. This effect has been traced back to the slit of the shield facing those chips, and finite element simulations indicate that more grounding points would reduce the remaining emissions. In a future prototype, long solder pads will allow grounding the shield almost all the way around.

All aspects of the control and readout paths have been tested, including the I^2C communication with all available devices (VTRx and CBCs on the FEHs). Eye diagrams of the 320 MHz clock and 320 Mb/s fast commands, both generated from the GBTx, showed sufficient data integrity. No synchronization losses or errors were observed over hours. The prototype module can be monitored effectively (e.g. voltages, optical power) via the SCA and resets from the SCA are received. The 4.8 Gb/s differential lines between GBTx and VTRx were successfully tested with a loop-back procedure. Random data were generated at the back-end in the Gigabit Link Interface Board (GLIB), sent optically to the VTRx, passed on to the GBTx, and sent back. Eye diagrams at various stages of the loop were examined and found to be of sufficient quality. Data were sent over days and the bit error rate was measured. No bit errors were observed for the default laser driver bias setting.

Readout tests were performed with small prototype FEHs, equipped with two CBC3 chips (Fig. 3). No full modules with connectors are available at this point. Data were read out from the CBCs directly (one CBC per side), as the CIC is not yet available. The 320 Mb/s full event data from the CBCs were read by the GBTx, and sent via the VTRx to the GLIB. A rudimentary DAQ firmware had to be developed for this test. The extracted noise is compatible with the noise achieved using a standard test board readout. The readout of the 320 Mb/s stub data via five lines per side was also exercised. Three stubs were generated artificially by masking most channels and by setting the threshold very low, so that (noise) hits were present in the unmasked channels. The position and the bending of those stubs were thus known. The correct information was retrieved, proving the successful readout of the stub information. Due to a bug in the layout three out of ten lines could not be tested. It should be noted that the FEHs were powered from the SEH in all tests.

4. Service Hybrid Test System

A total of 18 912 service hybrids for 2S and PS modules will have to be qualified within two years, starting from 2021, for use in the experiment. While the details of the Quality Control are under discussion, a cheap setup and a large throughput would clearly be advantageous. All

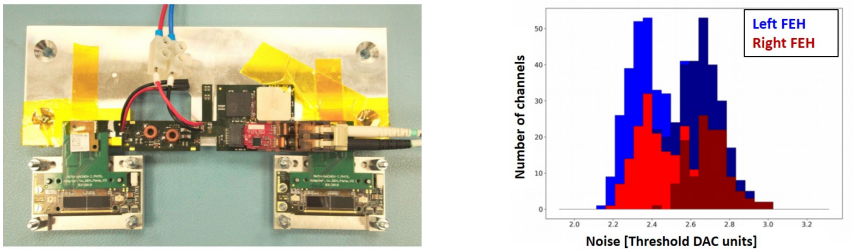

Figure 3: Left: readout of two small FEHs via the SEH. The FEHs are connected via adapter cards. Right: noise distributions of all readout channels. The two shadings correspond to channels with different FEH trace lengths, leading to two peaks per side.

SEHs should be tested at least once at their operating temperature. The present concept foresees a small cold volume, hosting the SEH under test, which is connected to two chillers, one running permanently at room temperature, the other running permanently at $-35°$C. A test board has been developed that allows to test the complete functionality of the 2S SEH. It is controlled by an on-board Raspberry Pi computer. The board features an FPGA for the test of the clock and reset lines, an ADC to measure slow control parameters, an I^2C RAM for I^2C testing, and two pairs of GBTx and VTRx (one pair is needed per SEH side). An HV isolation test is also possible. The isolation test, I^2C test, and monitoring via the ADC have been successfully tested. The clock and reset line test consists of counting clock cycles and resets with the FPGA, and comparing measurement with expectation. This works in principle, however a miscounting of clock cycles on the per mille level happens for one SEH side. The data line test uses pseudo-random data, generated at the back-end, which are sent via the test board's VTRx and GBTx to the SEH, and back. A bit error rate is measured. While the concept has been shown to work, unfortunately one SEH side shows a higher bit error rate. The mentioned problems are believed to be due to insufficient signal integrity on the test board, and the layout is being improved.

5. Summary

First fully functional prototypes of SEHs for the 2S modules have been developed, produced, and tested. For the first time FEHs were powered and read out by SEHs. This work serves as a proof-of-principle of the concept. In addition a complex test board was prototyped. Improved versions of both the SEH and the test board are under development.

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[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Tracker, CERN-LHCC-2017-009 (2017).

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[3] J. Troska et al., The VTRx+, an Optical Link Module for Data Transmission at HL-LHC, PoS (TWEPP-17) 048.

[4] https://project-dcdc.web.cern.ch/project-dcdc/