CLICdp-Conf-2018-008
15 October 2018

Design of a monolithic HR-CMOS sensor chip for the CLIC silicon tracker

I. Kremastiotis[1)*†], R. Ballabriga[*], N. Egidos[*‡], on behalf of the CLICdp collaboration

[*] *CERN, Switzerland,* [†] *Karlsruhe Institute of Technology, Germany,* [‡] *University of Barcelona, Spain*

Abstract

The CLIC Tracker Detector (CLICTD) is a monolithic active pixel sensor targeted at the tracking detector of a future experiment at the Compact Linear Collider (CLIC). The chip features a matrix of 16×128 cells, each cell measuring 300×30 μm^2. The cells are segmented in the long direction in order to maintain the benefits of the small collection electrode. In the digital logic, a simultaneous 8-bit Time of Arrival and 5-bit Time over Threshold measurement is performed. A 180 nm HR-CMOS Imaging Process was selected for the design of a chip that will meet the requirements of the tracker at CLIC. In this document, the CLICTD design and chip interface are presented.

Poster presented at Topical Workshop on Electronics for Particle Physics (TWEPP 2018)
KU Leuven, Antwerp, Belgium, 17–21 September 2018

This work was carried out in the framework of the CLICdp Collaboration

[1]E-mail: iraklis.kremastiotis@cern.ch

PROCEEDINGS OF SCIENCE

Design of a monolithic HR-CMOS sensor chip for the CLIC silicon tracker

Iraklis Kremastiotis * [a,b], **R. Ballabriga** [a], **N. Egidos** [a,c]

on behalf of the CLICdp collaboration

[a] *CERN, Geneva, Switzerland*
[b] *Karlsruhe Institute of Technology, Karlsruhe, Germany*
[c] *University of Barcelona, Barcelona, Spain*
E-mail: iraklis.kremastiotis@cern.ch

The CLIC Tracker Detector (CLICTD) is a monolithic active pixel sensor targeted at the tracking detector of a future experiment at the Compact Linear Collider (CLIC). The chip features a matrix of 16×128 cells, each cell measuring 300×30 μm^2. The cells are segmented in the long direction in order to maintain the benefits of the small collection electrode. In the digital logic, a simultaneous 8-bit Time of Arrival and 5-bit Time over Threshold measurement is performed. A 180 nm HR-CMOS Imaging Process was selected for the design of a chip that will meet the requirements of the tracker at CLIC. In this document, the CLICTD design and chip interface are presented.

Topical Workshop on Electronics for Particle Physics
17 - 21 September 2018
KU Leuven, Antwerp, Belgium

*Speaker.

1. Introduction

The Compact Linear Collider (CLIC) is an option for a future multi-TeV e^+e^- collider at CERN [1]. A multi-layer silicon tracker is currently foreseen for the CLIC detector [2].

The requirements for the CLIC tracking detector include a time measurement (Time of Arrival - ToA) with 8 bits range and 10 ns time-tagging and an energy measurement (Time over Threshold - ToT) with 5 bits precision. A single point resolution of 7 µm in the transverse plane is required. The total material budget including supports, cables and cooling is $1-1.5\%$ X_0 per detection layer, allowing for ~ 200 µm for the silicon layers (sensor and readout). The average power consumption should be limited to $150\,\mathrm{mW/cm^2}$. Thanks to the low duty cycle of the CLIC beam (156 ns bunch trains, repeated every 20 ms), a power pulsing scheme can be implemented, where different parts of the circuit are switched off between subsequent bunch trains, thus minimising the average power consumption. The maximum expected hit rates from beam-induced background particles in the innermost tracker layers, including safety factors, are approximately 0.6 $\mathrm{hits/mm^2/bunch\ train}$. Frame-based readout of the entire bunch train, without multi-hit capability, is therefore feasible for pixel areas not exceeding a few percent of $0.6\,\mathrm{mm^2}$.

In a monolithic detector the signal processing takes place in the same chip as the signal collection [3]. Monolithic detector chips are considered for the CLIC silicon tracker, as they can simplify the assembly of the large active area ($\sim 100\ \mathrm{m^2}$) of the system.

In this document, the main design aspects of the CLIC Tracker Detector (CLICTD), a monolithic detector chip designed according to the requirements for the CLIC silicon tracker, are presented. The matrix of the CLICTD prototype includes 16×128 elongated pixels of $300 \times 30\ \mu\mathrm{m^2}$, for a total sensitive area of $4.8 \times 3.84\ \mathrm{mm^2}$.

2. The process

A 180 nm CMOS imaging process with a High-Resistivity (HR) epitaxial layer has been chosen for this design. It offers a deep p-well, which allows the in-pixel digital logic to be isolated from the collection electrode. The signal collection is done with a tiny collection electrode with very small capacitance. This minimises the noise in the front-end. A modification of this process, presented in Figure 1, includes an additional N-type implant that allows for a full lateral depletion under the deep P-well [4].

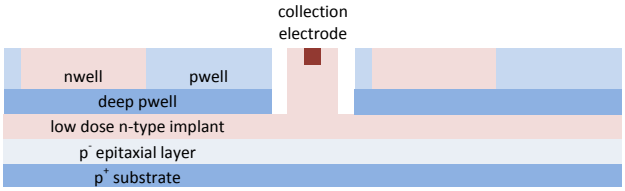


Figure 1: Process cross-section (not to scale).

3. The CLICTD detector channel

3.1 Analog front-end

The CLICTD detector channel consists of an elongated pixel of $300 \times 30\ \mu\mathrm{m^2}$. Following simulations and measurements with chips produced in the same process, the required single point

resolution of 7 µm in the transverse plane can be achieved with a 30 µm pitch [5]. In the analog part, the pixel is segmented along the row direction in eight front-ends, to ensure prompt charge collection. The pitch of the collecting diodes in the long direction is therefore 37.5 µm, which, according to simulations, is expected to allow for a prompt charge collection and thus not compromise the timing performance of the chip.

The charge collected in each diode is integrated in a Charge Sensitive Amplifier (CSA). The amplified signal is then compared with a global threshold in the discriminator. A 3-bit DAC for local threshold tuning is included to compensate for pixel-to-pixel variations. The whole chain is repeated eight times in each pixel, as illustrated in Figure 2.

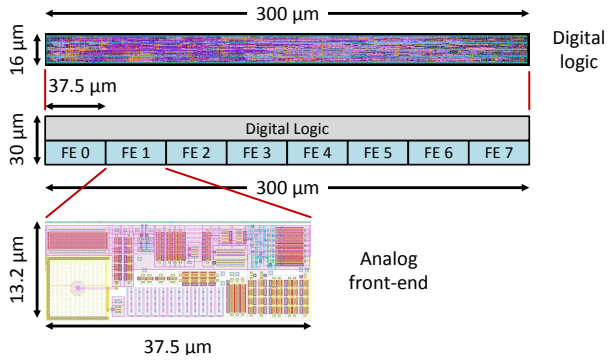


Figure 2: Layout of the CLICTD pixel, where the analog part is segmented in eight front-ends.

Simulation results show a gain of 550 $\mathrm{mV/ke^-}$, a noise of 14 $\mathrm{e^-}$ RMS and a minimum detectable charge (after threshold equalisation) of 93 $\mathrm{e^-}$. The main power consuming nodes of the analog front-end are set to a low power mode between subsequent bunch trains. The simulated power density for the analog part of the CLICTD matrix is $\sim 100\ \mathrm{mW/cm^2}$ during operation with continuous power. However, a reduction by a factor of ~ 50 is expected after applying the power pulsing scheme for the CLIC duty cycle.

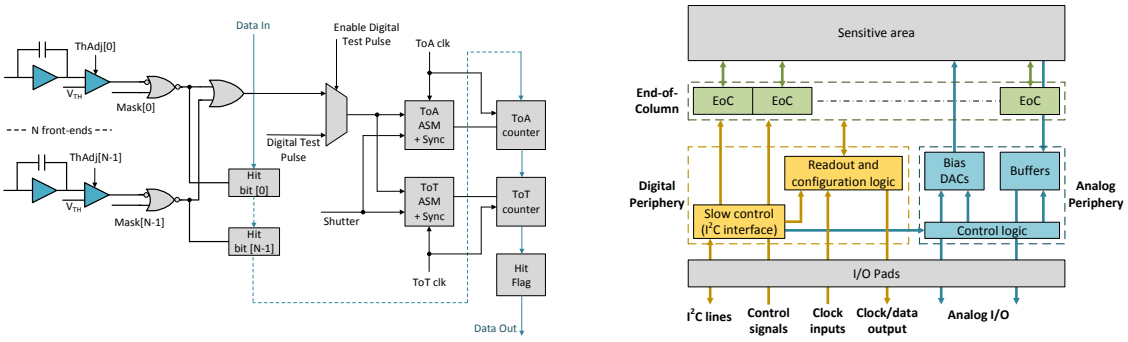
3.2 Digital logic

In the digital logic of the CLICTD pixel, binary hit information is stored for each of the eight front-ends. Then, all eight discriminated outputs are combined by means of an "OR" gate. The combined output is further processed for the ToA and ToT measurement. For the ToA measurement, a shutter signal is used as a time reference and the measurement is performed using a 100 MHz clock provided to the matrix during acquisition. The energy information is stored by measuring the time window while the CSA output remains above the applied threshold (ToT). The dynamic range of the ToT measurement is programmable, as the 100 MHz clock can be divided by a factor of $2-16$. The slope for the return to baseline of the CSA is also adjustable.

Apart from the nominal 8-bit ToA plus 5-bit ToT measurement, the counters can be combined to a 13-bit long counter and two different measurements can be performed: a 13-bit ToA measurement or a photon counting measurement, where the number of events that are above the applied threshold is accumulated in the counter. In the latter case, no further information (ToA, ToT) is stored for the detected hits. An additional "hit flag" bit, which is set to high once a hit is detected in the pixel, is included in the digital logic. The hit flag bit is used by the compression algorithm, as will be explained in Section 4.

A block diagram and layout of the CLICTD pixel is presented in Figure 3a. The option to mask (exclude from digital processing) individual front-ends is included in the logic. Test pulses can be injected to selected front-ends, as well as to the input of the digital logic. When the digital test pulse is selected, the combined output of the front-ends is disabled such that the digital and analog parts can be decoupled and tested separately.

Clock gating is implemented in order to minimise the digital power consumption. The clock signal will only be enabled in the in-pixel digital circuitry in two cases: when the pixel detects a hit during acquisition (provided that the hit happens within the shutter frame), and when the column is being read out. Different components contribute to the power consumption of the digital logic in the CLICTD matrix: power for data acquisition, readout, clock distribution in the matrix and leakage. Averaging these components over the 20 ms cycle of the CLIC beam (and assuming 1% pixel occupancy) leads to an average power consumption below 3 $\mathrm{mW/cm^2}$ for the in-pixel digital logic.



(a) (b)

Figure 3: Block diagrams: (a) CLICTD pixel, (b) CLICTD periphery.

4. The CLICTD prototype chip

A standard I^2C interface [6] was selected for the slow control of the CLICTD chip. This includes reading and writing all internal registers, as well as the matrix configuration.

For the matrix configuration, 41 bits are required for each pixel: five (one for masking, one for enabling test pulse, three for local threshold trimming) for each of the eight front-ends (40 bits total), plus one for enabling the digital test pulse injection in the logic. As the number of bits that can be shifted in the pixel is limited by the number of flip-flops (22) in the digital logic, the configuration needs to be performed in two steps in order to fully configure the matrix, each time latching the data to the appropriate front-end inputs.

A serial readout at a clock frequency of 40 MHz is implemented in the CLICTD chip. The data are shifted out column by column, starting from the leftmost one. Once all data in a column have been shifted out, the readout proceeds to the next column. In order to reduce the amount of data that are shifted out of the chip, a data compression scheme, based on a zero suppression algorithm is implemented. When data compression is enabled, the total of 22 bits stored in the pixel is shifted out only if a hit was detected. For pixels that were not hit, only one bit, corresponding to the hit flag, will be shifted out. The frame can then be reconstructed off-line, by reverting the compression algorithm.

As mentioned in Section 3.2, the possibility to inject test pulses to selected front-ends or to the input of the in-pixel digital logic is foreseen. The response to test pulses can be evaluated using the serial readout. Additionally, the option to monitor the amplifier output in the analog signal domain is included for a special pixel placed at one corner of the sensitive area.

The chip periphery is estimated to consume a power of ~ 50 mW, largely dominated by the differential drivers for the clock and data output lines.

5. Summary and future plans

The CLIC Tracker Detector (CLICTD) chip is a monolithic detector designed in the framework of the CLIC tracker R&D. A simultaneous 8-bit ToA and 5-bit ToT measurement can be performed in the (300×30 µm^2) pixel. In the analog part, the pixel is segmented in eight front-ends to ensure prompt charge collection. The CLICTD prototype features a matrix of 16×128 pixels.

Simulations show a minimum threshold of 93 e$^-$, a 10 ns time-stamping resolution and an average power consumption for the sensitive area (after power pulsing) of ~ 5 mW/cm^2. An additional power of ~ 50 mW is consumed by the periphery blocks. These results are within the detector specifications. The prototype is currently in the final design stage. Full chip verification is ongoing using the Universal Verification Methodology (UVM) [7]. Once produced, the chip will be characterised with electrical measurements using test pulses and radiation sources, as well as beam tests.

While the design of this chip is performed in view of the requirements of the tracker at CLIC, it is expected to provide valuable input also for other detector applications that could benefit from the features of the selected process technology and pixel architecture.

Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

References

[1] *Physics and Detectors at CLIC: CLIC Conceptual Design Report*, edited by L. Linssen, A. Miyamoto, M. Stanitzki, H. Weerts, CERN-2012-003.

[2] D. Dannheim, A. Nurnberg, *Requirements for the CLIC tracker readout*, CLICdp-Note-2017-002.

[3] W. Snoeys, *Monolithic pixel detectors for high energy physics*, Nucl. Instrum. Meth. A 731 (2013) 125-130.

[4] W. Snoeys et al., *A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance*, Nucl. Instrum. Meth. A 871 (2017) 90-96.

[5] M. Munker et al., *Study of the ALICE Investigator chip in view of the requirements at CLIC*, CLICdp-Note-2017-004.

[6] NXP, *I^2C-bus specification and user manual*, UM10204.

[7] A. Fiergolski, *Simulation Environment Based on the Universal Verification Methodology*, 2017 JINST 12 C01001.