The ATLAS Fast TracKer Architecture, Status & **High-Level Data Quality Monitoring Framework**

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OVERVIEW

The Fast Tracker [1] (FTK) is a highly parallel processor dedicated to quickly and efficiently reconstructing tracks in the pixel and SCT detectors of the ATLAS [2] experiment at LHC. It is designed to identify charged particle tracks with transverse momentum above 1 GeV and reconstruct their parameters at an event rate of up to 100kHz. The average latency of the processing is below 100 microseconds at the expected collision intensities. This performance is achieved by using custom ASIC chips with associative memory for pattern matching, while modern FPGAs calculate the track parameters. In this presentation is described the architecture, the current status and a High-Level Data Quality Monitoring framework of the FTK system. This monitoring framework provides an online comparison of the FTK hardware output with the FTK functional simulation, which is run on the pixel and SCT detector data at a low rate, allowing the detection of non-expected outputs of the FTK system.

THE FTK IN THE ATLAS TDAQ SYSTEM

Following L1-accept signals

FTK ARCHITECTURE





before the event processing

PATTERN MATCHING IN DEDICATED ASSOCIATIVE MEMORIES



In order to optimize

The pattern matching [3] is a core process of the FTK and takes place in ASICs called Associative Memory chips.

Each AM chip can contain up to 128k patterns. The memory size of the AM chip and the total number of patterns in the system affect the FTK performance accordingly.





- Each PU executes in pipeline the two main FTK algorithms, the Pattern Matching (PM) in ASICs and the Track Fitting (TF) in FPGAs.
- 3. Final Fit extrapolates the 8-layers tracks to hits in the remaining 4 layers and performs a 12-layer track fit which removes even more fake tracks.



THE FTK INFRASTRUCTURE & STATUS

The FTK system is composed of 8 VME crates and 5 ATCA shelves, containing in total 450 boards, 8000 AM chips, 2000 FPGAs and thousands high-speed I/O links.

The FTK core is compact (4 racks of electronics) and the power usage is low $(\sim 50 \text{ kW})$ compared to a farm of thousands of commercial CPUs [4] required to perform an equivalent task.



the FTK performance, silicon hits are organized into coarse resolution hits called SuperStrips (SS).



The FTK contains a pattern bank of ~ 1 billion patterns covering the whole detector phase space, mapped into 64 $\eta - \varphi$ towers.

FTK status in ATLAS

- IM/DF/FLIC : 100% installed.
- AUX/AMB : 100% installed / 100% at CERN
- SSB : 30% installed, more expected soon

THE HIGH-LEVEL DATA QUALITY MONITORING FRAMEWORK

Monitoring the functionality of the FTK system by comparing the output of the hardware with the output of the FTK Simulation run on the same ID data.

resolution hit (SS)

Goal: Confirmation that FTK hardware works as expected (in real time)



- A full event fragment (ID & FTK data) is sampled by the Data **Collection Manager**
- FTK Simulation [5] processes full event by following its basic algorithms:
 - Clustering Data distribution Pattern matching Track fitting – Second-stage track fitting – Merging Comparison of HW and SW events
 - Gets FTK simulated tracks (FTK SW)
 - Extracts real FTK tracks (FTK HW)
 - Compares track parameters

Histograms published to Online Histogramming Service

SW tracks Four classes of histograms: 1. Matched HW/SW: tracks are the same 2. Matched HW/SW: tracks are (slightly)

THE FTK PERFORMANCE



Tau identification efficiency as a function of the offline-tau p_T when applying the FTK selection (blue) and calorimeter clusters selection (red) at HLT. The efficiency is defined as the fraction of Level-1 tau matched to a true hadronic tau decay and to an offline tau identified with the offline loose Boosted Decision Tree (BDT). In both cases, the selections have be tuned to give the same background rejection factor of 2 per Level-1 tau candidate (with $p_T > 12$ GeV and calorimetric isolation of 4 GeV). [6]

<µ> = 60

b45_4j45_Tight

2b25_4j25_2j45_Tight_

2b55_4j55_Medium

2b35_4j35_Tight

ATLAS vs = 14 TeV Simulation $\overline{}$ tt (H \rightarrow bb) all hadronic putting additional load on the HLT processors. The plot shows two working points from a draft run-2 menu along with some examples of re-optimized working points in which the b-tagging is run with lower jet thresholds. The output rates of the various trigger items are shown as a function of the event-40 level $t\bar{t}h (h \rightarrow bb)$ efficiency. All operating points assume the re-fitted FTK performance. [6]



REFERENCES

HW tracks

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