Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase-II upgrade

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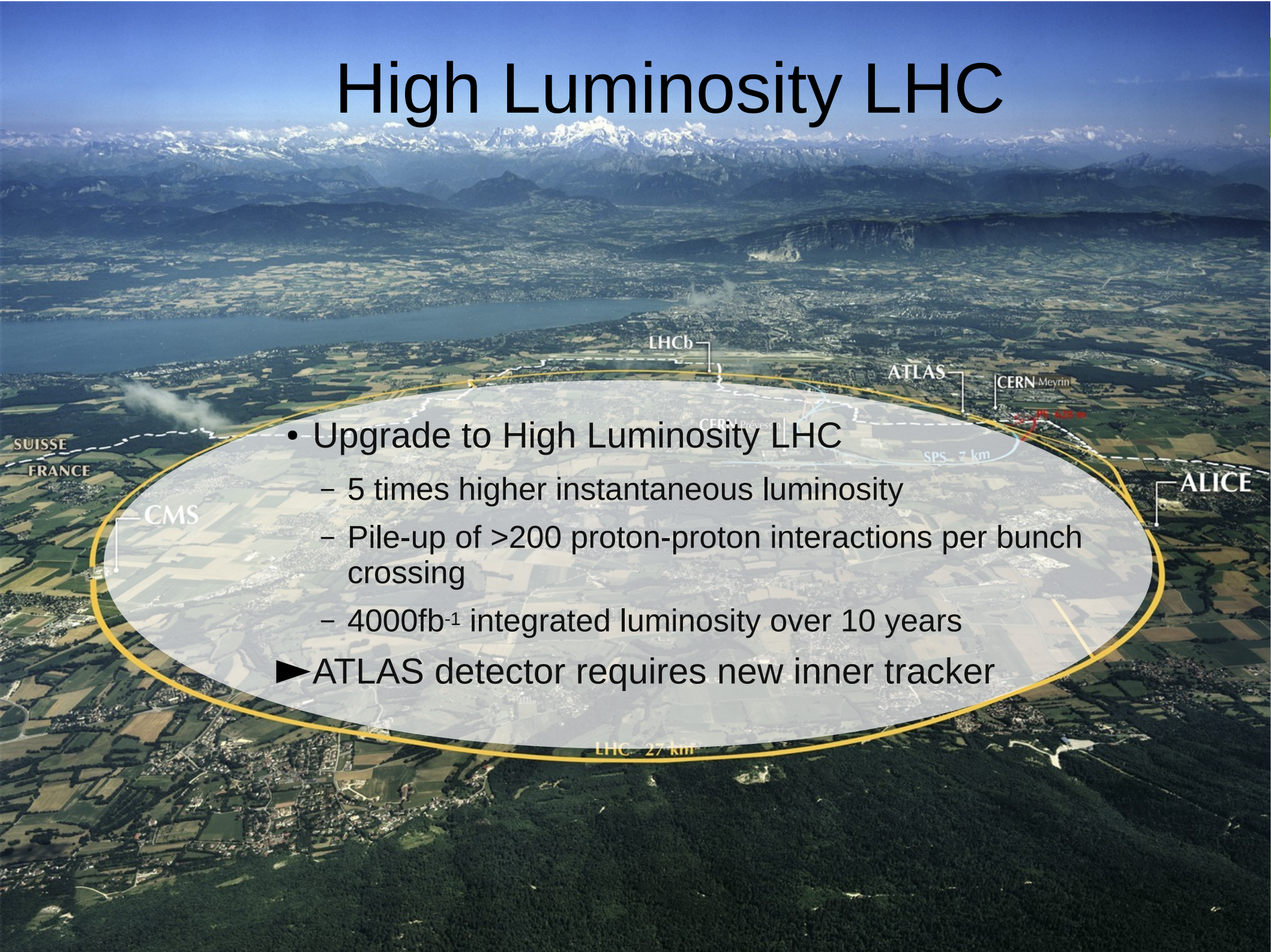
ATLAS EXPERIMENT

Content

- ATLAS Phase-II Upgrade for the HL-LHC
- Serial Powering
- Outer Barrel Demonstrator
- Detector Control System (DCS)
  - Interlock and Monitoring
- Usage of the DCS
- Lessons learned and next steps

High Luminosity LHC

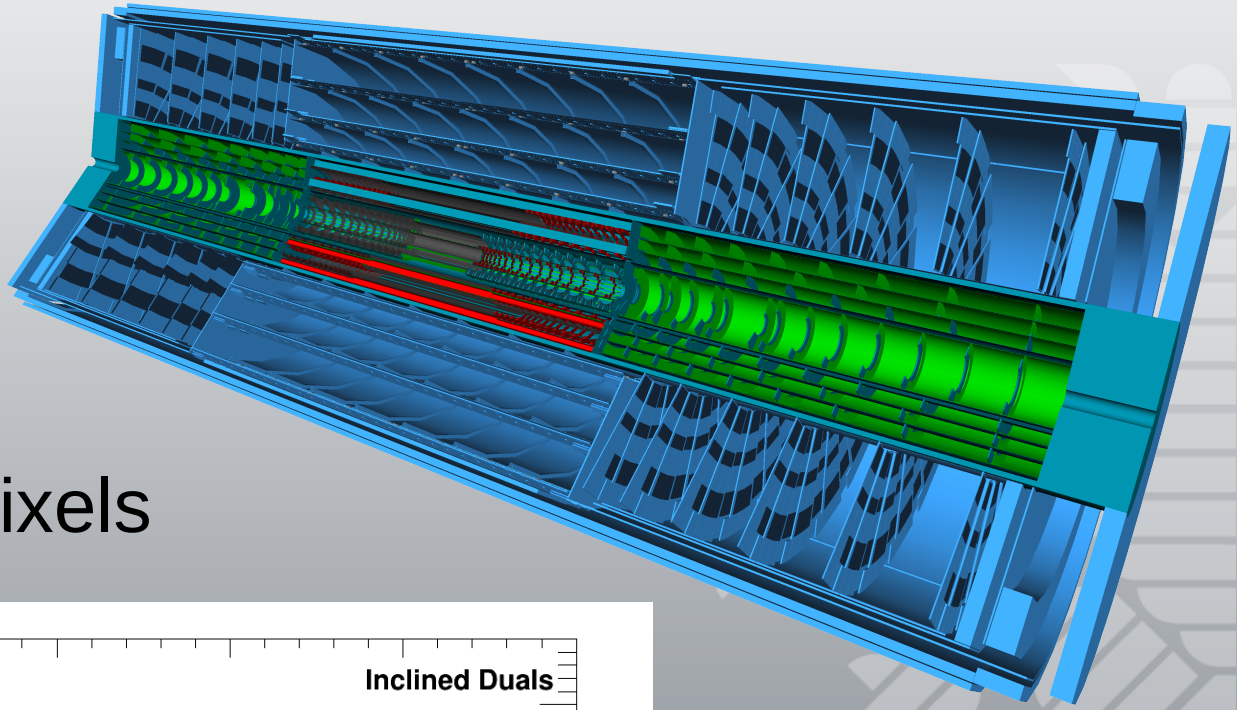


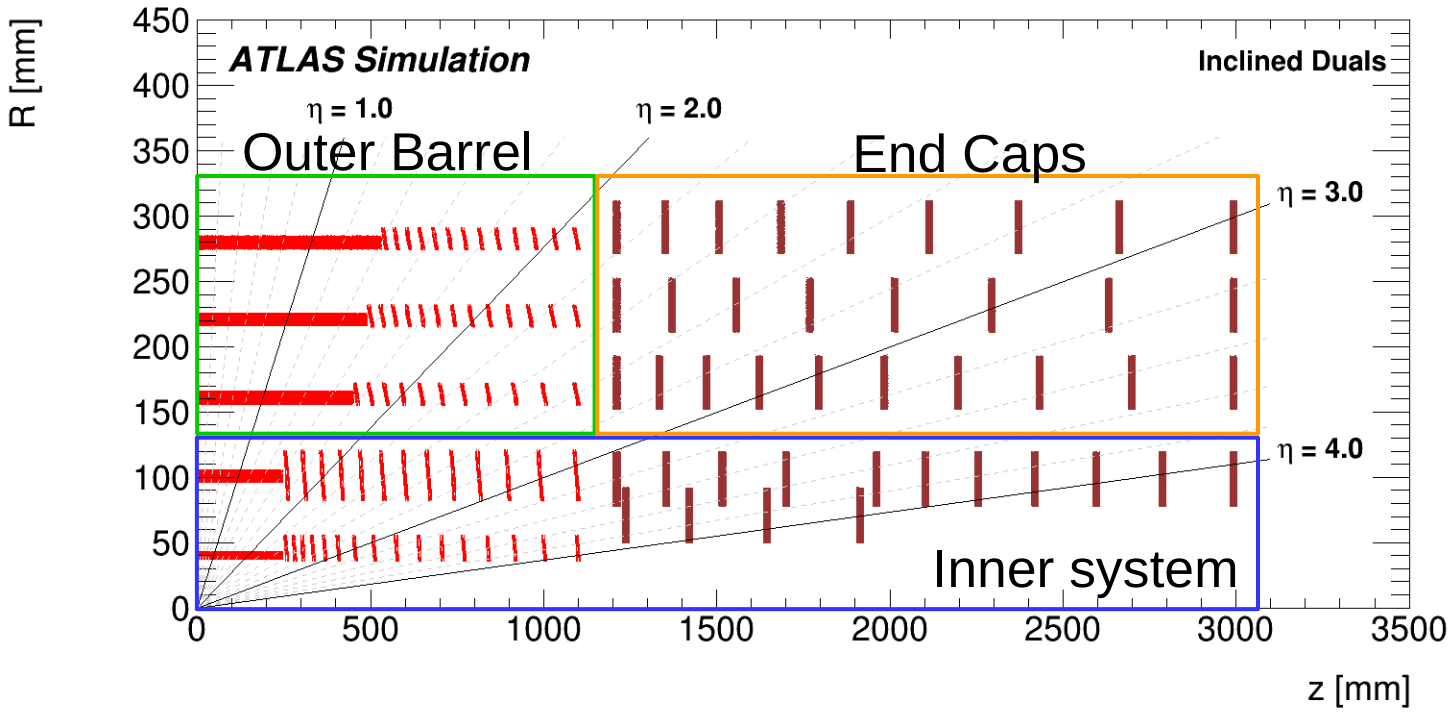
- Upgrade to High Luminosity LHC
  - 5 times higher instantaneous luminosity
  - Pile-up of >200 proton-proton interactions per bunch crossing
  - 4000fb^{-1} integrated luminosity over 10 years

►ATLAS detector requires new inner tracker

Inner Tracker (ITk)

- New full silicon inner tracker
- 4 double sided strips and 5 pixel layers
- Serial powering for pixels





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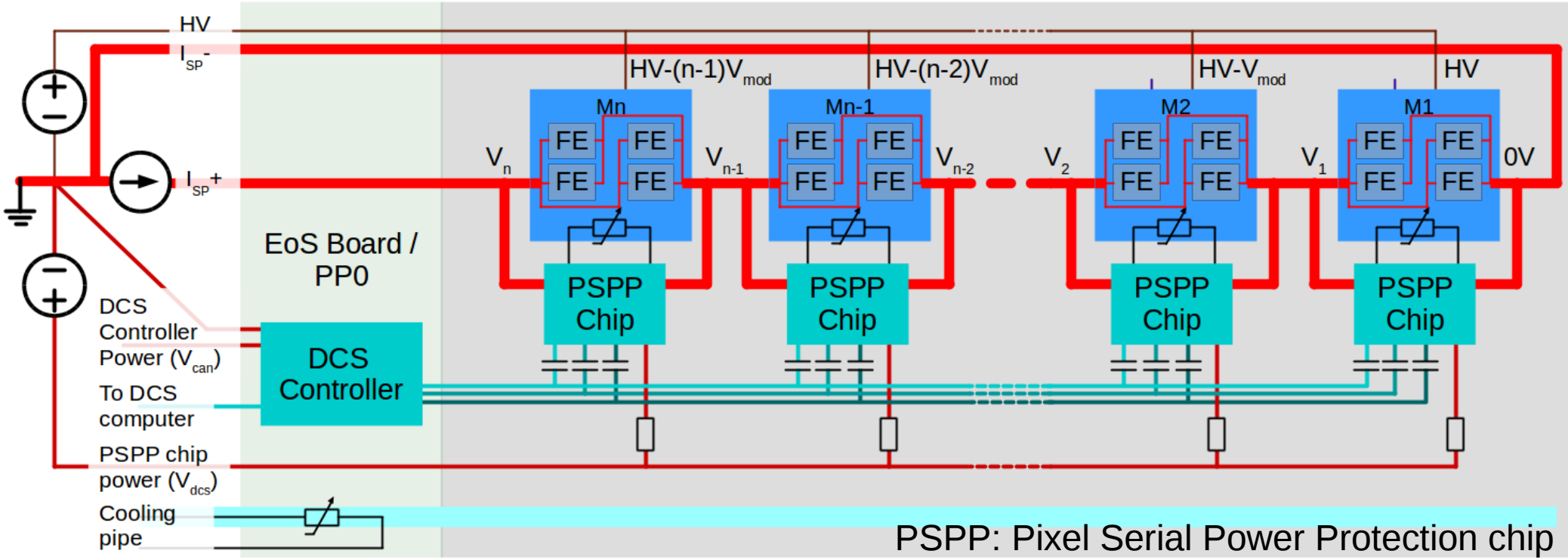
Serial Powering

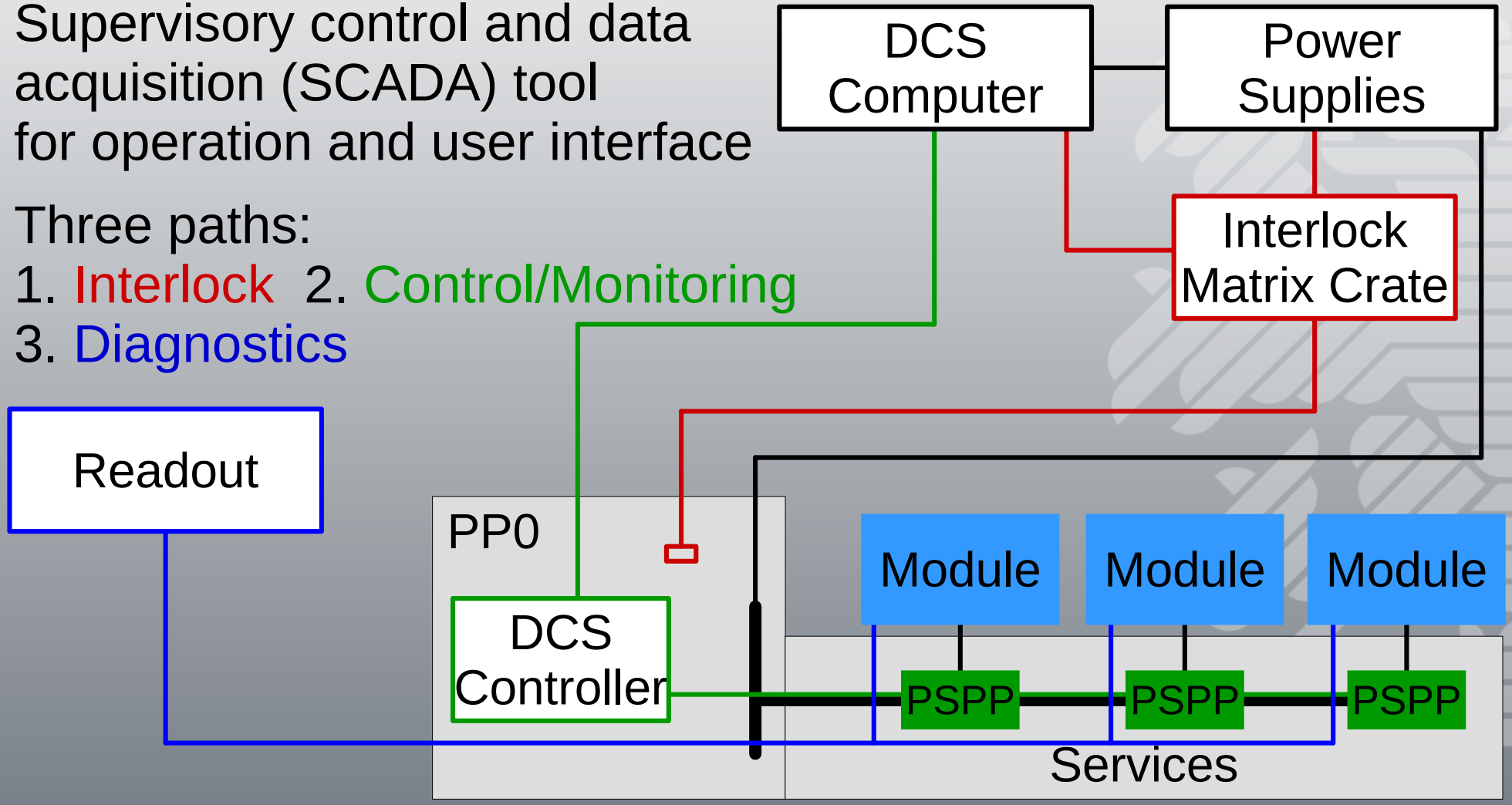


- Reduced number of supply lines
- No DC/DC converter needed
- 6-14 modules per chain
- Several HV lines per chain possible
- Each module on different potential → AC Coupling on data lines
- Protection against chain failure → Redundancy and bypass

→ A. Luengo

Detector Control System (DCS)

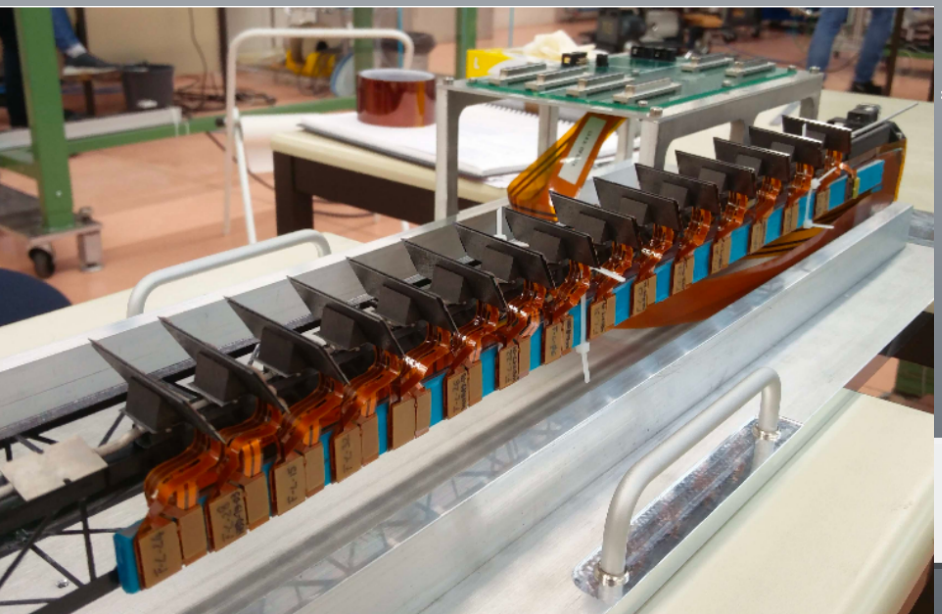
- Supervisory control and data acquisition (SCADA) tool for operation and user interface
- Three paths:
  1. Interlock 2. Control/Monitoring
  3. Diagnostics

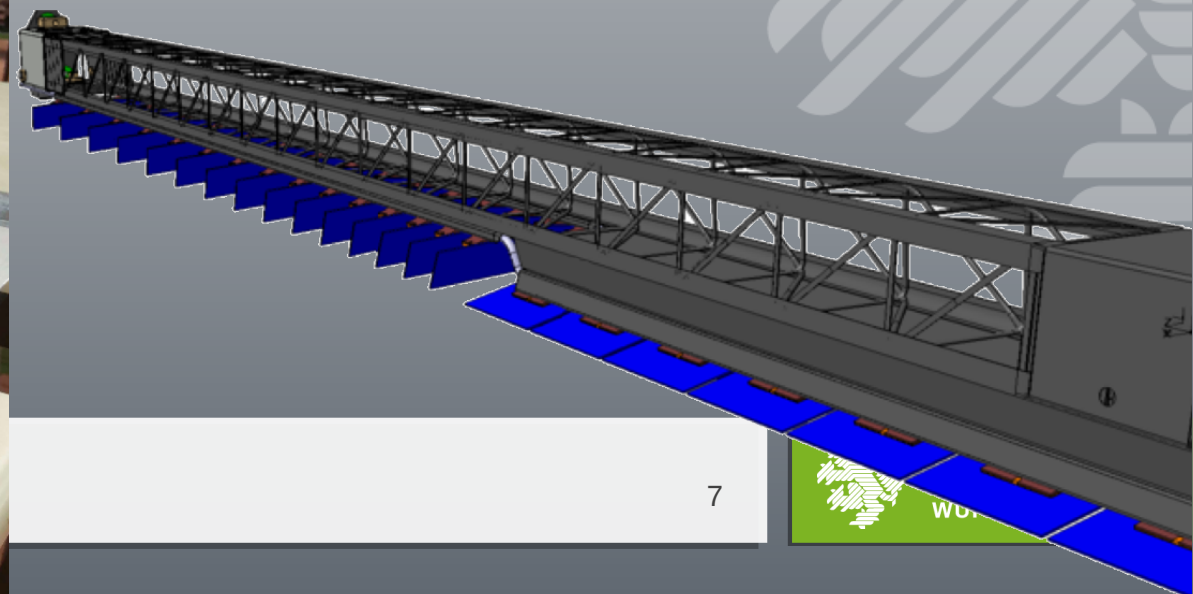


Outer Barrel Demonstrator Program

- Several prototypes to test different system aspects
  - Integration of modules
  - Thermal performance
  - Full electrical system
- Different test structures built

- Full Demonstrator
  - 6 serial power chains with electrical modules
  - Inclined section:
    4 x 8 dual-modules (2 FE)
  - Barrel section:
    2 x 7 quad-modules (4 FE)
  - 120 FE-I4 chips in total



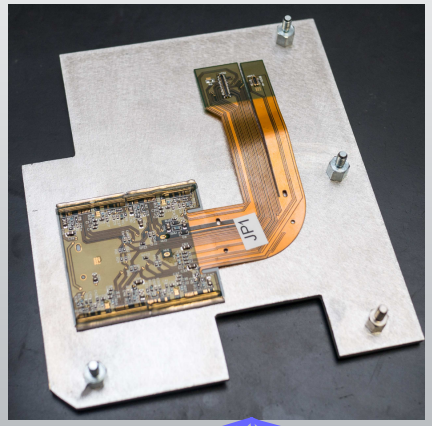


7-Module Electrical Prototype

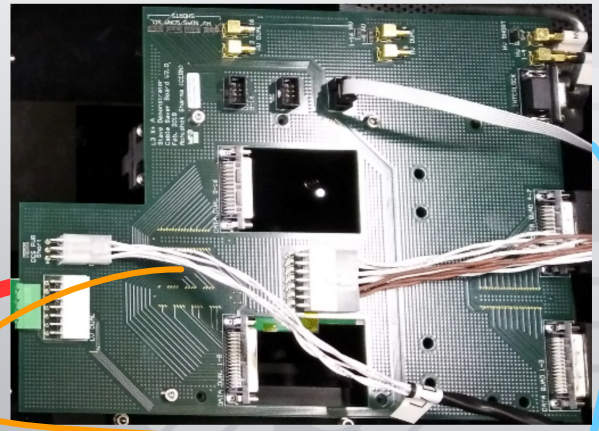
Quad Module

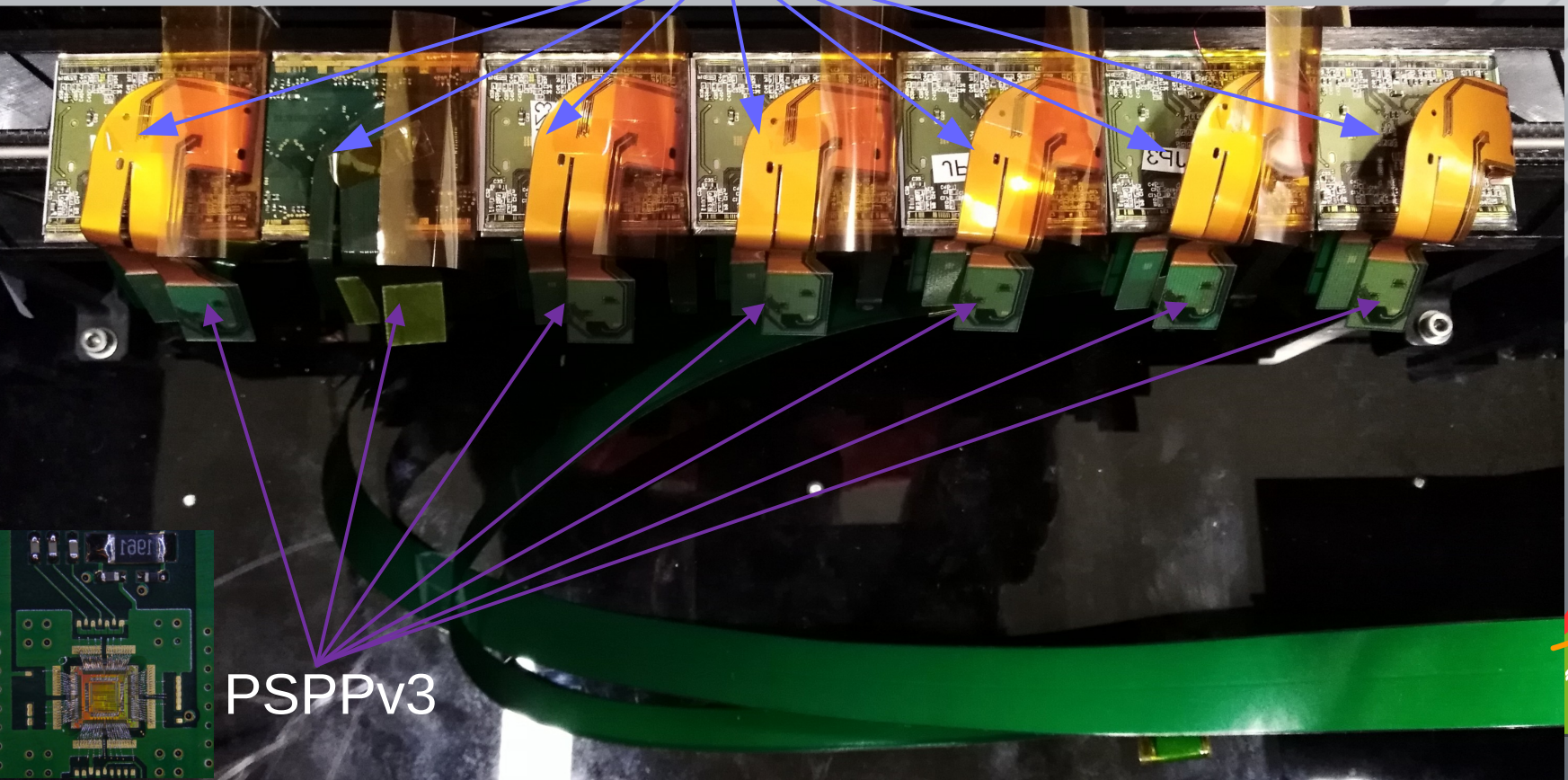
- 2A current for SP chain

- 2V per module



Cable Saver Board





PSPPv3

to DCS Controller

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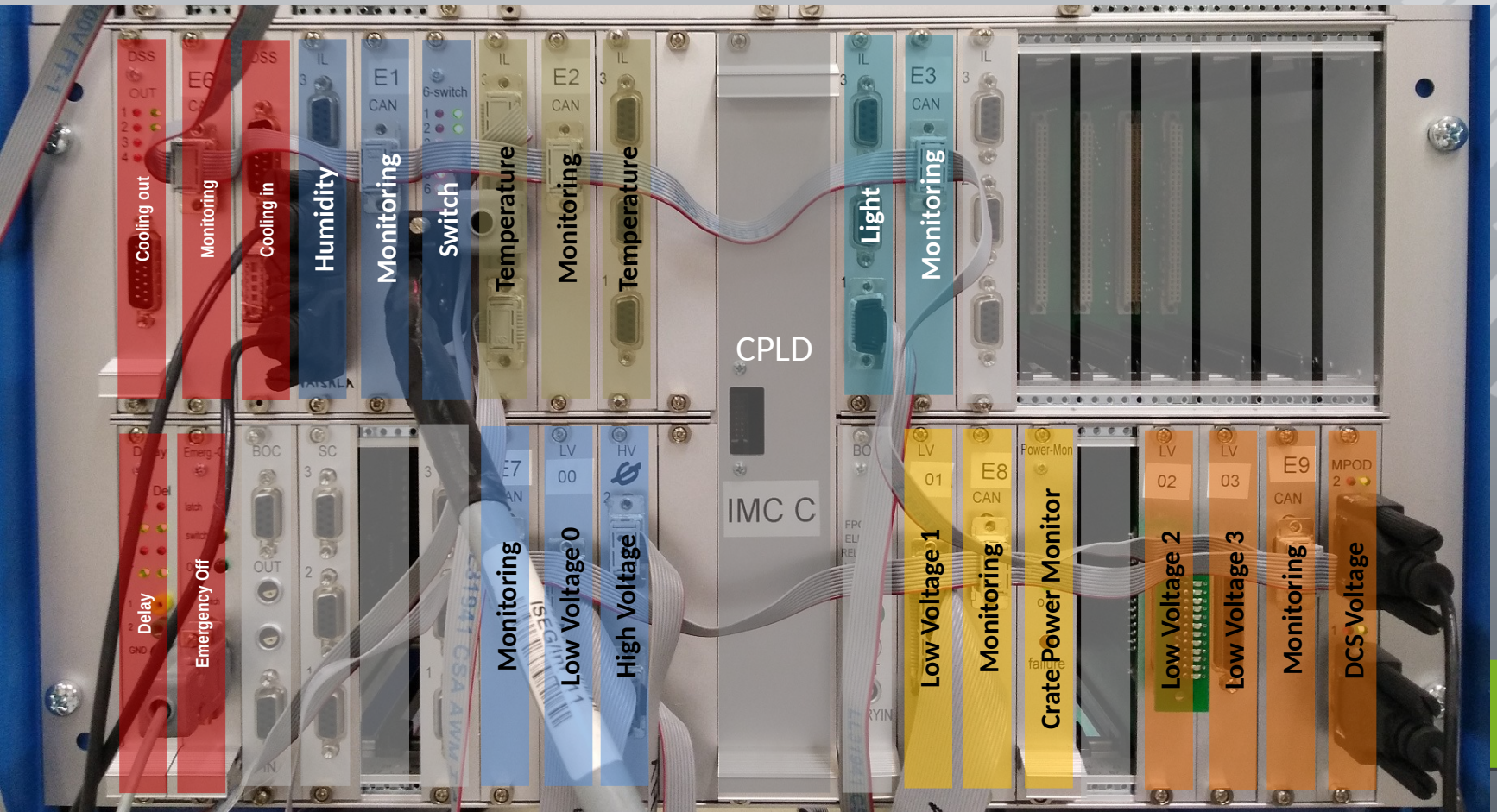
Interlock Matrix Crate

- Combinational logic with no configuration required
- Purely hardware based system
- Monitoring of sensors
- Acts on power supplies



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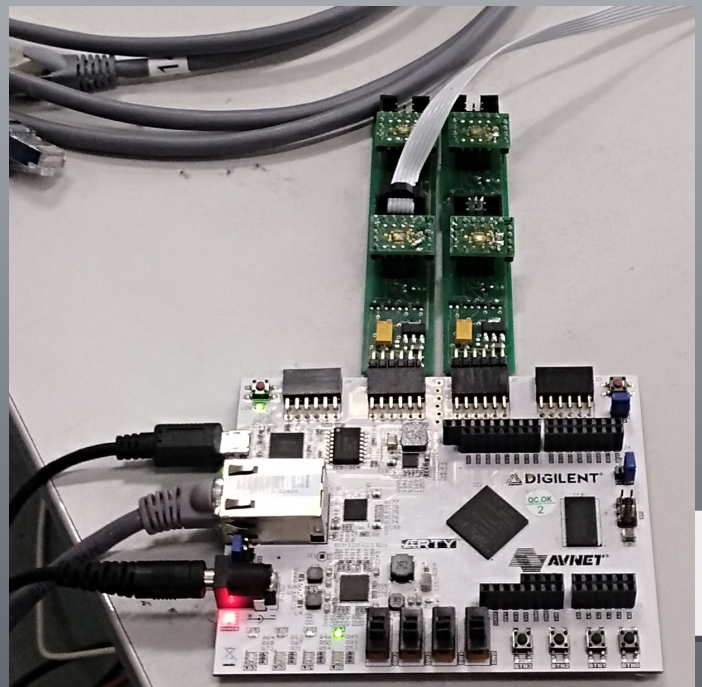
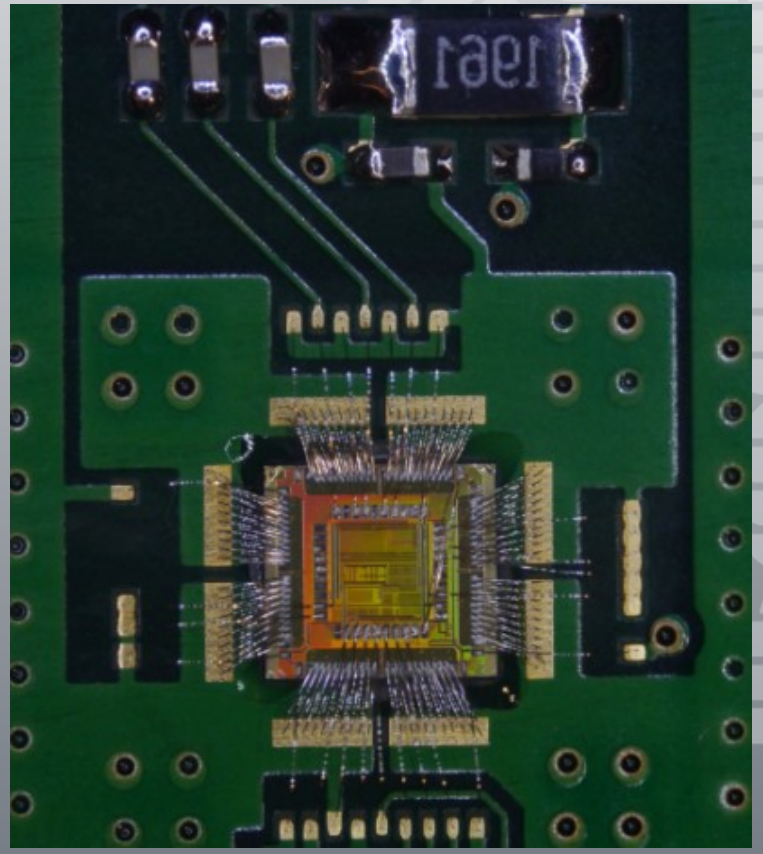
Control and Monitoring path

- Independent of readout and interlock
- Monitoring of each module in the serial power chain with the PSPP
  - Reduction of sensor cables
  - Temperature and Voltage
- Bypass to deactivate modules



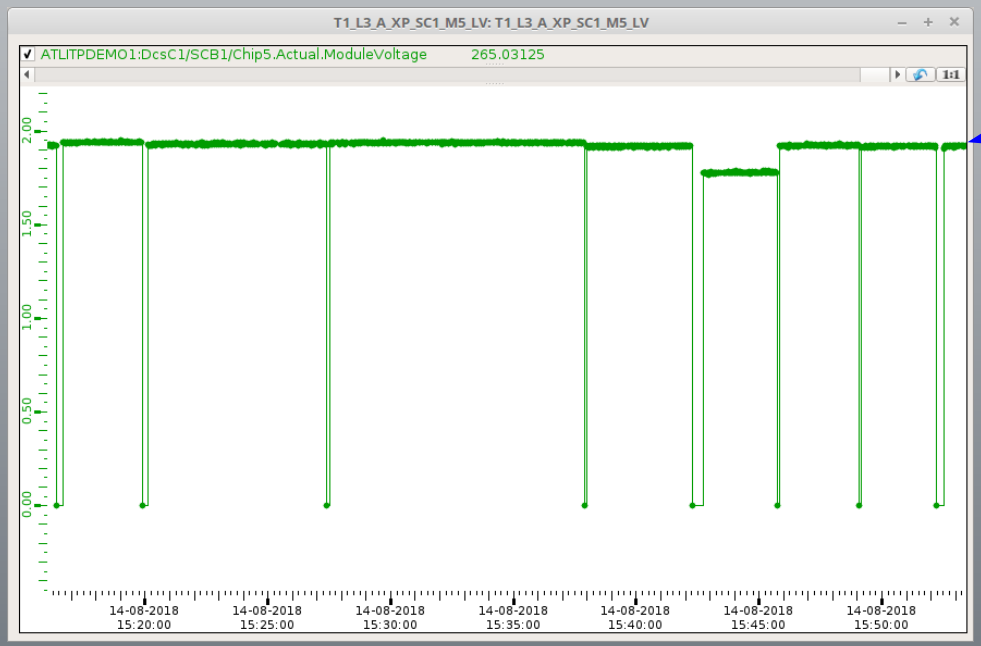
PSPPv3 mounted on flex

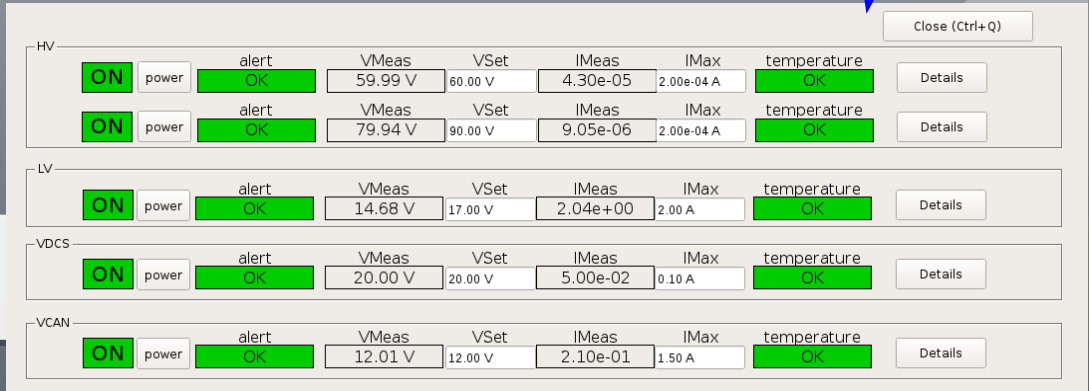


FPGA as Controller and interface to DCS Computer

User Interface and Operation

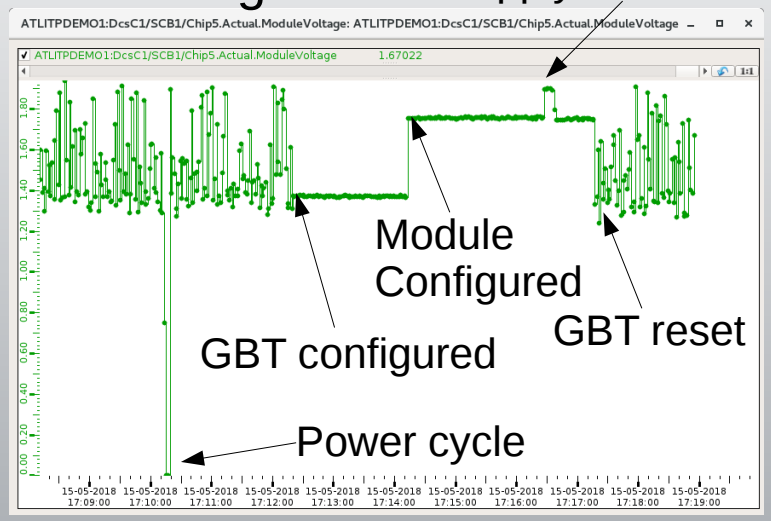
- User Interface with WinCC
- Control and operation of SP chain
  - Status and history



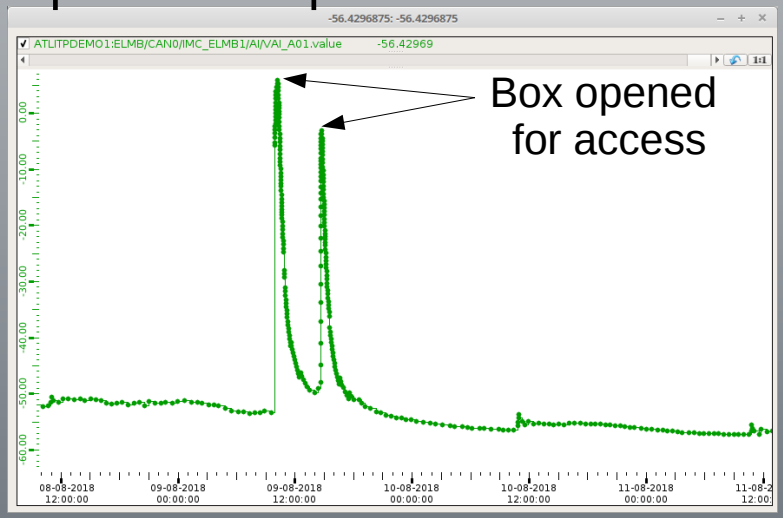


Operation of 7-Module structure

Module voltage



Setup box dew point



- Monitoring of temperature and voltage on module level
  - useful for debugging and commissioning
- Overvoltage protection used
  - Tests with noisy module
- User interface allows simple control of test system
  - Data archiving, remote access, ...

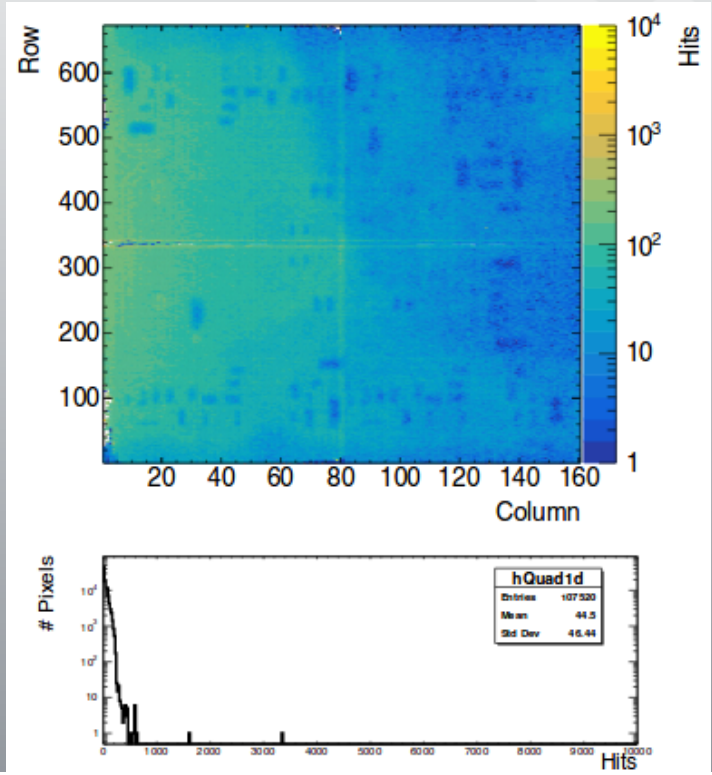
Readout Systems

- Different readout systems used
  - pyBAR, RCE, YARR, FELIX

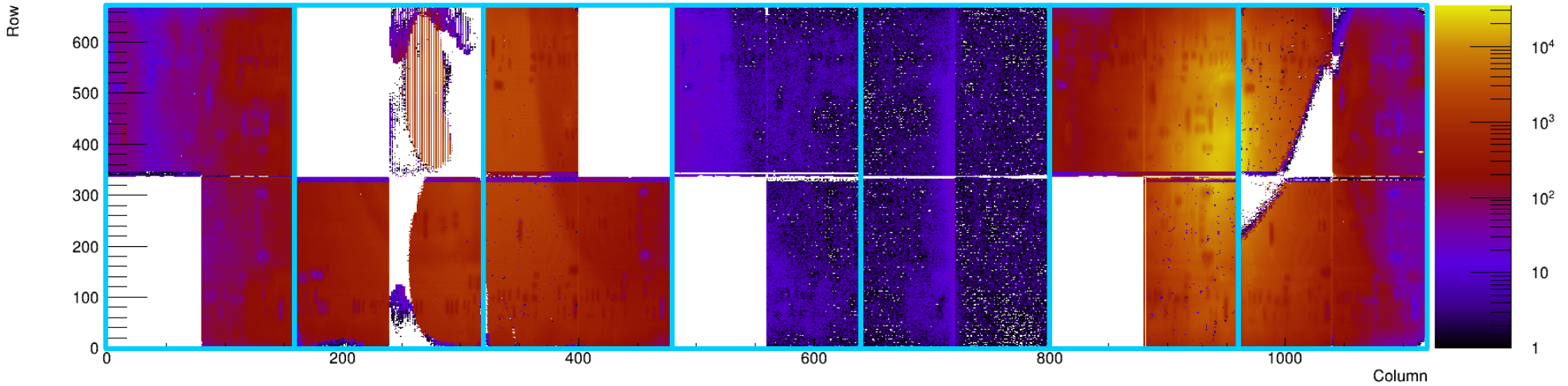
→ Talk G. Unel, Poster E. Buschmann, C. Dülsen

- Diagnostic path not yet integrated
- Movable radioactive source
- Readout with SP chain working

Source Scan with YARR

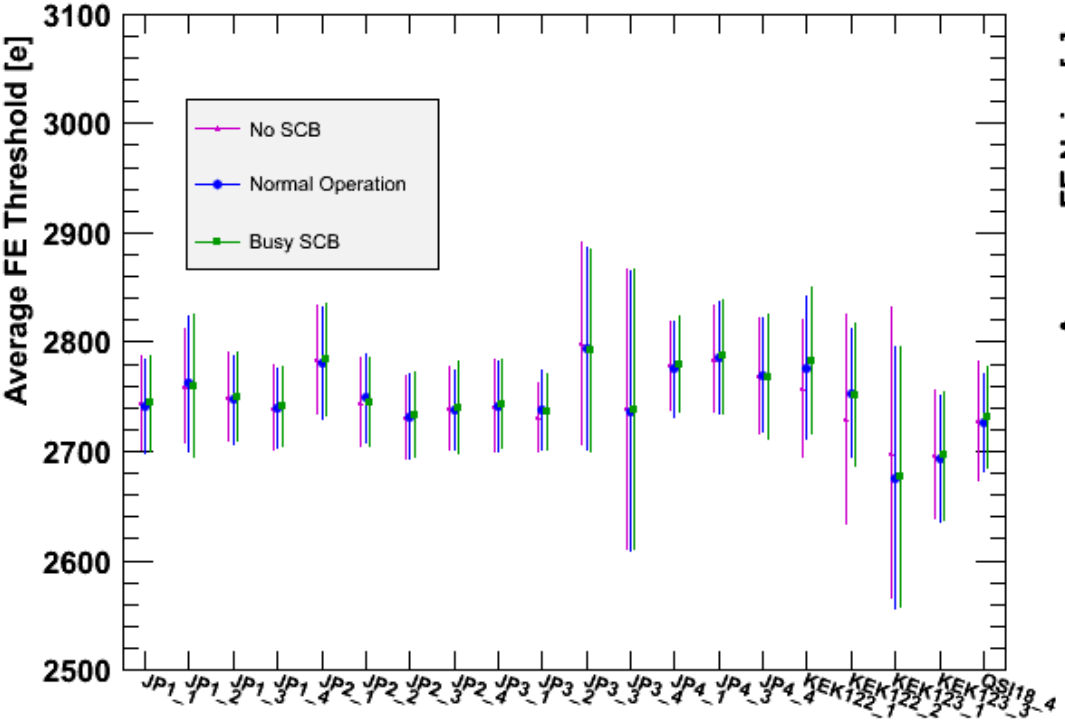


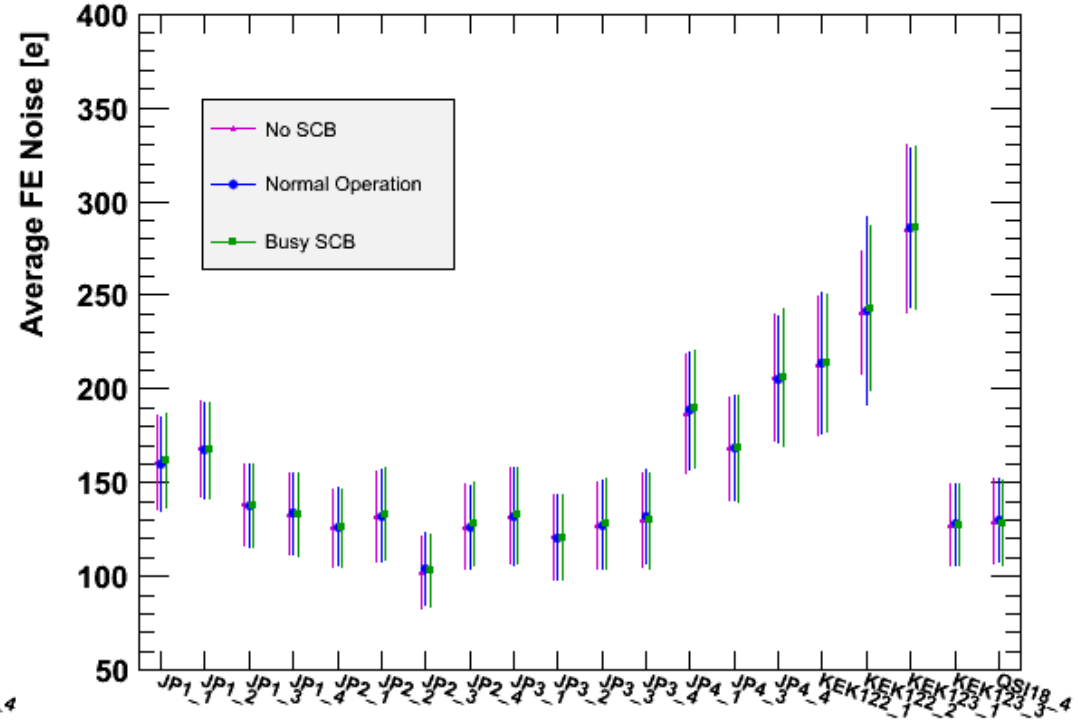
Source scan with pyBAR



DCS Noise measurements

- The PSPP communicates with a slow control bus (SCB)
  - Single ended AC coupled lines
  - Constant clock at 200kHz and Manchester encoded data at 100kBit/s
- Threshold scan performed with
  1. busy SCB, 2. normal operation, and 3. disconnected (no SCB, reference)
- No difference observed in the three cases



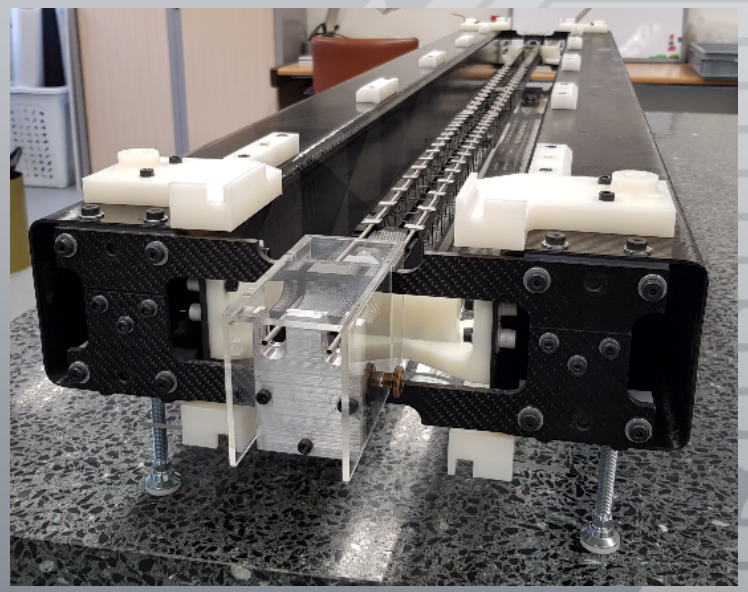


Lessons learned

- Complex system with many elements
- Full qualification of system with all components necessary
  - Found bugs in PSPP → solved in new version
  - Behavior of HV and LV supplies in a serial power chain
  - Monitoring of as many values as possible for debugging and commissioning
  - Interference of individual components leads to effects not visible in testing of single components
  - Organization and schedule of work
- Successful collaboration work

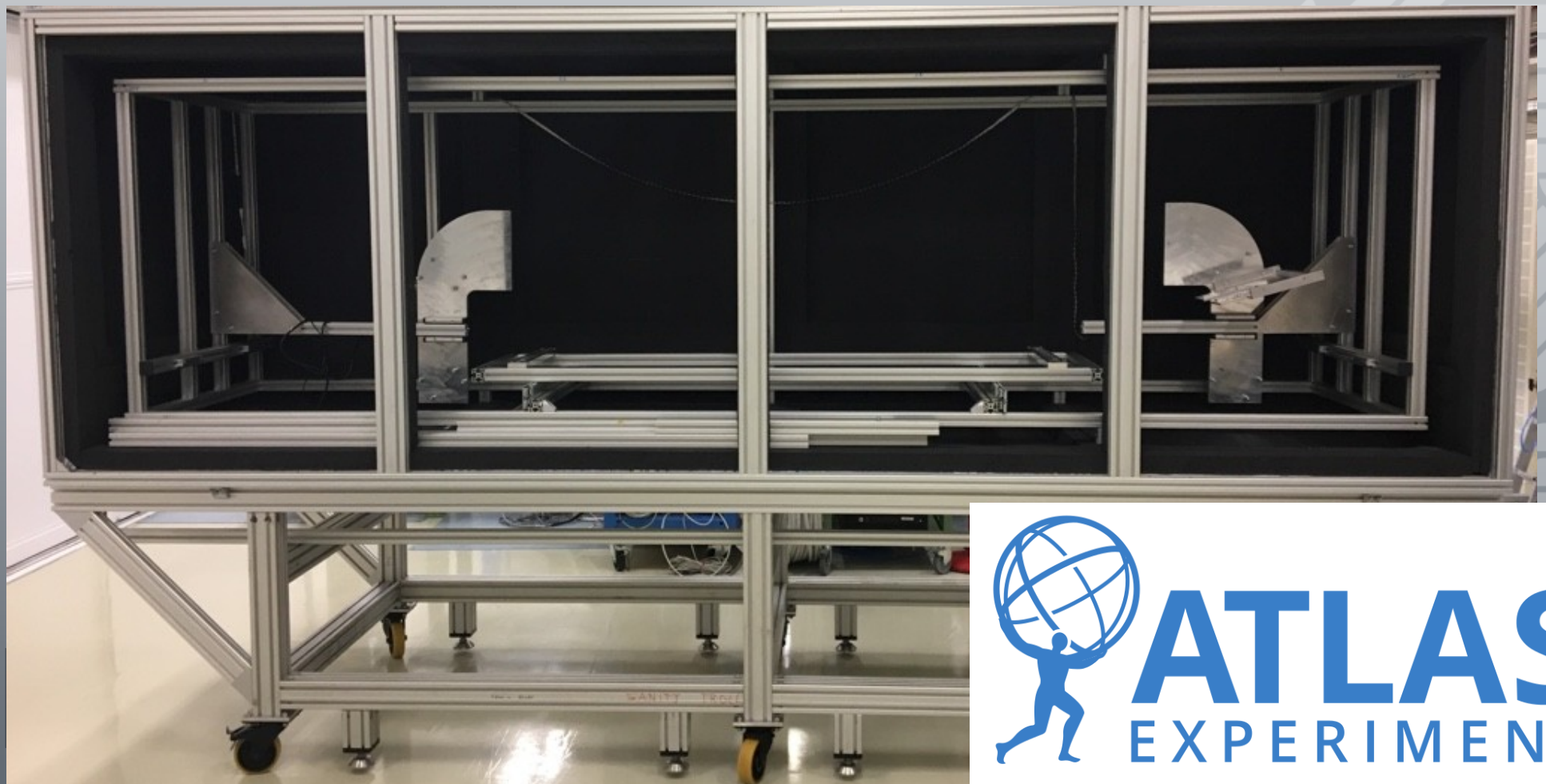
Next steps

- Finalization of full prototype
  - Mechanical integration of modules
  - Integrate all chains in DCS
- Further tests
  - Test chain with 16 modules
  - Bypass test with PSPP
  - Current source prototype
  - Readout of all 120 FE in parallel
- System test setups with RD53 modules planned



Thank you for your attention

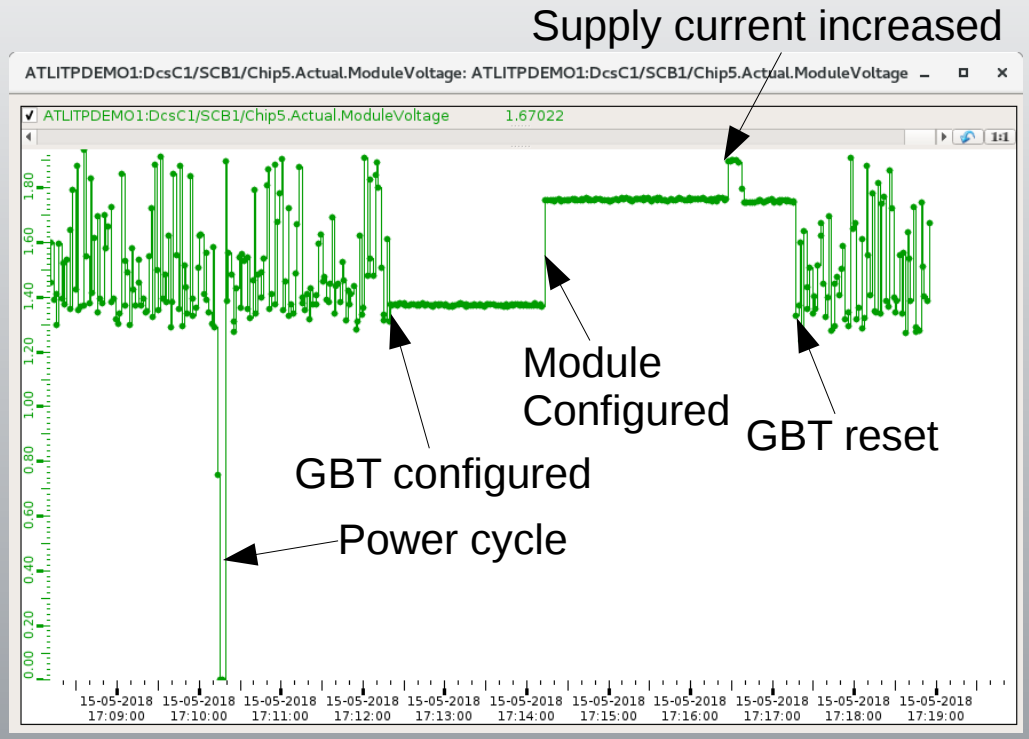
Thanks to all peoples involved in the Demonstrator program



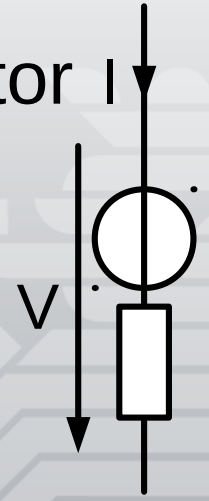
ATLAS EXPERIMENT

Backup

Voltage fluctuation caused by GBT

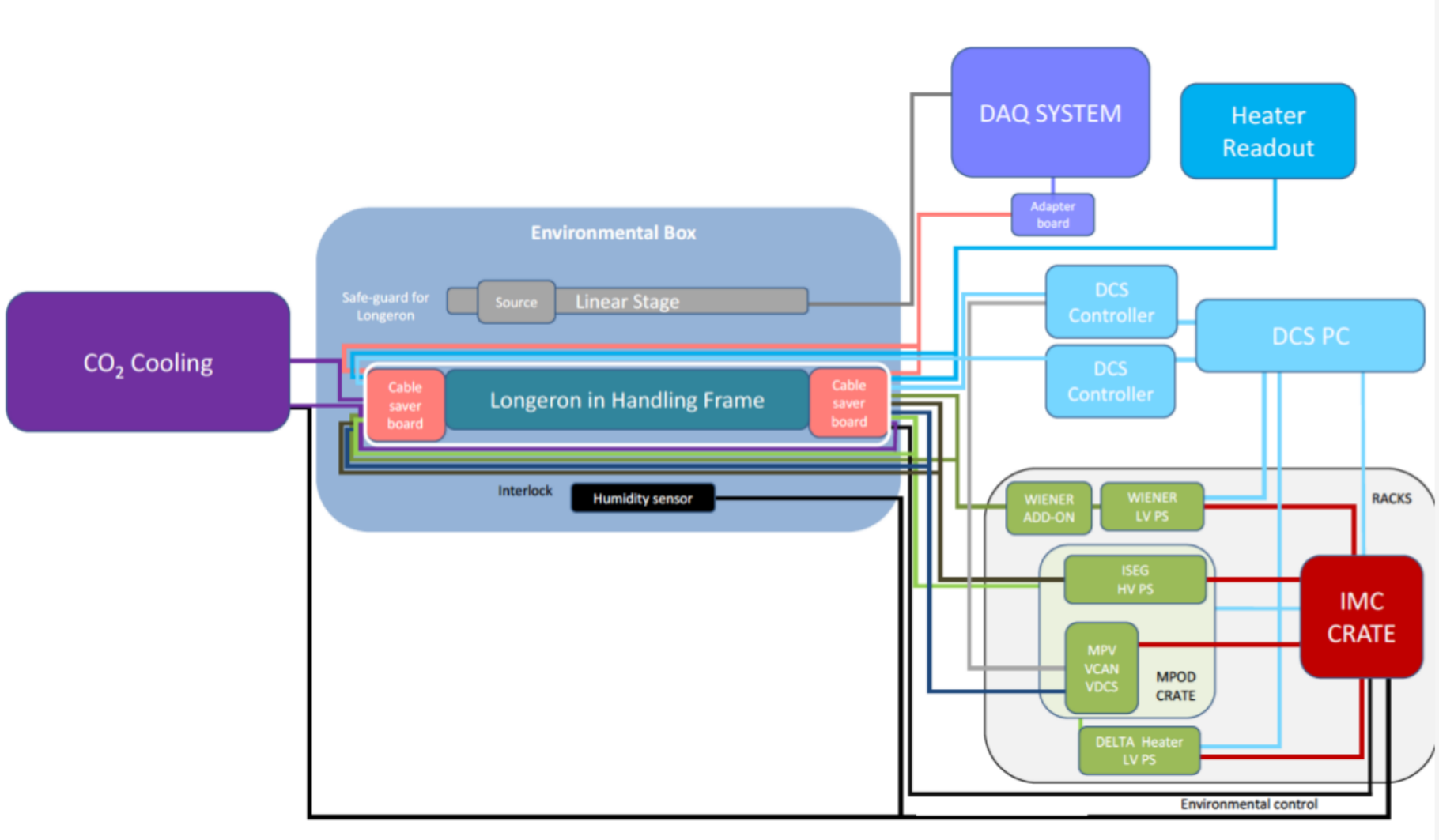


- GBT sends random data and clock when not configured
- FE doesn't check data integrity of commands



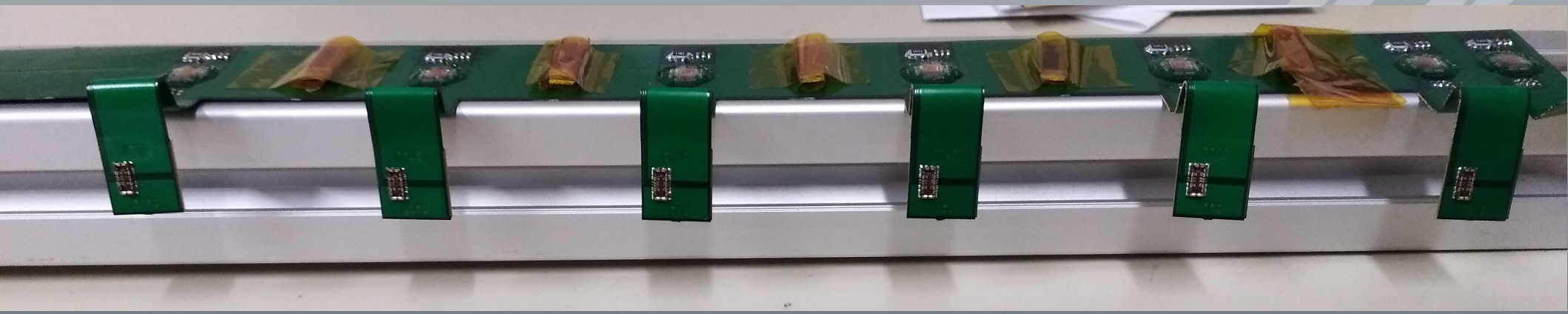
- FE behaves like a resistor plus offset voltage
  → Voltage variation not wanted in SP
- Normally constant consumption → constant voltage
- Voltage drops when shunt regulator is in overload
- Overload can be caused by wrong configuration in FE-I4

System Setup Overview

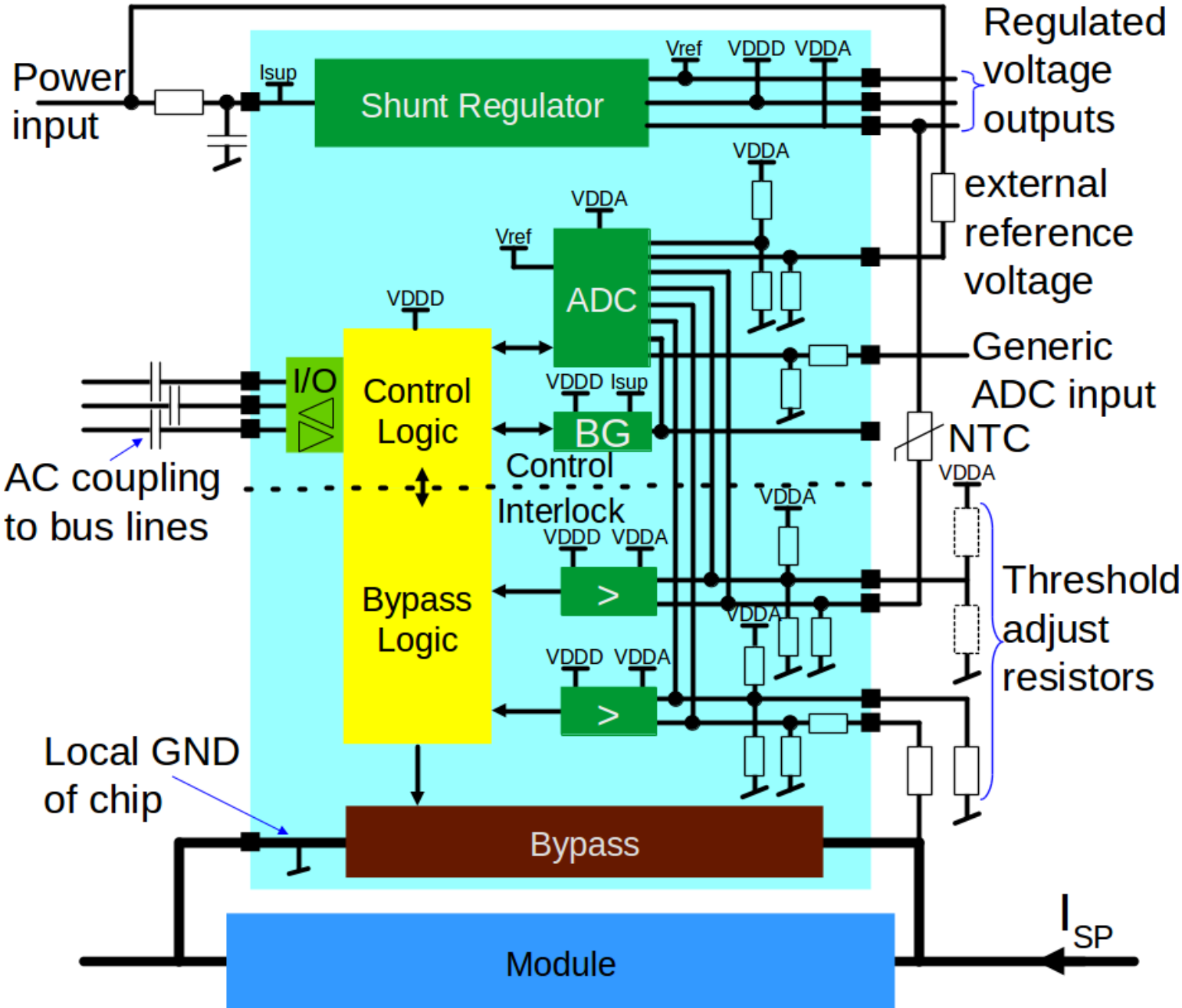


Type 0 Services

- Flex for power and data
- Power flex includes PSPPv3
- Flexes assembled and tested
- Bent and then integrated in Longeron structure

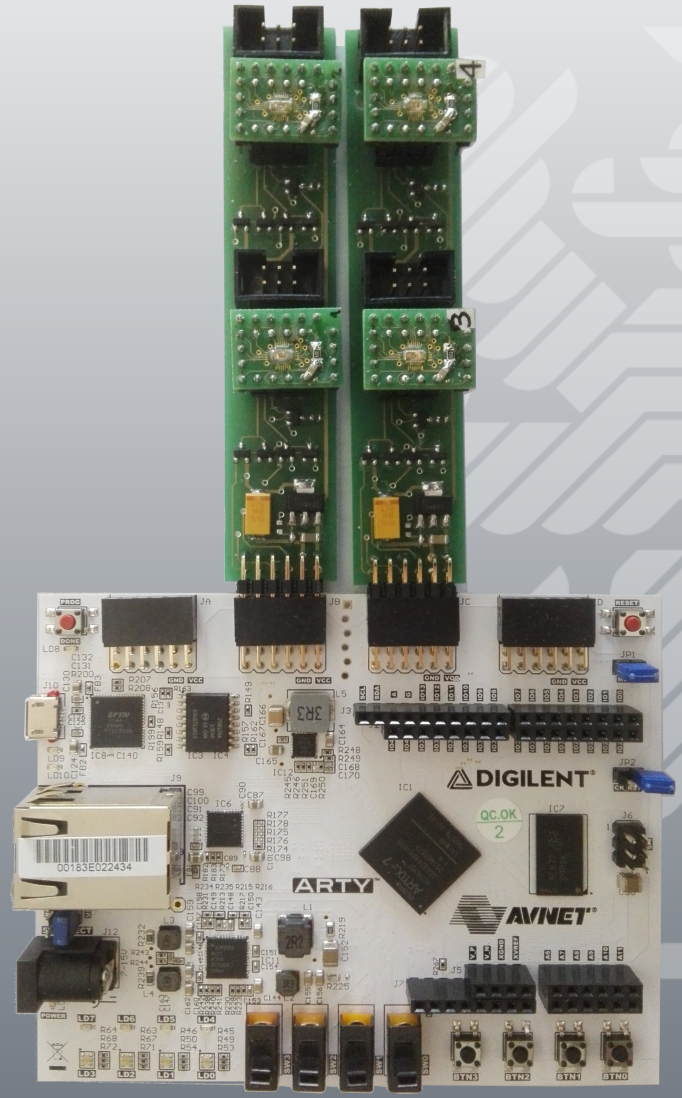


PSPPv3 Block Diagram

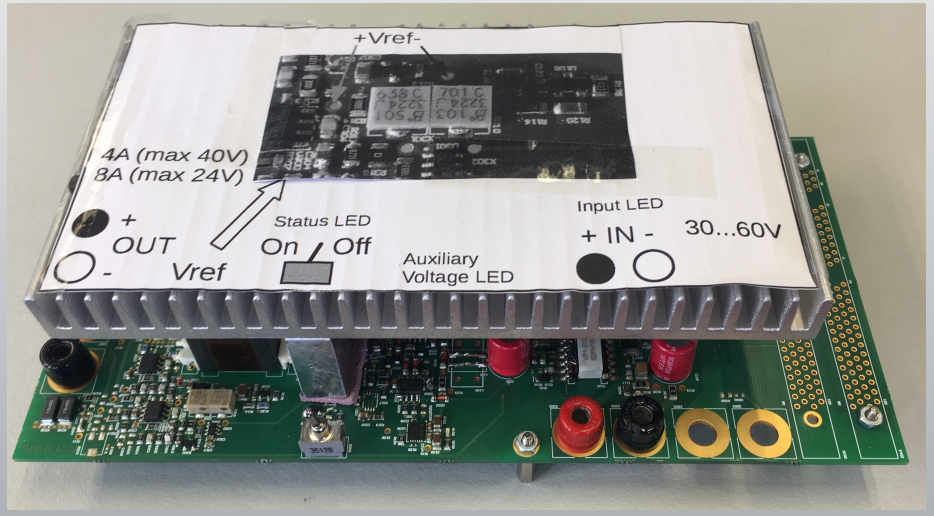


DCS Controller FPGA

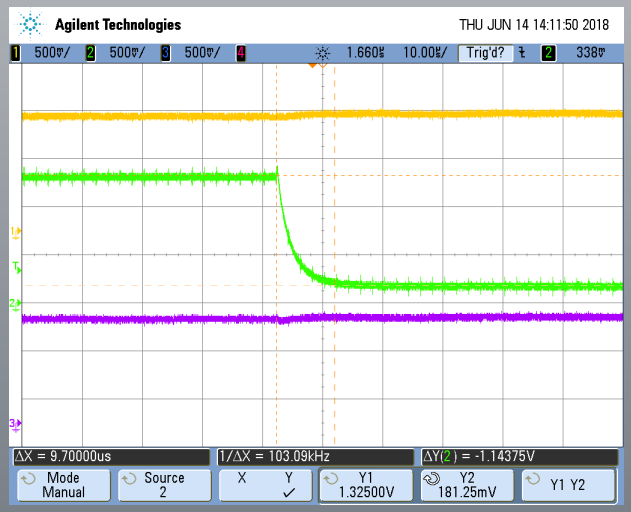
- DCS Controller in ARTIX FPGA
- Up to 4 SCB busses
  - Intended to use 2 Controllers with 3 busses each
- Communication over Ethernet
  - Modbus on TCP protocol implemented
- Modbus driver existing for WinCC
- Update with full controller logic in FPGA when available



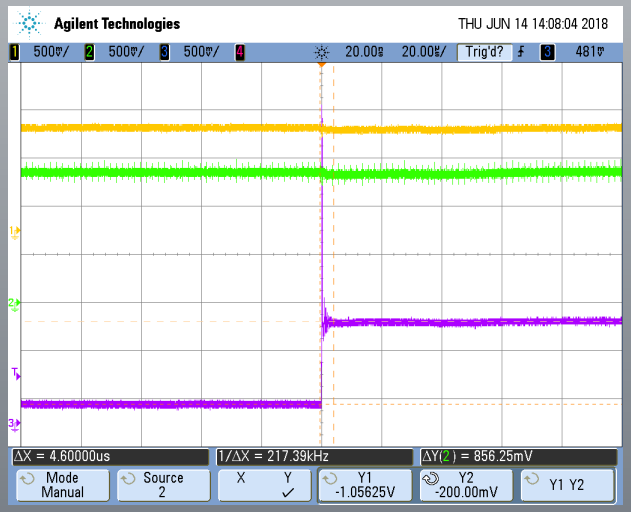
Current Source Prototype



- Current source prototype
- Improved stabilization of supplied current
- Still room for improvement



close bypass



open bypass

open bypass (lab PSU)

Readout systems

- pyBAR: Bonn ATLAS Readout in Python
  - FPGA based desktop readout system
  - For module testing
- YARR: Yet Another Rapid Readout
  - FPGA - PCIe based readout system
  - SW baseline for ITk
- RCE: Reconfigurable Cluster Element
  - GBT based with optical link
  - FPGA high speed readout cards for crate
  - Used in other ATLAS subdetectors, For system test
- FELIX: Front-End Link Exchange
  - GBT based with optical link
  - ATLAS wide readout interface
  - PCIe based

ATLAS Experiment