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D.E.C. TURBOCHANNEL TO CAMAC EXECUTIVE CRATE INTERFACE

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ABSTRACT

Hardware and software interfaces have been developed for Digital Equipment Corporation's (DEC) TURBOchannel IO bus to CAMAC. The TURBOchannel bus is currently supported on many of DEC's workstations which include DECstations using MIPS chips, Alpha AXPs and VAXstations. The hardware includes two interface cards, one which connects to the TURBOchannel in the workstation chassis and the other which is located in the CAMAC executive crate. The software has been developed for the OpenVMS VAX environment of the VAXstations and will be ported to OpenVMS AXP. This paper describes the hardware and software designs, performance and configuration details.

INTRODUCTION

The existing TRIUMF control system consists of several CAMAC highway systems. Each is called a GEC executive crate system which allows multiple CPUs (VAXes and Data General Novas) to address any of the serial or parallel branches in that system.

A pair of in-house-developed executive crate interfaces (0782/0783 modules) form the connection between the Q-bus of a VAX and the GEC executive crate. The 0782 connects to the Q-bus in the workstation chassis and the 0783 locates in the executive crate. This architecture allows multiple VAXes to access multiple executive crates and is found to be quite flexible.

Currently, DEC offers the TURBOchannel bus as an open bus and supports it on many of its workstations which include DECstations using MIPS chips, Alpha AXPs and VAXstations. Such workstations offer attractive price/performance over the computers that are presently being employed. A project was embarked on using the TURBOchannel bus from a VAXstation 4000 model 60 to access the CAMAC highway. This model offers a single TURBOchannel slot and runs the OpenVMS operating system.

Since the existing Q-bus to executive crate interface works well, the possibility of designing a TURBOchannel to Q-bus translator was considered and seemed to be a feasible approach. This required only one new module design rather than the two needed if both ends of the link were replaced. The software driver changes would also be reduced because the executive crate's module (0783) requirements were well known.

HARDWARE INTERFACE

The TURBOchannel interface is designated the 0831 TURBOchannel to Q-bus Translator. In the 0831/0783 system CAMAC arbitration and execution take place independently of the TURBOchannel operations. CAMAC operations are transparent to the software which reads or writes the 7 registers in the 0783 module. Figure 1 shows the sequence of reads and writes needed to execute a CAMAC operation. Each read or write cycle generates a Q-bus cycle between the 0831 and the 0783.

The TURBOchannel is a synchronous system in which changes of state are recognized at system clock edges while the Q-bus is an asynchronous system which depends on handshaking of signals between master and slave devices for sequencing the operations. This interface synchronizes the two systems by forcing the TURBOchannel to wait for the $\overline{rdy}$ signal while the Q-bus operation finishes (figure 2).

The Q-bus cycle shown in figure 2 starts when a TURBOchannel I/O cycle is executed to one of the memory-mapped 0783 registers. The decoded address signal *Qbus req* from the TURBOchannel triggers the Q-bus state machine to begin a transaction with the 0783 module. When the 0831 interface receives the *Qbus RPLY* signal from the 0783 it continues with TURBOchannel operation. The Q-bus state machine then finishes the Q-bus transaction with the 0783.

Figure 3 shows the functional blocks in the 0831 module. The Q-bus control logic and bus transceivers

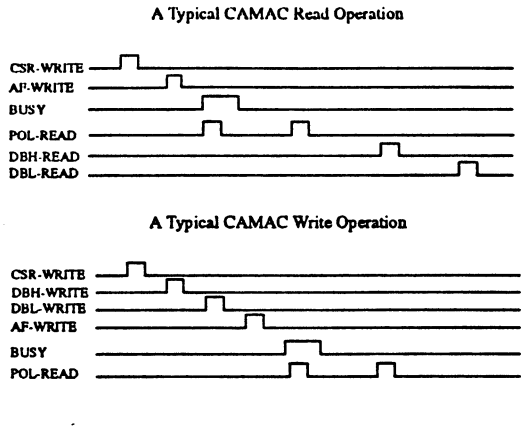

Figure 1. Timing Diagram for CAMAC Read and Write Operations

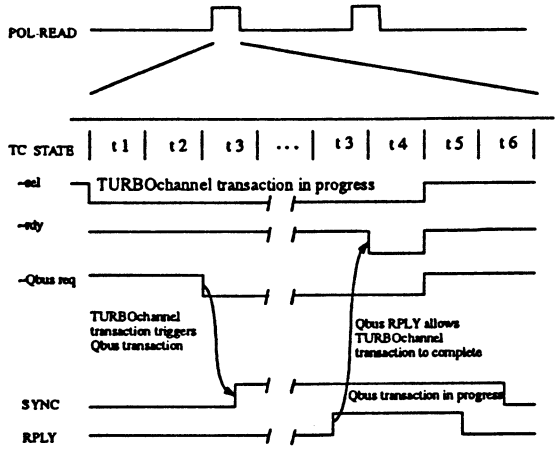

Figure 2. Timing Diagram for 0831 Module Read Operations

emulate Q-bus control signals and drive the signals over differential lines to the 0783. TURBOchannel control logic and bus tranceivers interface this module to the TURBOchannel machine. The address latch is necessary to store the Q-bus register address since address and data are multiplexed on the TURBOchannel and the address is present for only 1 system clock period. The control logic synchronizes the TURBOchannel and Q-bus state machines as well as generating the TURBOchannel and Q-bus control signals.

SOFTWARE INTERFACE

An existing software interface provides both standard and non-standard IEEE CAMAC calls in the OpenVMS VAX environment for the Q-bus configuration. This software driver was expanded to accommodate the TURBOchannel bus interface. Because the TRIUMF control system has many computers vying for arbitration in an executive crate, if any one CPU was to do multiple CAMAC cycles without rearbitrating, many computers may be held up from doing their CAMAC cycles. Such a situation has been deemed undesirable and so only programmed I/O type CAMAC access is performed. Together with the fact that a formal device driver will incur more overhead for each CAMAC call, the software interface is implemented as an installed, privileged, shareable image.

The program is written in VAX MACRO and the following calls are available: CDREG, CFSA, ZAP and EXEC_CRATE. CDREG combines the components of branch, crate, slot and A code into a single CAMAC register reference. CFSA performs a single CAMAC function. ZAP provides read/write to addresses in the I/O space. EXEC_CRATE allows inquiry and changes of the 0783 register offset which enables the caller to select more than one executive crate interface attached to that computer.

For the VAXstation 4000 model 60, the TURBOchannel I/O space starts at 30000000(hex) to 37FFFFFF, with 30000000 to 34000000 designated to the TURBOchannel devices and 34000000 to 37FFFFFF to the TURBOchannel adapter area (figure 4). In the program, 16 pages of the I/O space starting at 30000000 are mapped to a system wide global section. This allows reading and writing to the I/O space and prevents the memory from being paged out. The actual CAMAC access code is executed in kernel mode and in a protected block. Since a protected block runs in the highest interrupt priority level, IPL 31, data and code being referenced in the block are locked in memory.

The 0783 interface card has seven registers: CSR, POL, IHR, IMASK, AF, DBL and DBH. The format of the CSR and POL registers is shown in figure 5. All operations either read or write these registers. CAMAC operations are triggered by a write to the AF register and the completion of the operation is indicated by status bits in the POL register.

MULTIPLE EXECUTIVE CRATE EXPANSION

The TRIUMF control system needs to support multiple executive crates interfaces from one computer. The 0831, however, supports only one executive crate interface from each TURBOchannel slot. Two alternate designs have been considered to expand the number of interfaces supported from one slot. Both assume that the system is constrained so that only one CAMAC cycle is

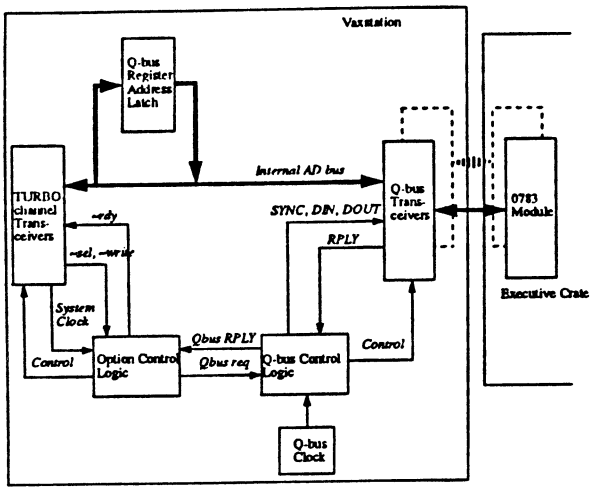

Figure 3. 0831 Module Block Diagram

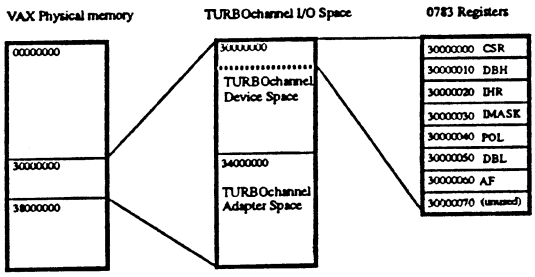

Figure 4. Addresses for 0783 Registers in the TURBOchannel I/O space

active at a time. The single active CAMAC cycle constraint is satisfied by the current software drivers.

In each design the 0831 decodes offset bits in addition to the register address to determine which 0783 to address. Polling determines when each interface has finished the requested cycle. The simpler scheme incorporates multiple sets of Q-bus line drivers and cables with each 0783 interface connected to the 0831 by a separate cable. This method leaves the 0783 design unchanged. A more efficient scheme would modify the 0783 modules to decode the address offset bits and run one cable to multiple 0783 interfaces.

Both schemes require the software driver to keep track of which interface is active but since all transactions are initiated by the driver this is not a problem. Interrupt handling is more complicated since there would be multiple interrupt sources.

SUMMARY

The design of this interface was undertaken to take advantage of the higher performance and lower cost of TURBOchannel based computers compared to the Q-bus based computers now used in the TRIUMF control system. Since a pair of modules is in use at TRIUMF for interfacing Q-bus to the executive crates it was decided to retain the executive crate module and design a TURBOchannel to Q-bus converter. In this way only one new module was needed. The new 0831 module is transparent to the VAXstation which sees the memory mapped registers residing in the executive crate module. The TURBOchannel cycle is held in a wait state while the Q-bus cycle with the executive crate module takes place.

Expansion of this scheme to support multiple executive crates with the same 0783 module from one TURBOchannel slot appears feasible by modifying the 0831 design to recognize offsets added to the 0783 register addresses.

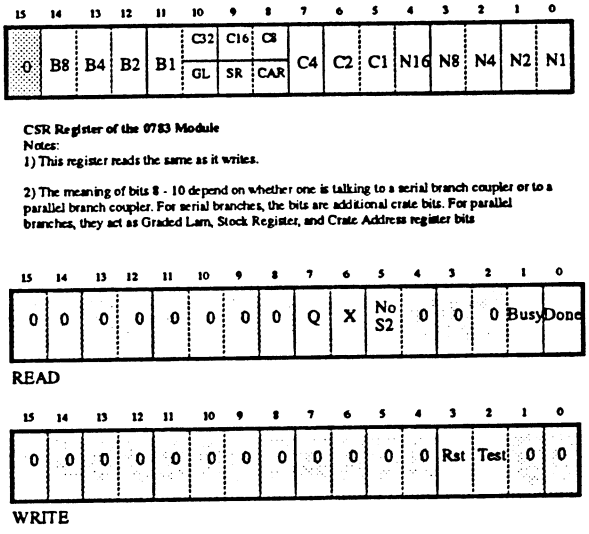

Figure 5. Format of the CSR and POL Registers for the 0783 Module

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