



## CMOS monolithic pixel sensors based on the column-drain architecture for the HL-LHC upgrade



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### ABSTRACT

Depleted Monolithic Active Pixel Sensors (DMAPS) constitute a promising low cost alternative for the outer layers of the ATLAS experiment Inner Tracker (ITk). Realizations in modern, high resistivity CMOS technologies enhance their radiation tolerance by achieving substantial depletion of the sensing volume. Two DMAPS prototypes that use the same “column-drain” readout architecture and are based on different sensor implementation concepts named LF-Monopix and TJ-Monopix have been developed for the High Luminosity upgrade of the Large Hadron Collider (HL-LHC).

LF-Monopix was fabricated in the LFoundry 150 nm technology and features pixel size of  $50 \times 250 \mu\text{m}^2$  and large collection electrode opted for high radiation tolerance. Detection efficiency up to 99% has been measured after irradiation to  $1 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ . TJ-Monopix is a large scale ( $1 \times 2 \text{ cm}^2$ ) prototype featuring pixels of  $36 \times 40 \mu\text{m}^2$  size. It was fabricated in a novel TowerJazz 180 nm modified process that enables full depletion of the sensitive layer, while employing a small collection electrode that is less sensitive to crosstalk. The resulting small sensor capacitance ( $\leq 3 \text{ fF}$ ) is exploited by a compact, low power front end optimized to meet the 25 ns timing requirement. Measurement results demonstrate the sensor performance in terms of Equivalent Noise Charge (ENC)  $\approx 11 e^-$ , threshold  $\approx 300 e^-$ , threshold dispersion  $\approx 30 e^-$  and total power consumption lower than  $120 \text{ mW}/\text{cm}^2$ .

### Contents

1. Introduction .....	605
2. Sensor implementation .....	605
3. Chip design and architecture .....	605
3.1. Chip architecture .....	605
3.2. LF-Monopix chip design .....	606
3.3. TJ-Monopix chip design .....	606
4. Measurement results .....	606
4.1. LF-Monopix .....	606
4.2. TJ-Monopix .....	606
5. Conclusion .....	607
Acknowledgments .....	607
References .....	607

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## 1. Introduction

Monolithic Active Pixel Sensors (MAPS) constitute an attractive alternative in high energy physics experiments as the building blocks of vertex detectors in high precision tracking applications. Their prominent advantage stems from the fact that the manufactured devices contain both the sensor and the front end electronics in the same silicon crystal and are ready to be used without the need for the expensive and labor-intensive process of fine pitch bump-bonding. Monolithic pixel sensors have already been successfully used in experiments with low radiation environments [1,2], but their radiation tolerance was limited. Advancements in CMOS imaging technologies that enable the use of high resistivity substrate and high voltage biasing can be exploited to achieve full depletion of the sensitive volume and generation of high electric fields to ensure fast charge collection by drift. During the phase-II of the HL-LHC upgrade, the ATLAS ITk will be improved [3] to cope with the unprecedented levels of radiation and ten times higher hit rate. A dedicated CMOS collaboration has been established to develop and characterize fully Depleted MAPS (DMAPS), for the outer layers of the ATLAS ITk. These devices are required to tolerate particle fluence up to  $1.5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$  and a Total Ionizing Dose (TID) up to 80 Mrad. Moreover they must be able to comply with the 25 ns timing requirement of the ATLAS experiment. DMAPS prototypes manufactured in different technologies have been reported with encouraging results regarding the sensor radiation tolerance [4–7]. Additionally, multiple nested wells offered by modern CMOS processes allow for complex readout circuitry to be implemented inside the pixel, enabling the use of fast readout architectures.

Two large scale DMAPS prototypes have been developed for the ATLAS ITk based on a common “column-drain” readout architecture derived from the FE-I3 front end chip [8]. The simple in-pixel logic does not severely constrain the pixel dimensions and the hit rate capabilities of this approach are well established and exceed the requirements of the ITk outer layers. A different sensor implementation concept was pursued in each chip. The first prototype, called LF-Monopix, is based on a large collection electrode and is manufactured in the LFoundry 150 nm HV-CMOS process. The second prototype, called TJ-Monopix, employs a small collection electrode and is fabricated in the TowerJazz 180 nm imaging process using a novel modification to enhance radiation tolerance [9]. The radiation hardness of LF-Monopix and the implemented large collection electrode sensor has been proven by beam test results. Full functionality of TJ-Monopix after irradiation is demonstrated here for the first time and its performance is evaluated by laboratory and radioactive source measurement results reported in this work.

## 2. Sensor implementation

A crucial factor in the design of monolithic pixel sensors, that affects radiation tolerance and performance of the detector is the geometry of the collection electrode. In Fig. 1(a) the cross section of the LF-Monopix pixel sensor is depicted. The collection electrode is formed by a large very deep n-well that includes all the in-pixel electronics. A high resistivity ( $>2 \text{ k}\Omega \text{ cm}$ ) p-type substrate constitutes the sensitive volume that can be biased to high voltages. Its depth can vary from  $750 \mu\text{m}$  to  $100 \mu\text{m}$  after backside processing. The generated strong and uniform electric field ensures high radiation tolerance to Non Ionizing Energy Loss (NIEL) damage and high charge collection efficiency [4,6]. The disadvantage of this implementation is the large sensor capacitance ( $\approx 300\text{--}400 \text{ fF}$ ) that degrades the analog performance in terms of noise and signal rise time, and has to be compensated with increased power consumption. Additionally, significant design efforts are needed to reduce the crosstalk noise from the in-pixel digital activity that is coupled to the input node.

In contrast, a different concept is pursued in TJ-Monopix. A small n-well is used as the collection electrode and the in-pixel electronics are implemented around it. The most important benefit of this geometry

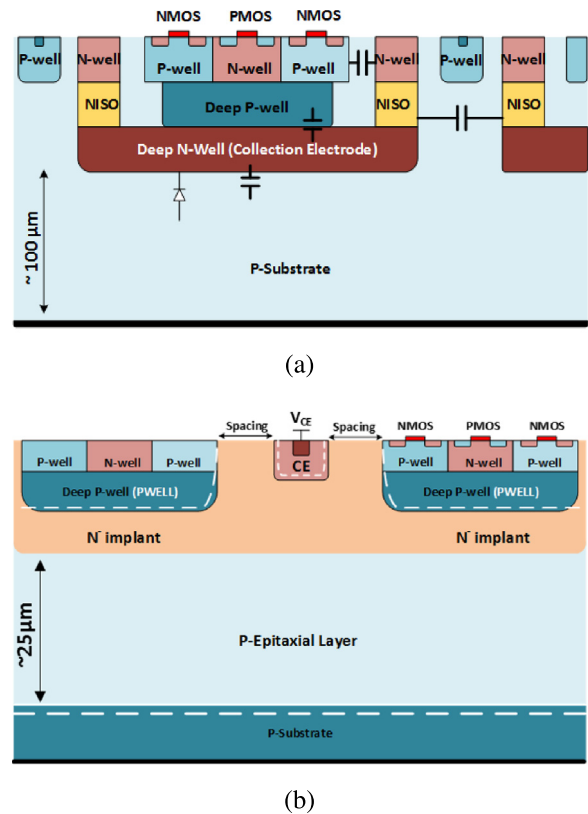


Fig. 1. (a) LF-Monopix and (b) TJ-Monopix sensor design cross section.

is the very small sensor capacitance ( $\approx 3 \text{ fF}$ ) that allows for very low noise and fast signal timing while keeping the power consumption minimal. Furthermore, crosstalk noise coupling is substantially reduced. The PMOS transistor n-wells are shielded by deep p-well implants. A  $25 \mu\text{m}$  thick, high resistivity ( $>1 \text{ k}\Omega \text{ cm}$ ) p-type epitaxial layer that is grown on a low resistivity substrate is used as the sensitive volume. To fully deplete the epitaxial layer and enhance radiation tolerance, a process modification has been developed [9]. As depicted in Fig. 1(b), a planar n-layer that realizes two p–n junctions is implanted over the full pixel area. As a consequence, the depletion boundary is extended laterally, to the otherwise undepleted part of the sensitive layer, even for small reverse bias voltages. Small pixel size is essential to reduce the distance between collection electrodes and ensure that the electric field is not degraded in the area between pixels. Measurement results from a test chip manufactured in the modified process to assess the sensor performance are very promising [5]. Charge collection efficiency remains uniform and high ( $>95\%$ ) and the signal timing is still fast after irradiation to  $1 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ .

## 3. Chip design and architecture

### 3.1. Chip architecture

Both prototypes follow the same basic architecture scheme that is depicted in Fig. 2. Their differences in terms of readout logic are limited to implementation details and layout organization. A 40MHz Bunch Crossing ID (BCID) time stamp, generated by a gray counter is distributed over the whole matrix. After a hit pulse is produced by a pixel’s analog front end, the Leading Edge (LE) and Trailing Edge (TE) information are stored in local in-pixel RAM memories. Arbitration over the common data bus is based on a token that is propagated with priority through the column from top to bottom and through different columns from left to right. A busy token flag is sent to the external

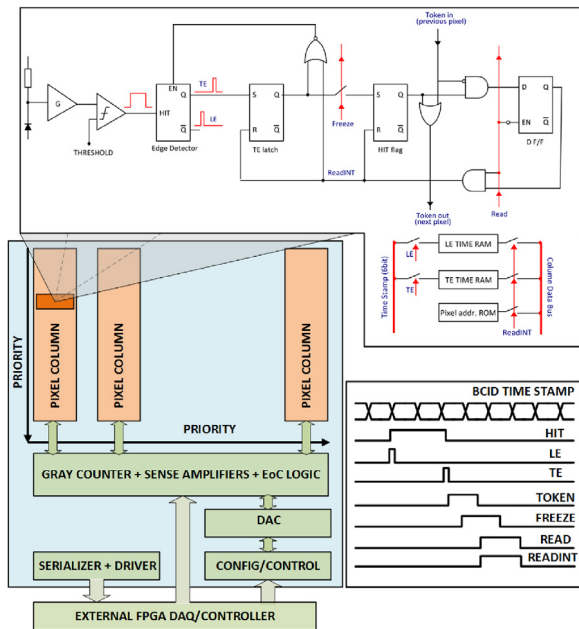


Fig. 2. Chip architecture of LF-Monopix and TJ-Monopix.

Data Acquisition (DAQ) controller that initiates and controls the readout sequence. A local read signal is produced in the pixel that has been hit and has the highest priority to transmit the hit data. The data received from the RAM sense amplifiers at the end of each column are arbitrated by the end of column logic (EoC), and sent to the DAQ system using a 160 Mbps serial link. A trigger memory has not been implemented in the current prototypes and hit data is sent out immediately.

### 3.2. LF-Monopix chip design

The LF-Monopix chip [6,7,10] is the successor to CCPD\_LF and LF-CPIX [4,6] development line in 150 nm LFoundry technology and the first to incorporate a full standalone fast readout. It consists of a  $129 \times 36$  matrix of pixels with  $50 \times 250 \mu\text{m}^2$  size, while its total size is  $10 \times 9.5 \text{ mm}^2$ . Special guard ring structures enable high voltage biasing up to 280 V before breakdown. An AC coupled charge sensitive amplifier (CSA) is used to amplify the input signal. The discriminator can be tuned by an in-pixel 4-bit DAC to reduce threshold dispersion. Each pixel consumes  $\approx 36 \mu\text{W}$  of power yielding a total analog power consumption equal to  $290 \text{ mW}/\text{cm}^2$ . The matrix is not uniform and consists of nine pixel flavors with different discriminator and CSA implementations. To reduce crosstalk noise, the peak transient currents of the readout logic and therefore the injected current to the sensitive node must be minimized. To this end, techniques that include current steering logic and column bus readout through a current-limiting source follower have been used [10].

### 3.3. TJ-Monopix chip design

Promising results of the modified process test chip encouraged the design of two large scale prototypes based on the same technology and front-end, called MALTA [11] and TJ-Monopix [7,12] featuring different readout schemes. The small sensor capacitance yields a very high input signal equal to  $\approx 15 \text{ mV}$  for the Most Probable Value (MPV)  $1500 e^-$ . The high input signal to noise ratio can be exploited by a compact, non-conventional, low power front-end derived from the ALPIDE chip [13], that has been optimized for fast timing performance to meet the 25 ns requirement. TJ-Monopix chip layout is shown in Fig. 3. It features a  $448 \times 224$  small size pixel ( $36 \times 40 \mu\text{m}^2$ ) matrix, while

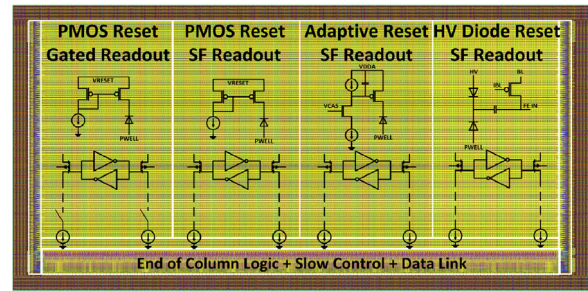
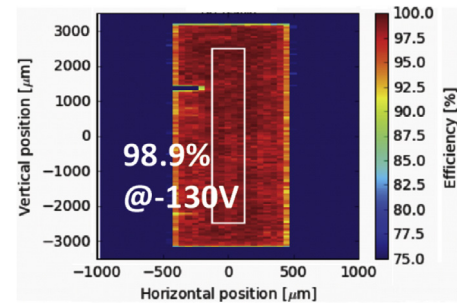


Fig. 3. TJ-Monopix chip layout.

Fig. 4. LF-Monopix detection efficiency measurement after irradiation to  $1.5 \cdot 10^{15} n_{\text{eq}}/\text{cm}^2$  [6].

the total chip dimensions are  $1 \times 2 \text{ cm}^2$ . The analog power consumption is  $< 65 \text{ mW}/\text{cm}^2$ , and combined with the 6-bit time stamp distribution the total power consumption is only  $120 \text{ mW}/\text{cm}^2$ . No in-pixel threshold tuning has been implemented since the front-end has been carefully designed for low threshold dispersion ( $< 30 e^-$ ). The matrix is split in four flavors. Apart from the standard pixel variation that features a PMOS input reset scheme, a novel leakage current compensation circuit and the possibility to bias the sensor with high voltage from the front-side are explored. A low power column bus readout variation is also implemented.

## 4. Measurement results

### 4.1. LF-Monopix

LF-Monopix chips have been irradiated with neutrons up to  $1.5 \cdot 10^{15} n_{\text{eq}}/\text{cm}^2$  at the Jozef Stefan Institute reactor while the chips received an additional 1 Mrad background TID. The breakdown voltage has been measured equal to 280 V before irradiation [7], while after irradiation it drops to  $\approx 200 \text{ V}$  and is still adequate to fully deplete the sensor. By applying a sophisticated threshold tuning algorithm based on the pixel noise occupancy, the threshold was tuned to  $1500 e^-$  with a dispersion of  $\approx 100 e^-$ . The achieved threshold value is low compared to the MPV, which is higher than 12 keV for an unirradiated sample and 4.5 keV after irradiation [6]. While the threshold value is not significantly affected after irradiation, the ENC did increase from  $200 e^-$  to  $350 e^-$  due to the background TID, with a dispersion equal to  $30\text{--}70 e^-$  depending on the CSA flavor. The input charge to output voltage gain has been measured equal to  $12 \mu\text{V}/e^-$  and is not degraded after irradiation. Fig. 4 shows the high detection efficiency (98.9%) of an irradiated LF-Monopix chip that was cooled down to  $-40 \text{ }^\circ\text{C}$ , measured in a 2.5 GeV electron beam [6]. The noise occupancy during the measurement was  $< 10^{-6}/25 \text{ ns}$ .

### 4.2. TJ-Monopix

While TJ-Monopix wafers were received in February 2018, and extensive characterization is currently in progress, first laboratory results are available. TJ-Monopix chips were also irradiated up to  $1.5 \cdot$

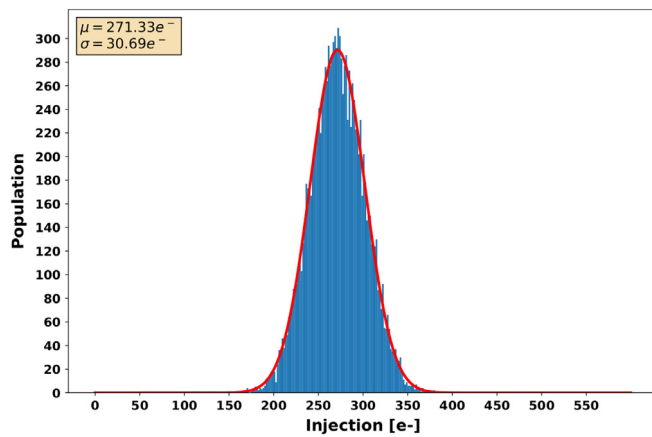


Fig. 5. TJ-Monopix threshold scan: PMOS input reset flavor, p-well =  $-5$  V, substrate =  $-20$  V.

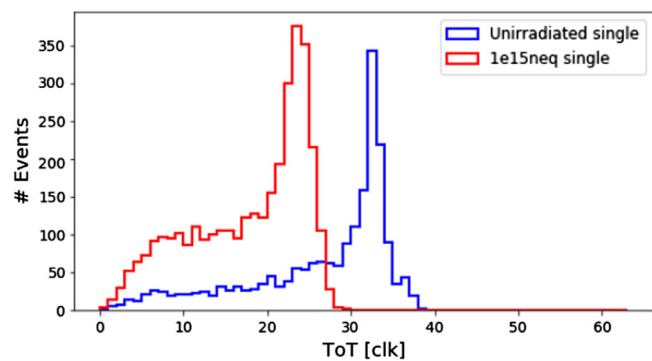


Fig. 6. TJ-Monopix  $^{55}\text{Fe}$  spectrum before and after irradiation to  $1.5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ : HV-AC coupled pixel flavor, p-well =  $0$  V, substrate =  $-16$  V, HV =  $+30$  V.

$10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$  and  $1$  Mrad background TID, and remain fully functional. Since the sensor is fully depleted, the p-well potential inside the matrix can be separate from the epitaxial layer potential. The minimum p-well bias voltage is  $-6$  V, while the substrate biasing is limited by the minimum voltage before punchthrough between the p-well and the epitaxial layer occurs and is equal to  $-20$  V [9]. The maximum front-side biasing voltage when using the special AC coupled flavor is  $+50$  V. The noise performance and threshold were measured for the PMOS input reset flavor with p-well biasing =  $-5$  V and substrate biasing =  $-20$  V. ENC was measured equal to  $11 e^-$  with  $0.8 e^-$  dispersion in agreement with simulation and the gain has been measured equal to  $0.4 \text{ mV}/e^-$ . The high gain and low noise are a direct consequence of the small sensor capacitance. As shown in Fig. 5, the threshold was measured equal to  $271 e^-$  with dispersion equal to  $30.7 e^-$ . The noise occupancy that corresponds to these measurements is  $\approx 4 \cdot 10^{-8}/25$  ns. After irradiation, ENC is increased to  $20 e^-$  and the threshold is increased to  $470 e^-$  with dispersion equal to  $50 e^-$ .

Fig. 6 depicts the spectrum of an  $^{55}\text{Fe}$  source that was measured using the AC coupled HV flavor pixels and the ToT charge information. The bias voltages were set to p-well =  $0$  V, substrate =  $-20$  V, HV =  $+30$  V. The measurement was repeated using an irradiated chip. The  $K_{\alpha}$  ( $5.9$  KeV) and  $K_{\beta}$  ( $6.5$  KeV) peaks produced by the electron capture decay of  $^{55}\text{Fe}$  to  $^{55}\text{Mn}$  are visible for the unirradiated case while for the irradiated chip, only the  $K_{\alpha}$  peak is clearly visible. It must be noted that the peak amplitude is degraded after irradiation due to the different front end settings, that were applied to increase the threshold and lower the noise occupancy.

## 5. Conclusion

Two large scale prototype chips based on the same fast readout architecture were implemented to demonstrate the feasibility of depleted monolithic active pixel sensors for the harsh radiation environment of the ATLAS ITk. The LF-Monopix radiation tolerance has been proven by means of  $\approx 99\%$  efficiency after irradiation to  $1.5 \cdot 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$  while the TJ-Monopix chip remains functional after the same level of irradiation and first measurement results demonstrate the high analog performance of the small collection electrode implementation.

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